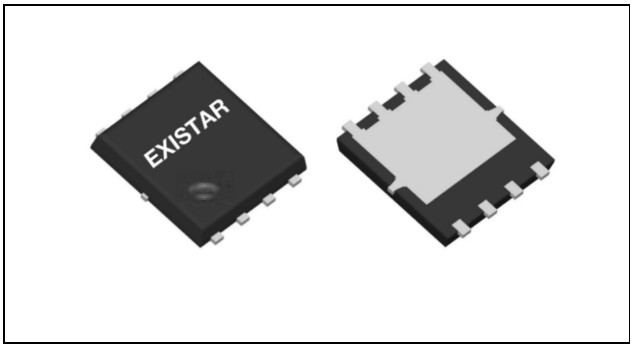
N-Channel 100V MOSFET

E100N6P0HL1

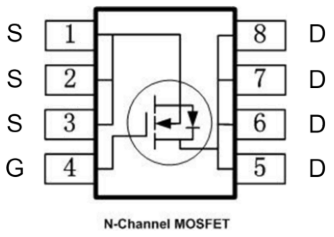
V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
100V	6 @ V_{GS} = 10V	62

PDFN5X6



Features

- Low $R_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested



Pb-free
RoHS
COMPLIANT
HALOGEN
FREE

Applications

- DC/DC conversion
- Power switch
- PD charger
- Moto driver

Package And Ordering Information

Ordering code	Package	Marking
E100N6P0HL1	PDFN5x6	E100N6P0HL1

Ordering Information

Package	Units/ Reel	Reels/ Inner Box	Units/ Inner Box
PDFN5x6	5000	1	5000

Key Performance Parameters

Parameter	Value	Unit
VDS, min @ Tj(max)	100	V
ID, pulse	248	A
RDS(ON), max @ VGS=10V	6	mΩ
Qg	56.1	nC

Absolute Maximum Ratings at Tj=25°C Unless Otherwise Noted

Parameter		Symbol	Limit	Unit
Drain-source voltage		V_{DS}	100	V
Gate-source voltage		V_{GS}	±20	
Continuous drain current	T_C=25°C	I_D	62	A
	T_C=100°C		40	
Pulsed drain current		$I_{D,pulse}$	248	
Avalanche energy, single pulse		E_{AS}	144	mJ
Power dissipation	T_C=25°C	P_D	41	W
	T_A=25°C		-	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	℃

Thermal Characteristics

Parameter		Symbol	Max.	Unit
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	3	°C/W
Thermal resistance, junction-to-ambient	Steady state	$R_{\theta JA}$	62	

Electrical Characteristics at Tj=25°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Static						
Drain to source breakdown voltage	$V_{(BR)DSS}$	100			V	V_{GS} = 0, I_D = 250 μA
Gate-source threshold voltage	$V_{GS(th)}$	1.0	1.8	2.5	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-body leakage	I_{GSS}			±100	nA	V_{DS} = 0 V, V_{GS} = ±20 V
Zero gate voltage drain current	I_{DSS}			1	μA	V_{DS} = 80 V, V_{GS} = 0 V
Drain-source on-resistance	$R_{DS(on)}$		5.3	6	mΩ	V_{GS} = 10 V, I_D = 20 A
Drain-source on-resistance	$R_{DS(on)}$		7.5	8.5	mΩ	V_{GS} = 4.5 V, I_D = 15 A

Forward transconductance	gfs		60		S	V_{DS} = 5 V, I_D = 15 A
Gate resistance	Rg		0.95		Ω	f=1MHz
Gate Charge						
Total gate charge	Qg		56.1		nC	V_{DS} = 50 V, I_D = 30 A, V_{GS} = 10 V
Gate-source charge	Qgs		9.7			
Gate-drain charge	Qgd		16.9			
Dynamic						
Turn-on delay time	$t_{d(on)}$		19.6		ns	V_{DS} = 50 V, I_D =20 A, V_{GS} = 10 V, R_{GEN} =3.3 Ω
Rise time	t_r		20.8			
Turn-off delay time	$t_{d(off)}$		18.8			
Fall time	t_f		4.8			
Input capacitance	C_{iss}		2570		pF	V_{DS} =25 V, V_{GS} = 0 V, f = 1MHz
Output capacitance	C_{oss}		1155			
Reverse transfer capacitance	C_{rss}		130			
Body Diode						
Diode forward voltage	V_{SD}			1.2	V	V_{GS} = 0 V, I_F = 20 A
Reverse recovery time	t_{rr}		47		ns	V_R= 50 V, I_S =20 A, di/dt = 100 A/μs
Reverse recovery charge	Q_{rr}		55		nC	

Electrical Characteristics Diagrams

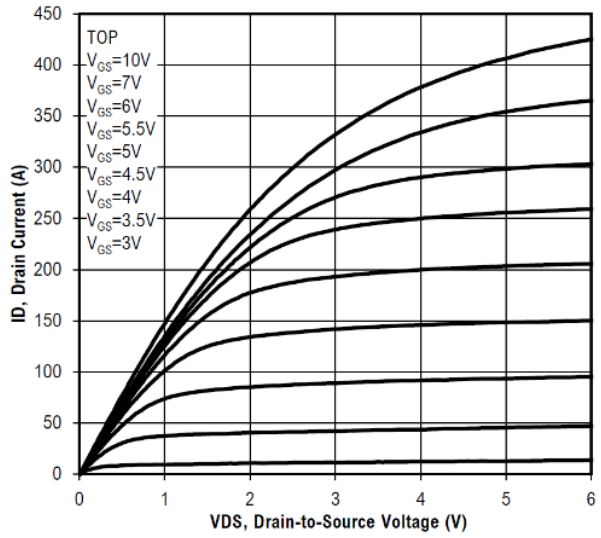


Figure 1. On-Region Characteristics

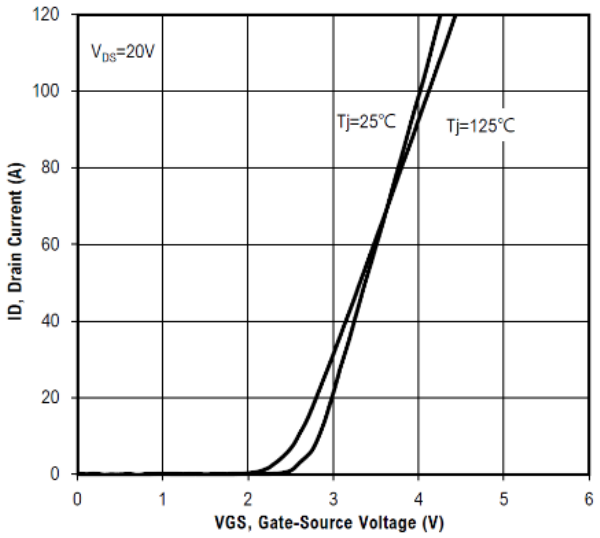


Figure 2. Transfer Characteristics

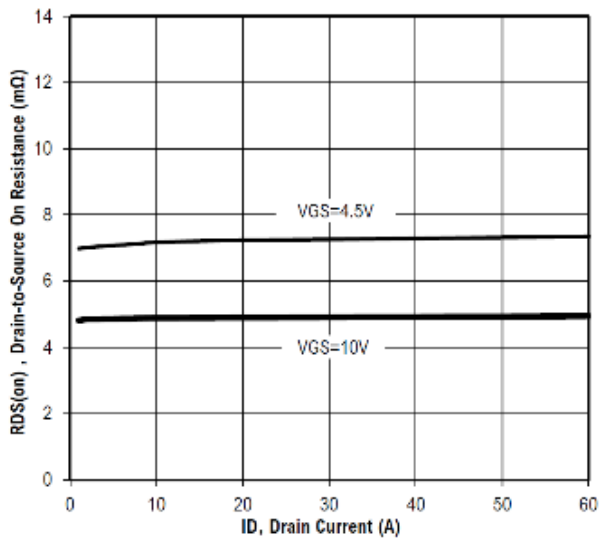


Figure 3. On-Resistance vs. Drain Current and Gate

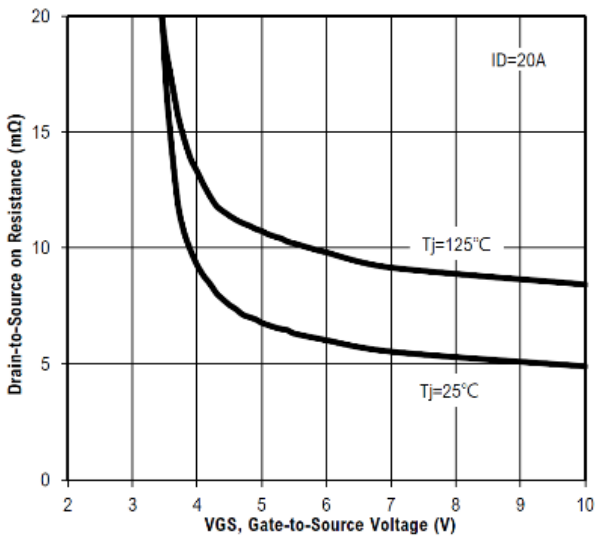


Figure 4. On-Resistance vs. Gate-Source Voltage

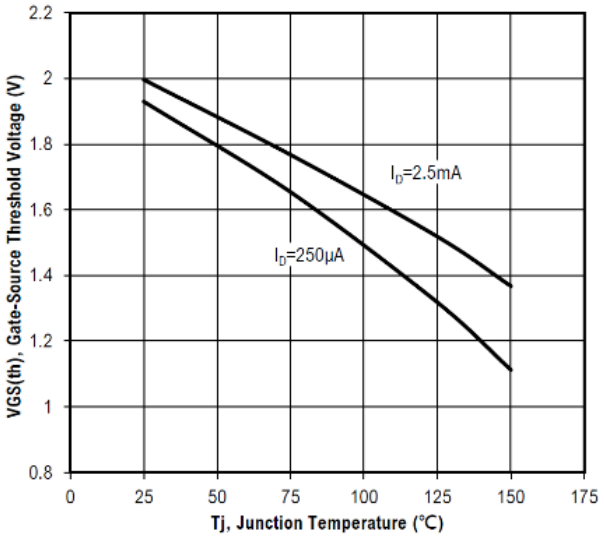


Figure 5. Gate Threshold Voltage

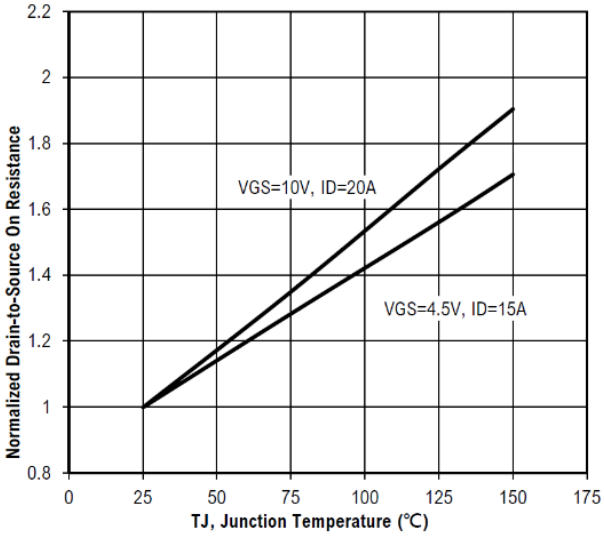


Figure 6. On-Resistance vs. Junction Temperature

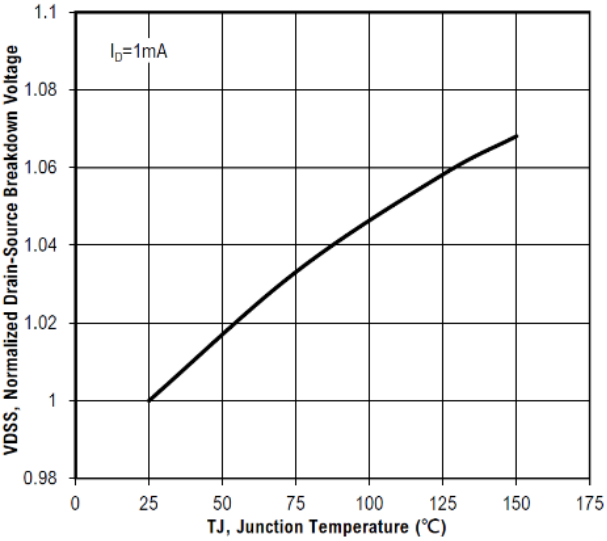


Figure 7. Drain-source breakdown voltage vs. Junction Temperature

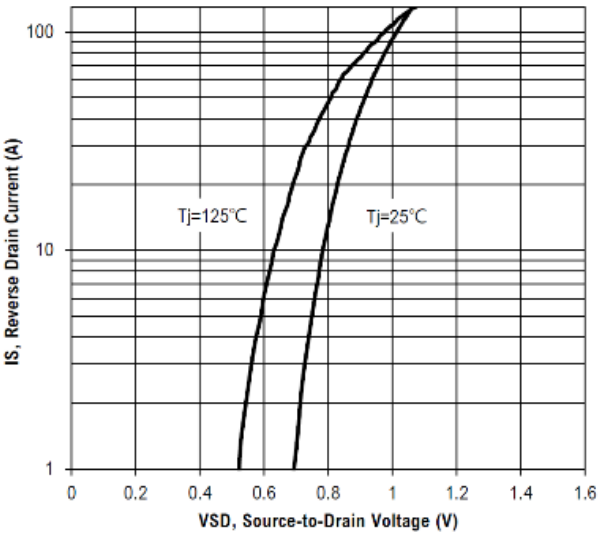


Figure 8. Body-Diode Characteristics

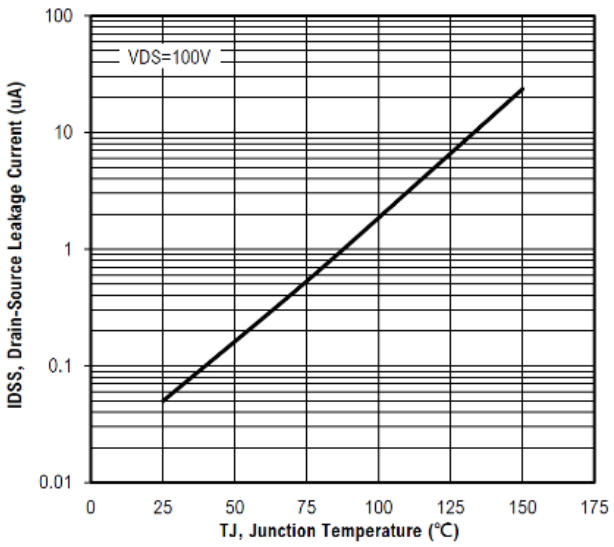


Figure 9. Zero Gate Voltage Drain Current vs. Junction Temperature

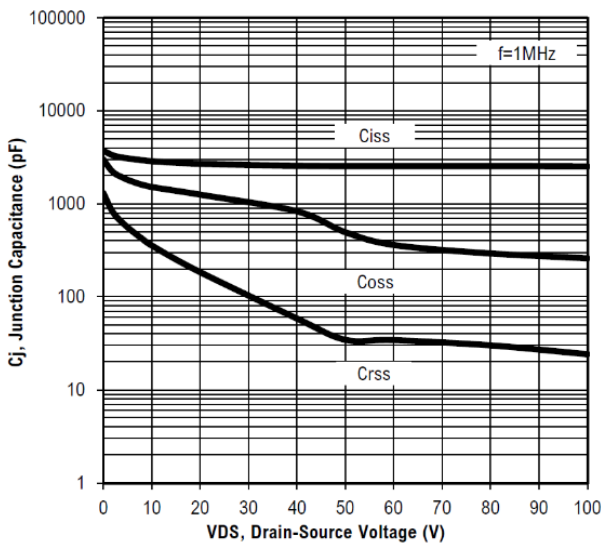


Figure 10. Capacitance vs. Drain to Source Voltage

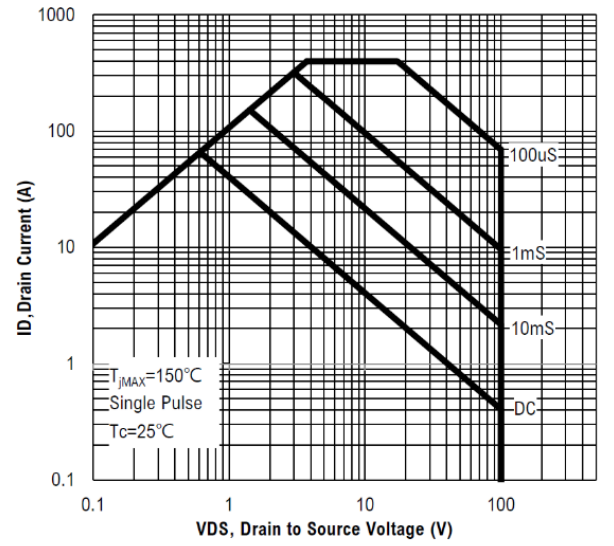


Figure 11. Maximum Forward Biased Safe Operating Area

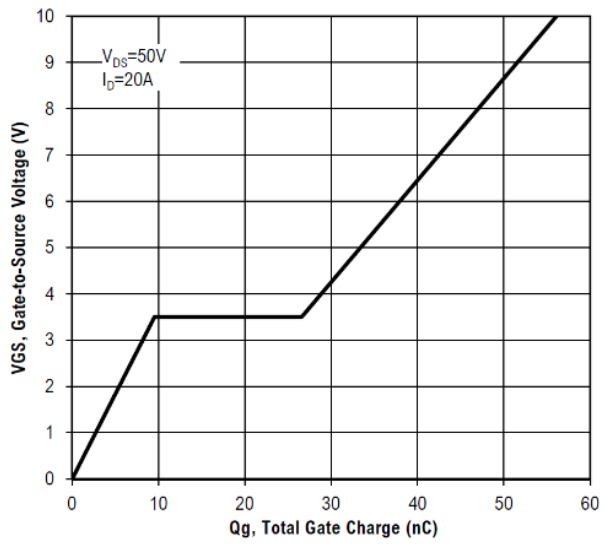


Figure 12. Gate-Charge Characteristics

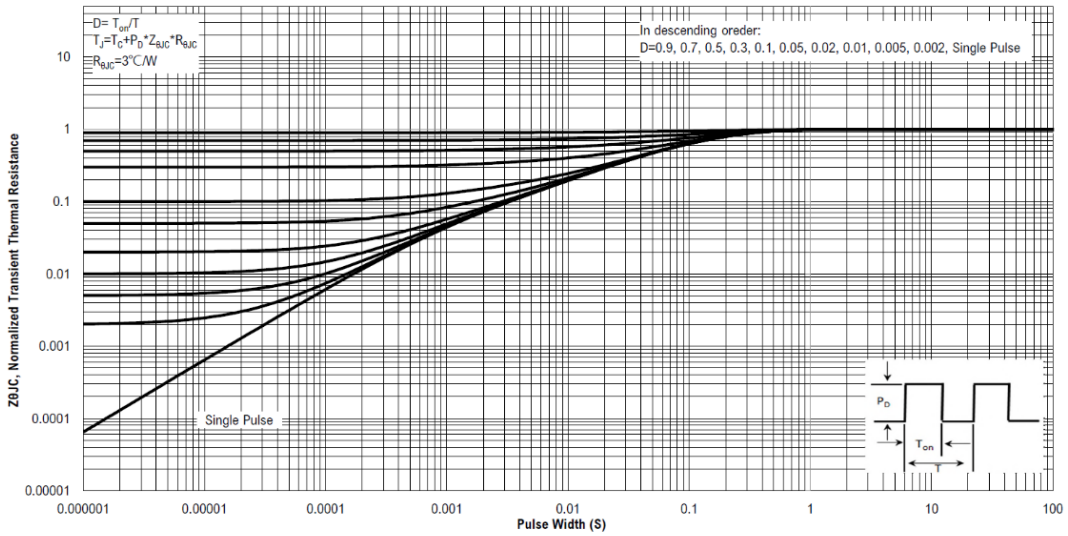


Figure 13. Transient Thermal Resistance

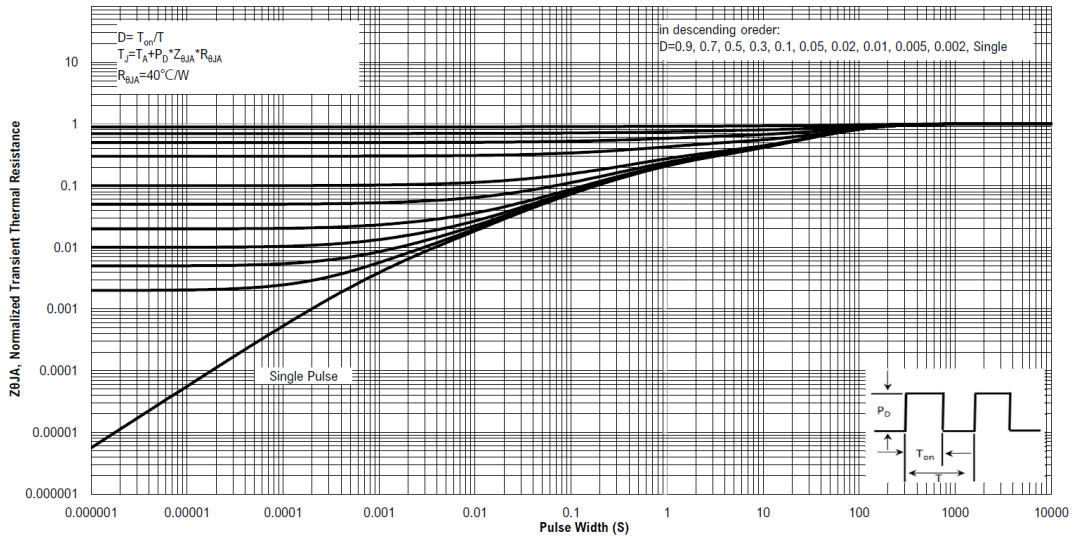
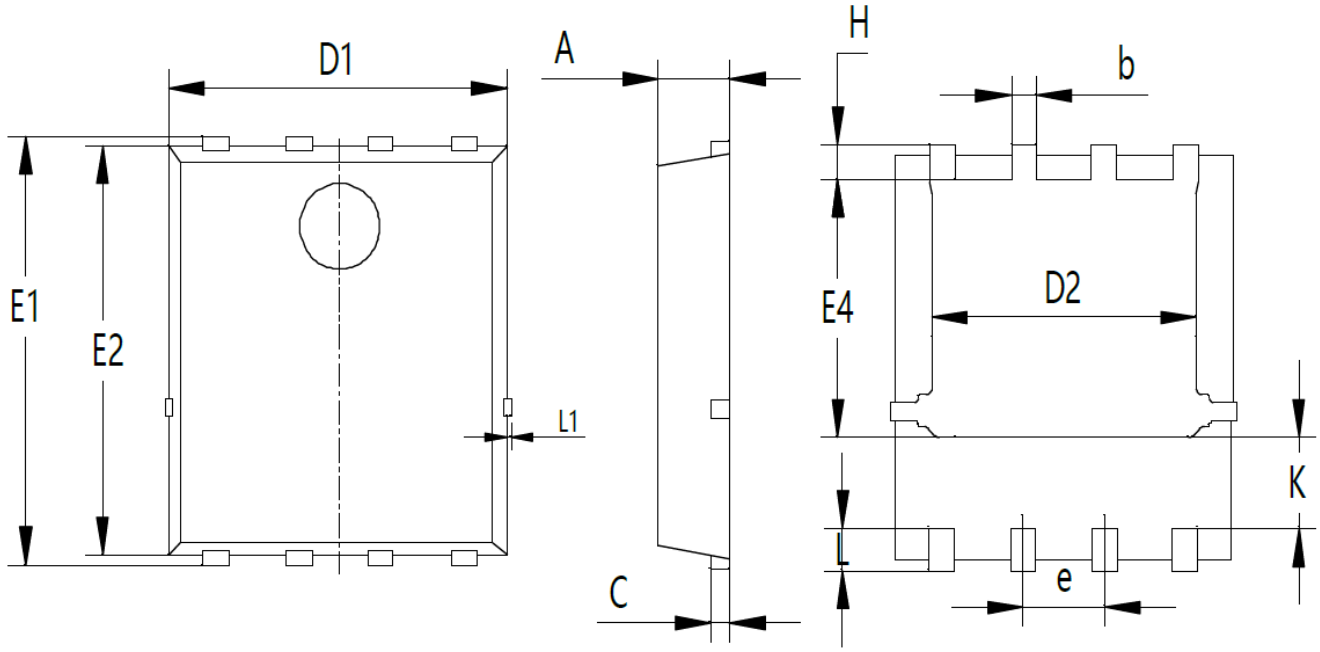


Figure 14. Transient Thermal Resistance

Package Outline Dimensions



Symbol	mm		
	Min	Nom	Max
A	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.154	0.254	0.354
D1	5.00	5.20	5.40
D2	3.80	4.10	4.25
e	1.17	1.27	1.37
E1	5.95	6.15	6.35
E2	5.66	5.86	6.06
E4	3.52	3.72	3.92
H	0.40	0.50	0.60
L	0.30	0.60	0.70
L1	0.12 REF		
K	1.15	1.30	1.45

Legal Disclaimer

The information given in this document shall be for illustrative purposes only and shall in no event be regarded as a guarantee of conditions or characteristics. Existar Technologies reserves the right to change any information herein. With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Existar Technologies or its affiliates hereby make no representation or warranty of any kind, expressed or implied, as to any information provided hereunder, including without limitation as to the accuracy, completeness or non-infringement of intellectual property rights of any third party, and they assume no liability for the consequences of use of such information. In addition, any information given in this document is subject to customer's compliance with its obligations stated herein and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Existar Technologies in customer's applications. The information contained herein is exclusively intended for technically trained staff. No license is granted by implication under any patent right, copyright, mask work right, or other intellectual property right. It is customer's sole responsibility to evaluate the suitability of the product for the intended application and the completeness of the product information given herein with respect to such application. In no event shall Existar Technologies or its affiliates be liable to any party for any direct, indirect, special, punitive, incidental or consequential damages of any nature whatsoever, including but not limited to loss of profits and loss of goodwill, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory.