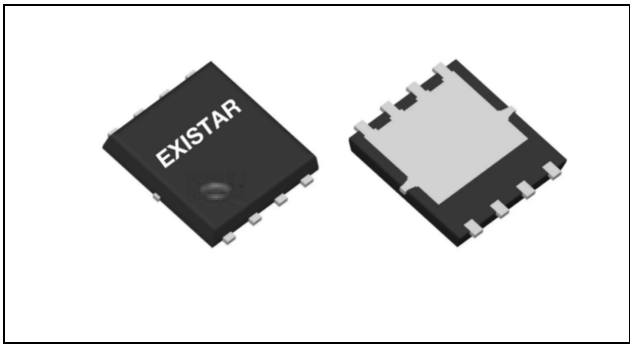
N-Channel 40V MOSFET

E040N2P5HL1

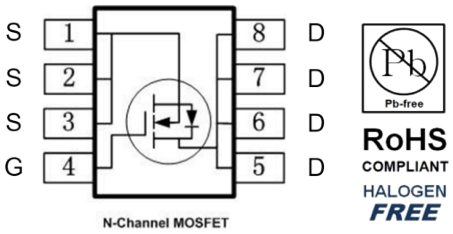
V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
40V	2.5 @ V_{GS} = 10V	105

PDFN5X6



Features

- Low $R_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested



Applications

- DC/DC conversion
- Power switch
- PD charger
- Moto driver

Package And Ordering Information

Ordering code	Package	Marking
E040N2P5HL1	PDFN5x6	E040N2P5HL1

Ordering Information

Package	Units/ Reel	Reels/ Inner Box	Units/ Inner Box
PDFN5x6	5000	1	5000

Key Performance Parameters

Parameter	Value	Unit
VDS, min @ Tj(max)	40	V
ID, pulse	435	A
RDS(ON), max @ VGS=10V	2.5	mΩ
Qg	45.5	nC

Absolute Maximum Ratings at Tj=25°C Unless Otherwise Noted

Parameter		Symbol	Limit	Unit
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	±20	
Continuous drain current	T_C=25°C	I_D	105	A
	T_C=100°C		-	
Pulsed drain current		$I_{D,pulse}$	435	
Avalanche energy, single pulse		E_{AS}	125	mJ
Power dissipation	T_C=25°C	P_D	35.7	W
	T_A=25°C		-	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to 150	℃

Thermal Characteristics

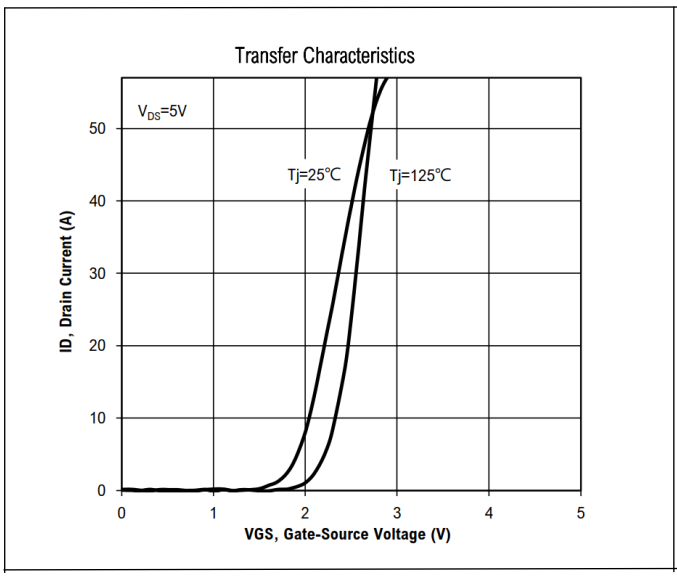
Parameter		Symbol	Max.	Unit
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	3.1	°C/W
Thermal resistance, junction-to-ambient	Steady state	$R_{\theta JA}$	62	

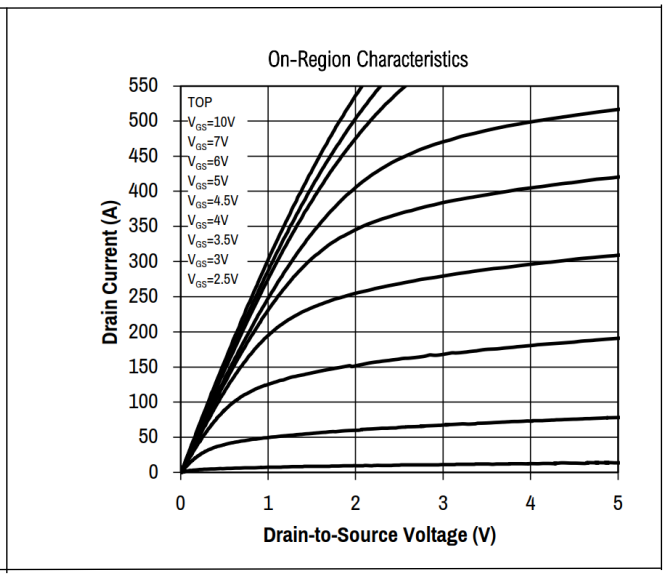
Electrical Characteristics at Tj=25°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Static						
Drain to source breakdown voltage	$V_{(BR)DSS}$	40			V	V_{GS} = 0, I_D = 250 μA
Gate-source threshold voltage	$V_{GS(th)}$	1.2		2.3	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-body leakage	I_{GSS}			±100	nA	V_{DS} = 0 V, V_{GS} = ±20 V
Zero gate voltage drain current	I_{DSS}			1	μA	V_{DS} = 32 V, V_{GS} = 0 V
Drain-source on-resistance	$R_{DS(on)}$		1.85	2.5	mΩ	V_{GS} = 10 V, I_D = 20 A
Drain-source on-resistance	$R_{DS(on)}$		2.45	3.0	mΩ	V_{GS} = 4.5 V, I_D = 15 A

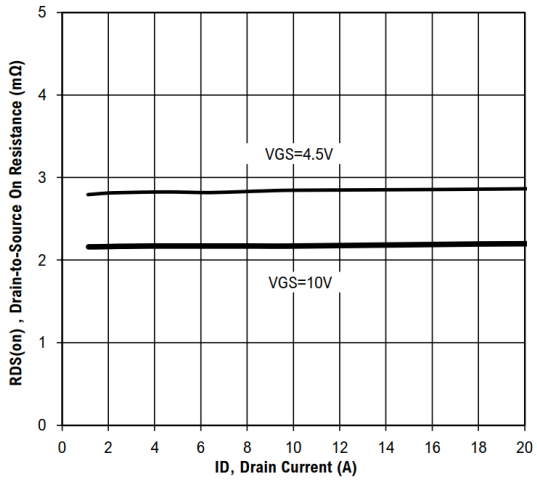
Forward transconductance	gfs		22		S	V_{DS} = 5 V, I_D = 5 A
Gate resistance	Rg		0.8		Ω	f=1MHz
Gate Charge						
Total gate charge	Qg		45.5		nC	V_{DS} = 20 V, I_D = 20 A, V_{GS} = 10 V
Gate-source charge	Qgs		9			
Gate-drain charge	Qgd		6.6			
Dynamic						
Turn-on delay time	$t_{d(on)}$		18.6		ns	V_{DS} =20 V, I_D =20 A, V_{GS} = 10 V, R_{GEN} = 3.3 Ω
Rise time	t_r		45.8			
Turn-off delay time	$t_{d(off)}$		16.6			
Fall time	t_f		7.8			
Input capacitance	C_{iss}		2940		pF	V_{DS} =20 V, V_{GS} = 0 V, f = 1MHz
Output capacitance	C_{oss}		628			
Reverse transfer capacitance	C_{rss}		34			
Body Diode						
Diode forward voltage	V_{SD}			1.2	V	V_{GS} = 0 V, I_F = 20 A
Reverse recovery time	t_{rr}		24		ns	V_R= 20 V, I_S =20 A, di/dt = 100 A/μs
Reverse recovery charge	Q_{rr}		16		nC	

Electrical Characteristics Diagrams

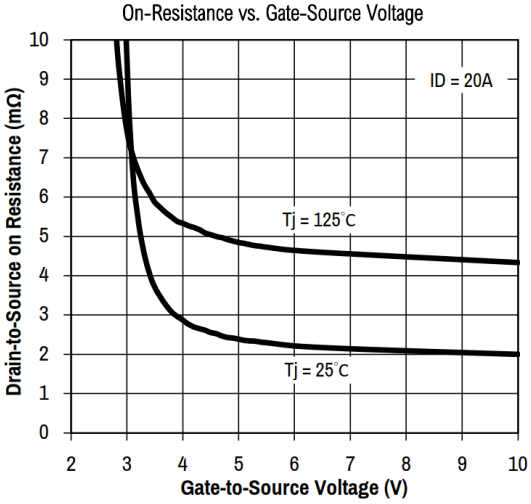




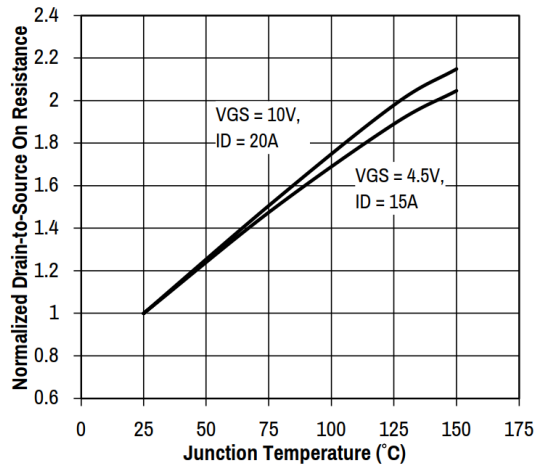
On-Resistance vs. Drain Current and Gate



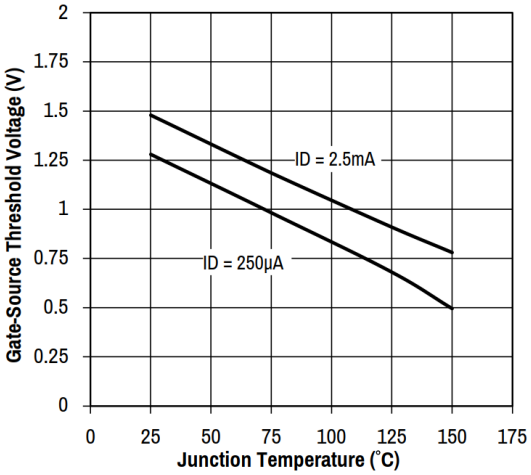
On-Resistance vs. Gate-Source Voltage



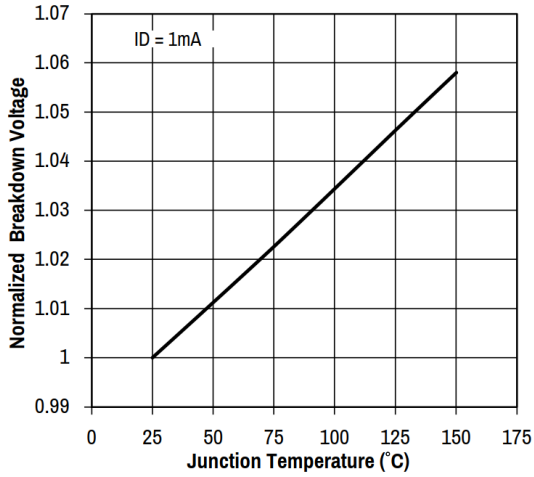
On-Resistance vs. Junction Temperature



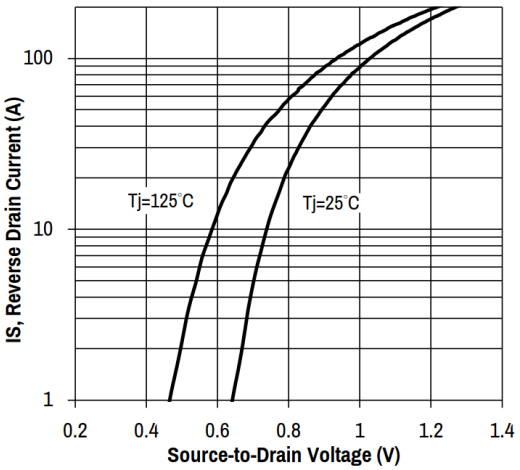
Gate Threshold Voltage



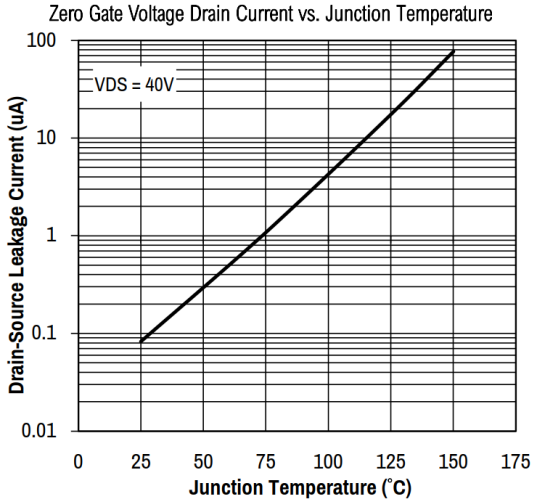
Drain-source breakdown voltage vs. Junction Temperature



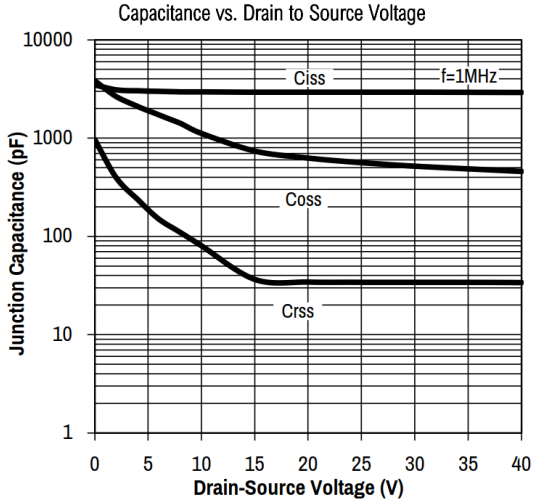
Body-Diode Characteristics



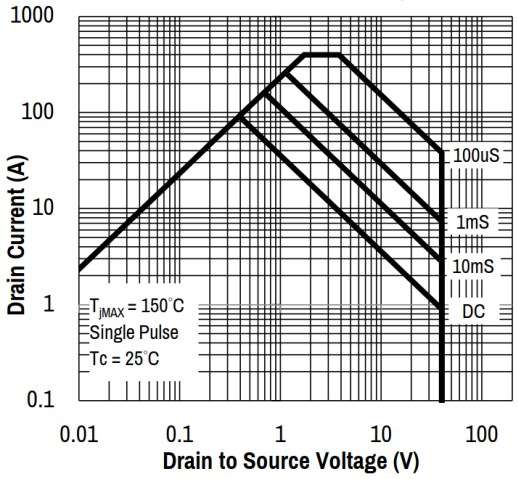
Zero Gate Voltage Drain Current vs. Junction Temperature



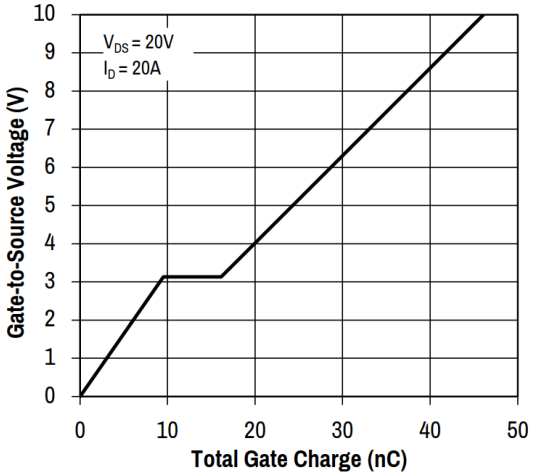
Capacitance vs. Drain to Source Voltage



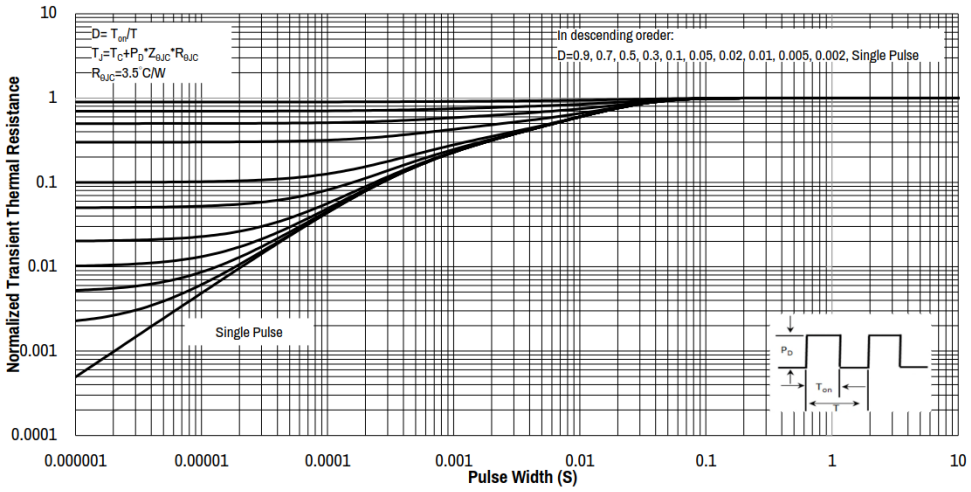
Maximum Forward Biased Safe Operating Area



Gate-Charge Characteristics



Transient Thermal Resistance



Test circuits and waveforms

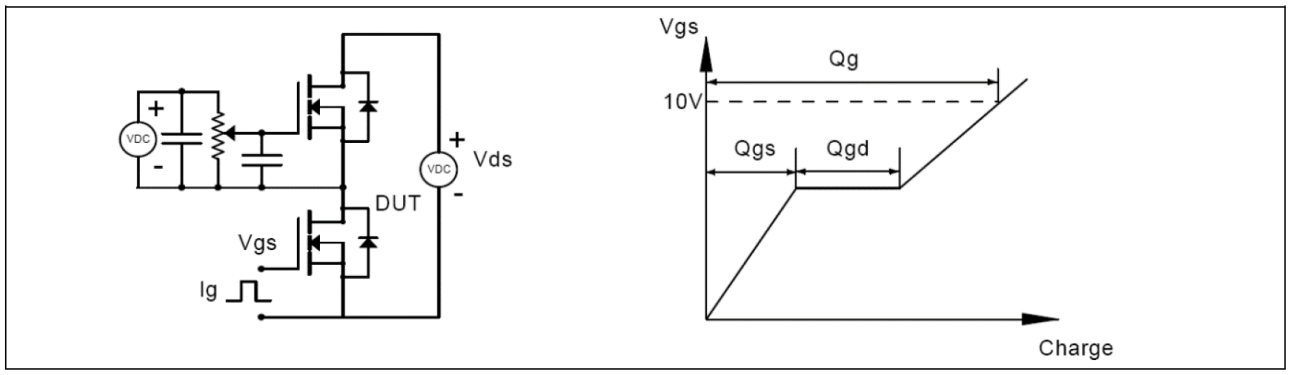


Figure 1. Gate charge test circuit & waveform

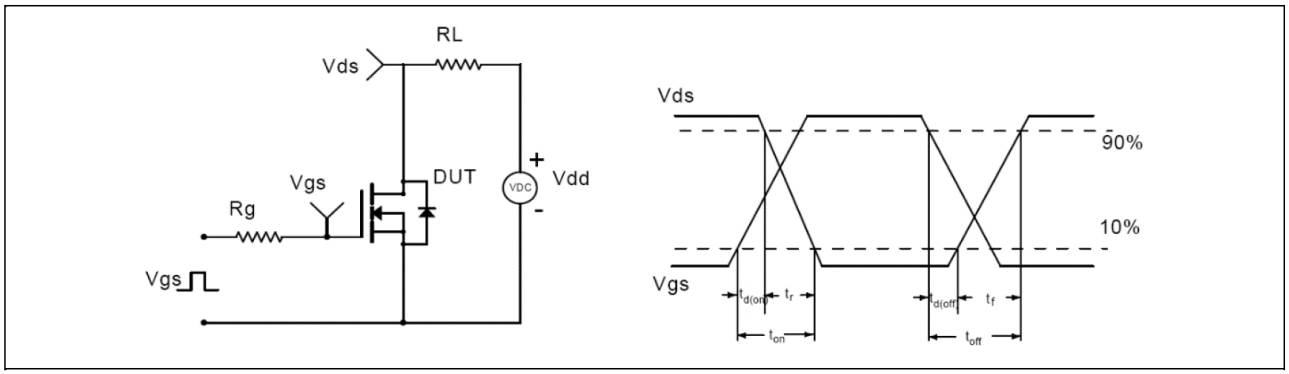


Figure 2. Switching time test circuit & waveforms

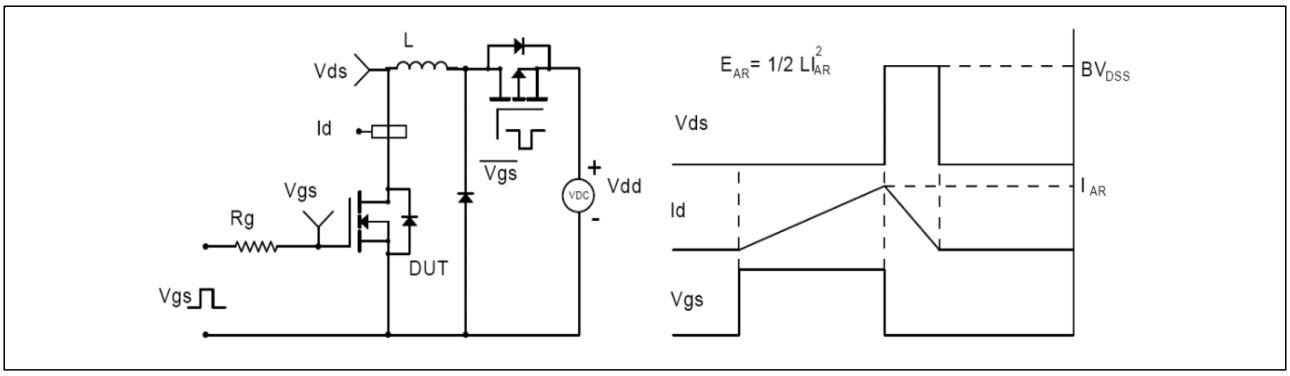


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

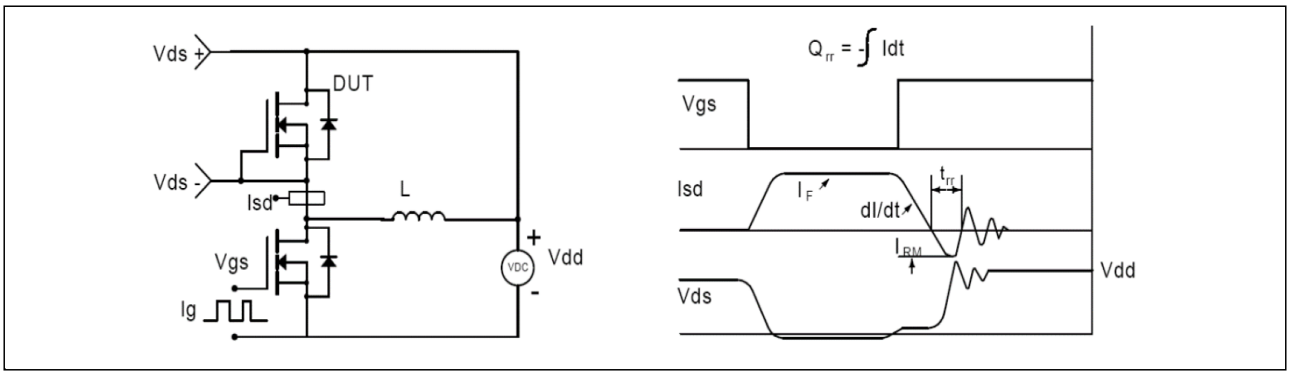
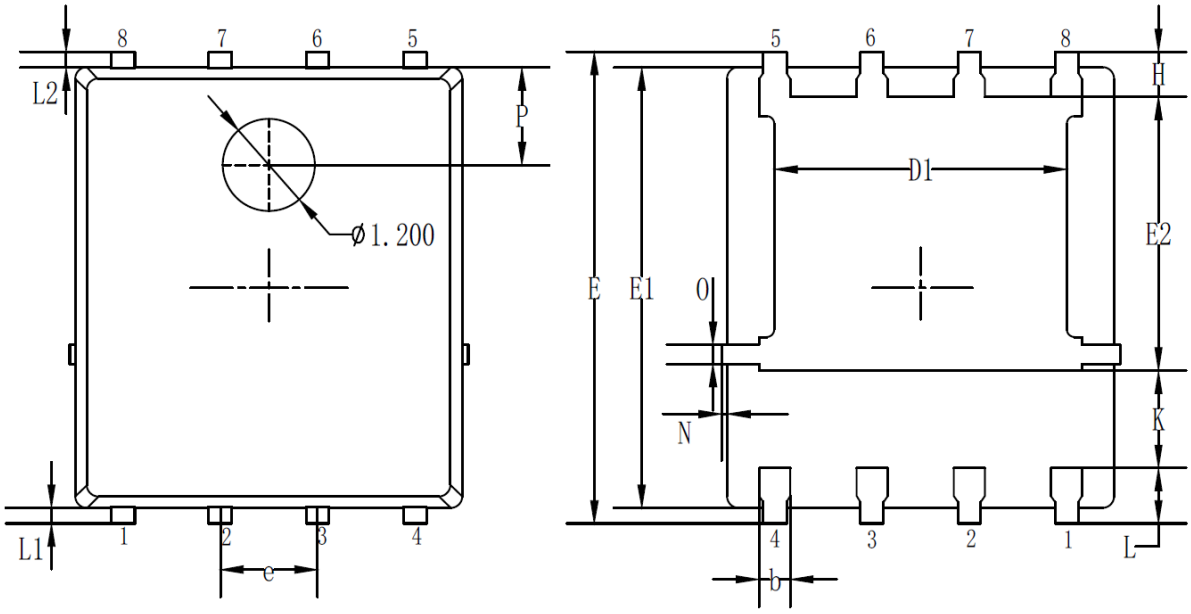
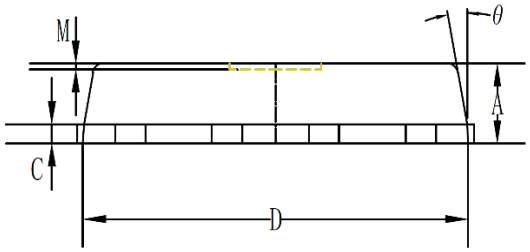


Figure 4. Diode reverse recovery test circuit & waveforms

Package Outline Dimensions





Symbols	Millimeters		
	MIN.	NOM.	MAX.
A	0.90	1.05	1.20
b	0.35	0.40	0.50
C	0.20	0.25	0.35
D	4.90	5.05	5.20
D1	3.72	3.82	3.92
E	0.60	6.15	6.30
E1	5.60	5.75	5.90
E2	3.47	3.57	3.67
e	1.27 BSC.		
H	0.48	0.58	0.68
K	1.17	1.27	1.37
L	0.64	0.74	0.84
L1/L2	0.20 REF.		
θ	8°	10°	12°
M	0.08 REF.		
N	0	-	0.15
O	0.25 REF.		
P	1.28 REF.		

Legal Disclaimer

The information given in this document shall be for illustrative purposes only and shall in no event be regarded as a guarantee of conditions or characteristics. Existar Technologies reserves the right to change any information herein. With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Existar Technologies or its affiliates hereby make no representation or warranty of any kind, expressed or implied, as to any information provided hereunder, including without limitation as to the accuracy, completeness or non-infringement of intellectual property rights of any third party, and they assume no liability for the consequences of use of such information. In addition, any information given in this document is subject to customer's compliance with its obligations stated herein and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Existar Technologies in customer's applications. The information contained herein is exclusively intended for technically trained staff. No license is granted by implication under any patent right, copyright, mask work right, or other intellectual property right. It is customer's sole responsibility to evaluate the suitability of the product for the intended application and the completeness of the product information given herein with respect to such application. In no event shall Existar Technologies or its affiliates be liable to any party for any direct, indirect, special, punitive, incidental or consequential damages of any nature whatsoever, including but not limited to loss of profits and loss of goodwill, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory.