



PSMN1R0-30YLC

N-channel 30 V 1.15 mΩ logic level MOSFET in LPAK using NextPower technology

7 June 2024

Product data sheet

1. General description

Logic level enhancement mode N-channel MOSFET in LPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads
- Ultra low R_{ds(on)} and low parasitic inductance

3. Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	30	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	-	100	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	272	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; Fig. 12		-	1.1	1.4	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12		-	0.85	1.15	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 15 V; V _{GS} = 4.5 V; Fig. 14 ; Fig. 15		-	14.6	26	nC
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 15 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15		-	103.5	145	nC
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 100 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 4		-	-	259	mJ

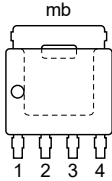
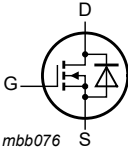
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
Q _r	recovered charge	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 15 V	-	67	-	nC

[1] Continuous current is limited by package.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R0-30YLC	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R0-30YLC	1C030L

8. Limiting values

Table 5. Limiting values

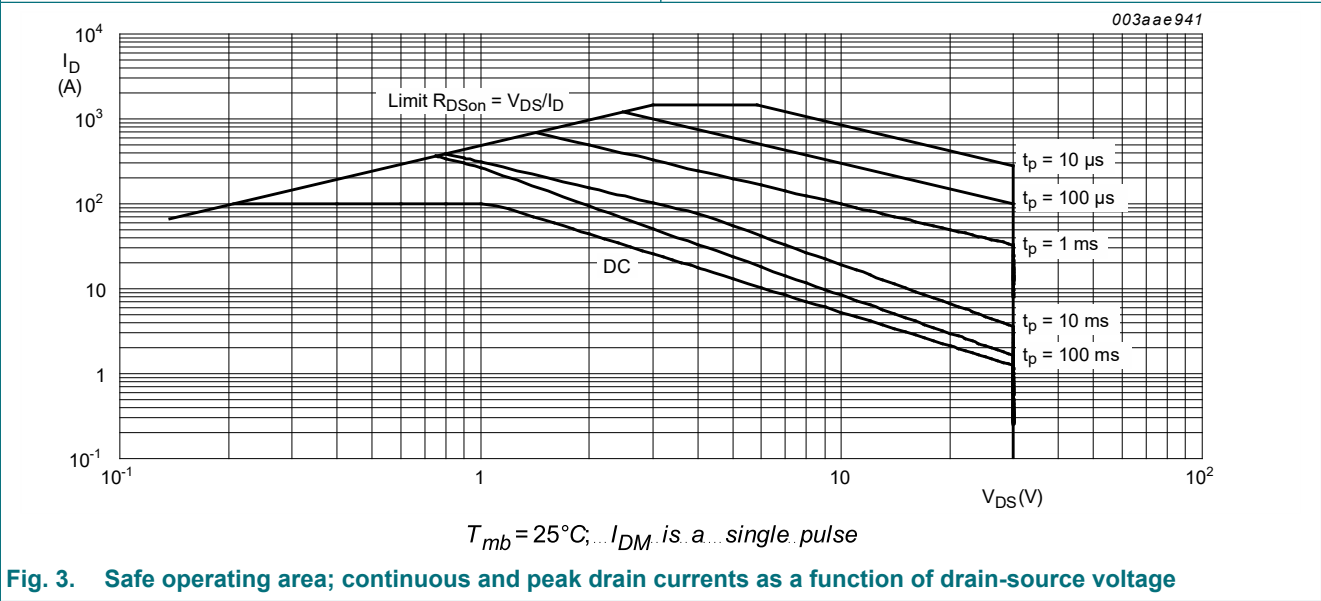
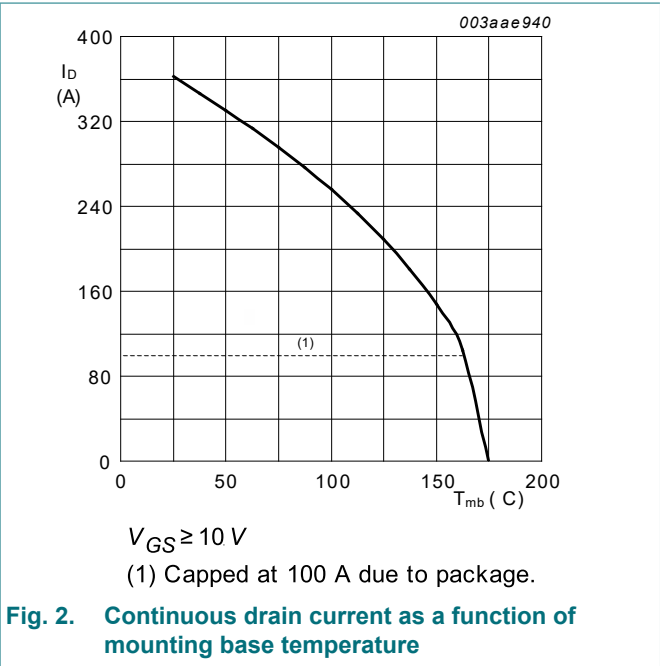
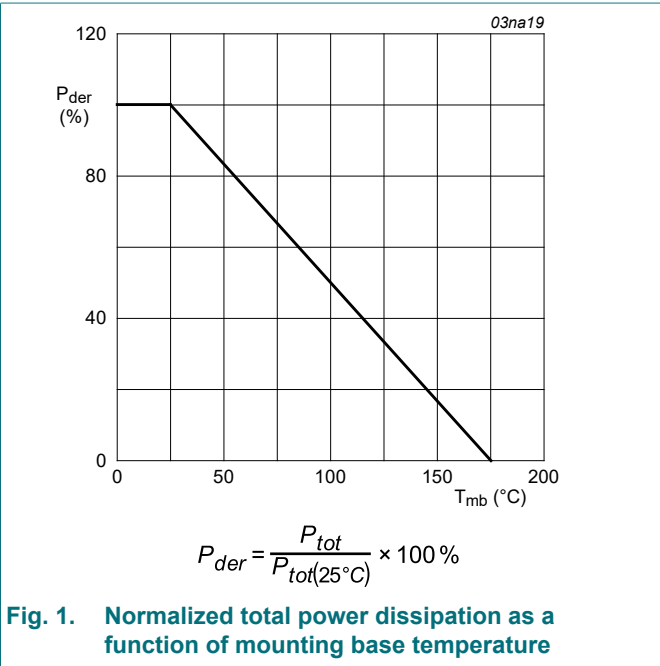
In accordance with the Absolute Maximum Rating System (IEC 60134).

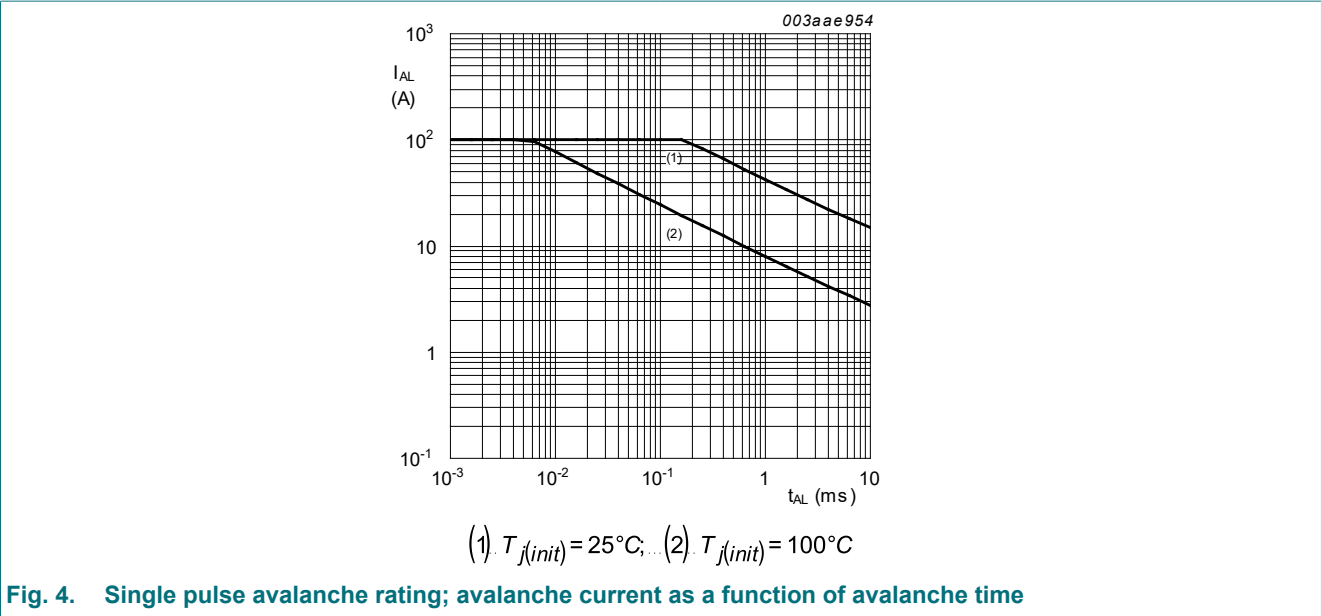
Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	30	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	30	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	272	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	100	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	[1]	100	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3	-	1450	A
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C

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Symbol	Parameter	Conditions		Min	Max	Unit
T _{slid(M)}	peak soldering temperature			-	260	°C
V _{ESD}	electrostatic discharge voltage	machine model according to JEDEC JESD22-A115		960	-	V
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[1]	-	100	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	1450	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 100 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 4		-	259	mJ

[1] Continuous current is limited by package.

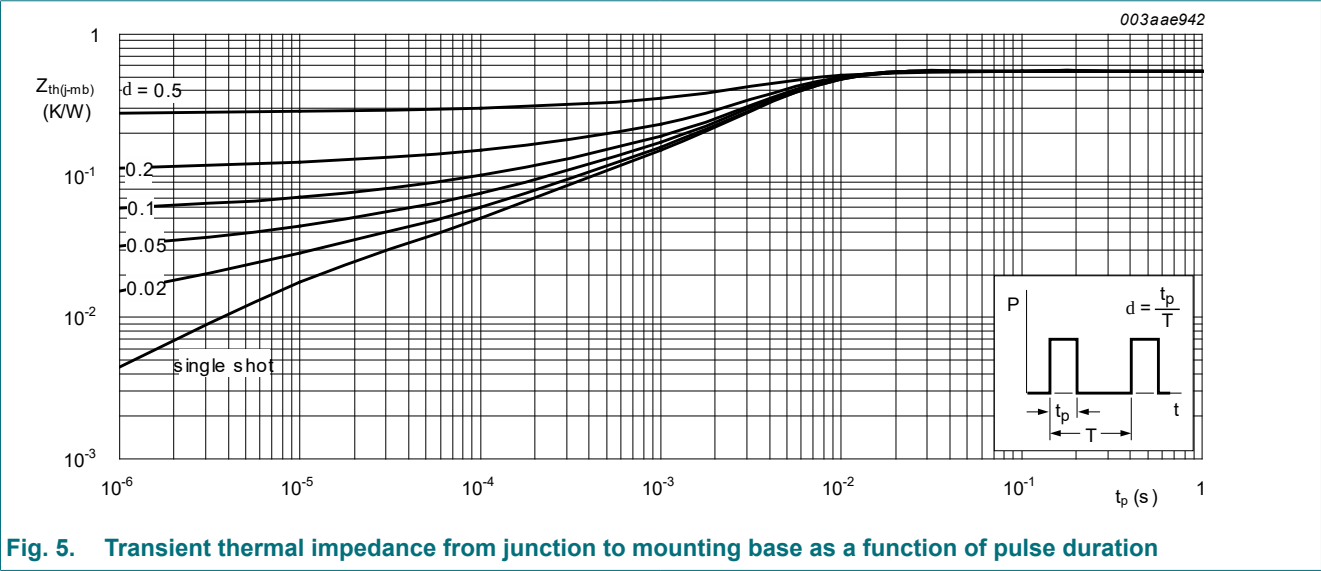




9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.45	0.55	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25^{\circ}\text{C}$	30	-	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = -55^{\circ}\text{C}$	27	-	-	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS}=V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 10	1.05	1.41	1.95	V
		$I_D = 10 \text{ mA}$; $V_{DS}=V_{GS}$; $T_j = 150 \text{ }^\circ\text{C}$; Fig. 11	0.5	-	-	V
		$I_D = 1 \text{ mA}$; $V_{DS}=V_{GS}$; $T_j = -55 \text{ }^\circ\text{C}$; Fig. 11	-	-	2.25	V
I_{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 30 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 150 \text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -16 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}$; $I_D = 25 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 12	-	1.1	1.4	mΩ
		$V_{GS} = 4.5 \text{ V}$; $I_D = 25 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$; Fig. 12 ; Fig. 13	-	-	2.4	mΩ
		$V_{GS} = 10 \text{ V}$; $I_D = 25 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 12	-	0.85	1.15	mΩ
		$V_{GS} = 10 \text{ V}$; $I_D = 25 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$; Fig. 12 ; Fig. 13	-	-	1.85	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	1.1	2.2	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 10 \text{ V}$; Fig. 14 ; Fig. 15	-	103.5	145	nC
		$I_D = 25 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 4.5 \text{ V}$; Fig. 14 ; Fig. 15	-	50	70	nC
		$I_D = 0 \text{ A}$; $V_{DS} = 0 \text{ V}$; $V_{GS} = 10 \text{ V}$; Fig. 15	-	96.5	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 4.5 \text{ V}$; Fig. 14 ; Fig. 15	-	12.9	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	10.1	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	2.8	-	nC
Q_{GD}	gate-drain charge		-	14.6	26	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}$; $V_{DS} = 15 \text{ V}$; Fig. 14	-	2.2	-	V
C_{iss}	input capacitance	$V_{DS} = 15 \text{ V}$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 16	3322	6645	9968	pF
C_{oss}	output capacitance		605	1210	1815	pF
C_{rss}	reverse transfer capacitance		240	481	842	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 \text{ V}$; $R_L = 0.6 \text{ } \Omega$; $V_{GS} = 4.5 \text{ V}$; $R_{G(ext)} = 4.7 \text{ } \Omega$	-	44	-	ns
t_r	rise time		-	77	-	ns
$t_{d(off)}$	turn-off delay time		-	108	-	ns
t_f	fall time		-	60	-	ns
Q_{oss}	output charge	$V_{GS} = 0 \text{ V}$; $V_{DS} = 15 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$	-	35.2	-	nC
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 17	-	0.8	1.1	V
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}$; $dI_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 15 \text{ V}$	-	45	-	ns
Q_r	recovered charge		-	67	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_a	reverse recovery rise time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 15\text{ V}$; Fig. 18		-	28.5	-	ns
t_b	reverse recovery fall time			-	16.5	-	ns

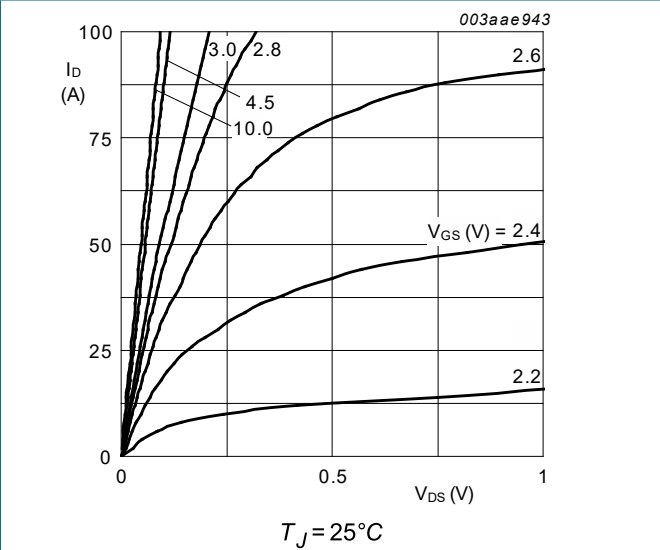


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

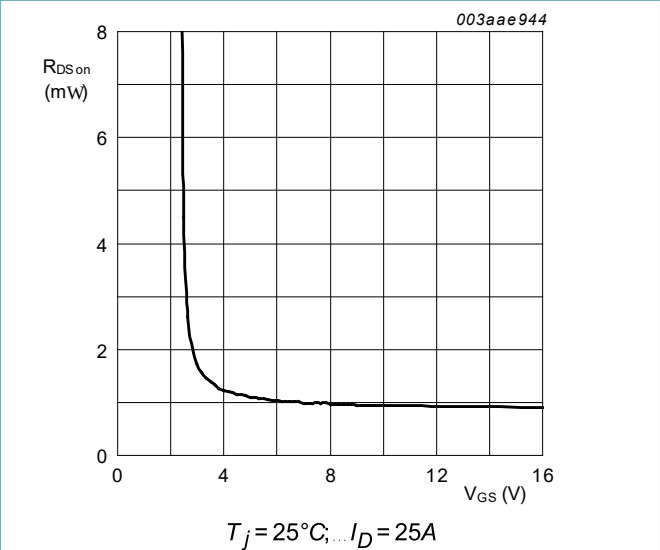


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

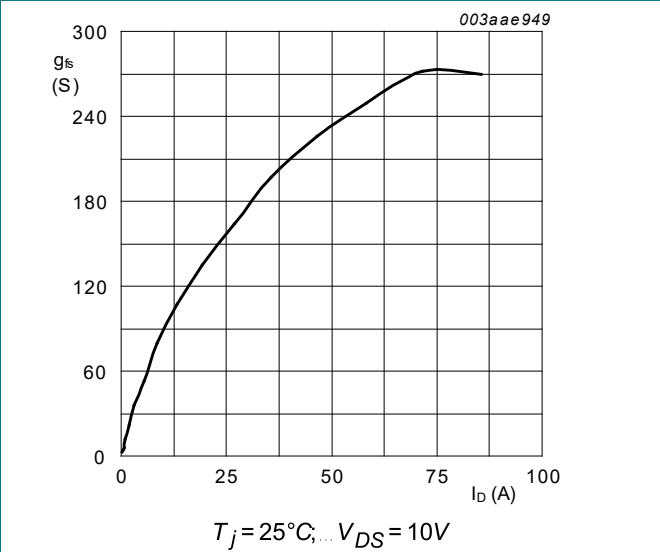


Fig. 8. Forward transconductance as a function of drain current; typical values

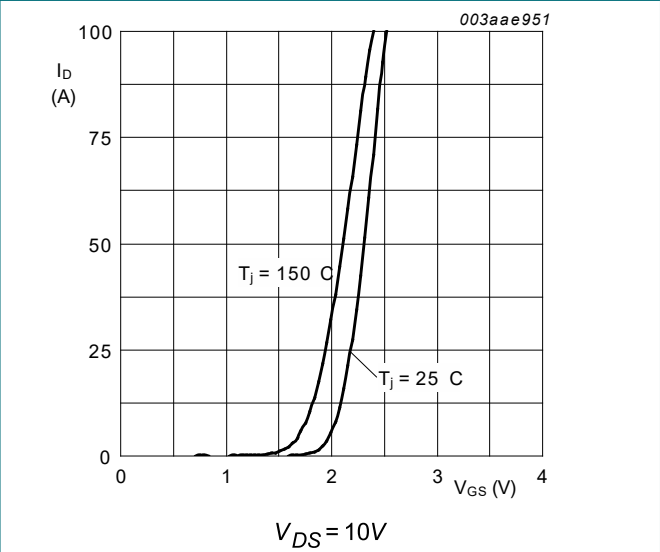


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

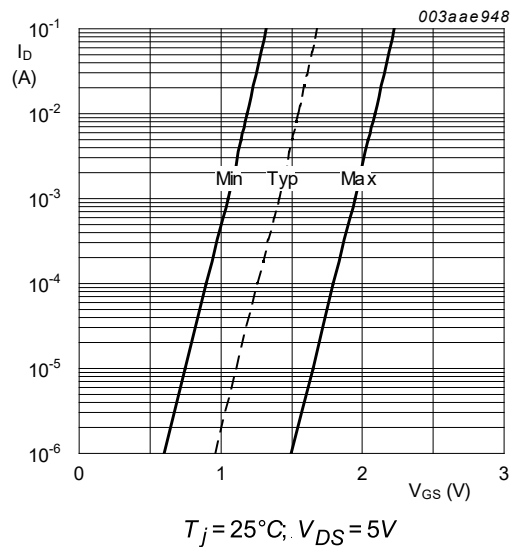


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

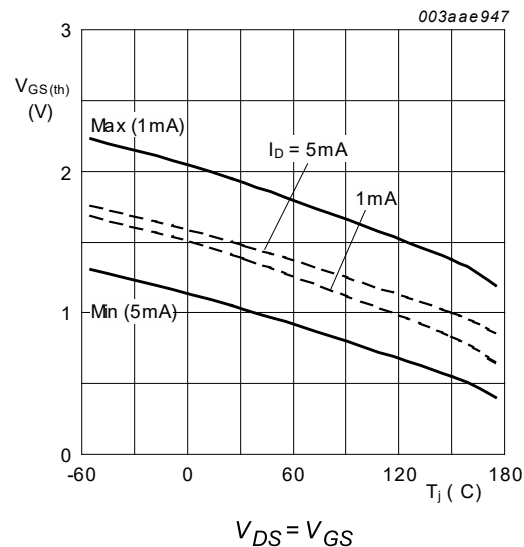


Fig. 11. Gate-source threshold voltage as a function of junction temperature

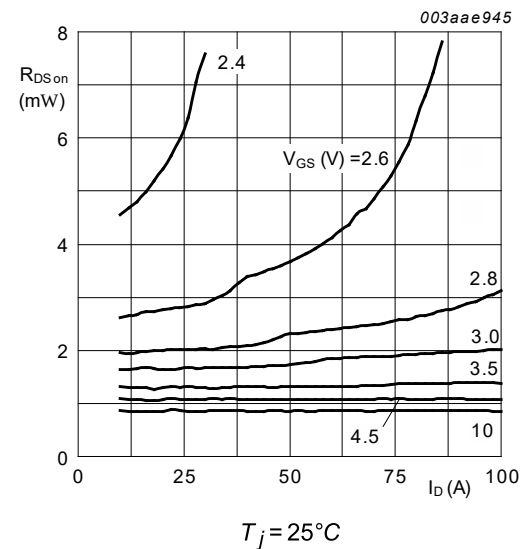


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

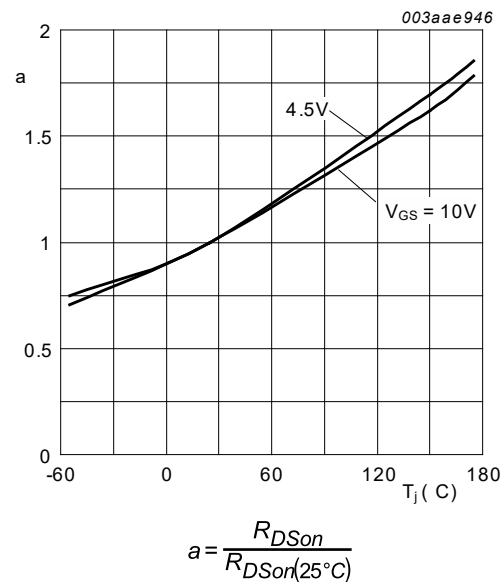


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

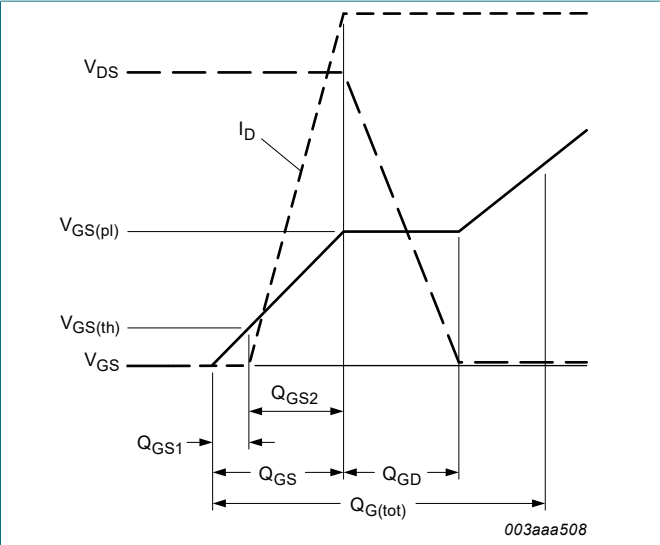


Fig. 14. Gate charge waveform definitions

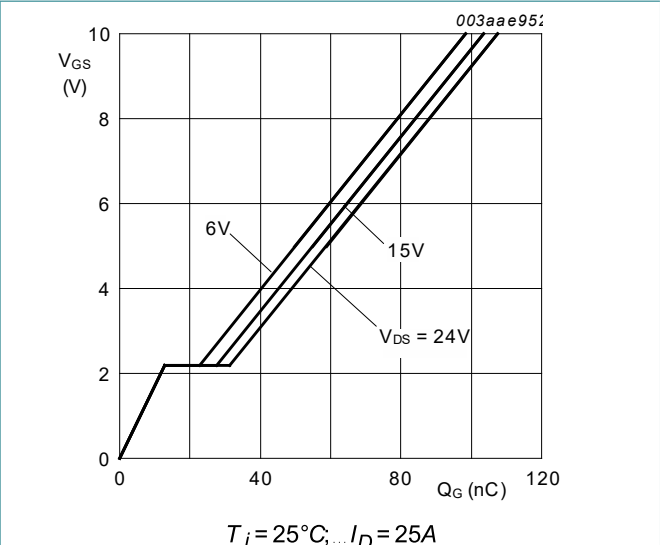


Fig. 15. Gate-source voltage as a function of gate charge; typical values

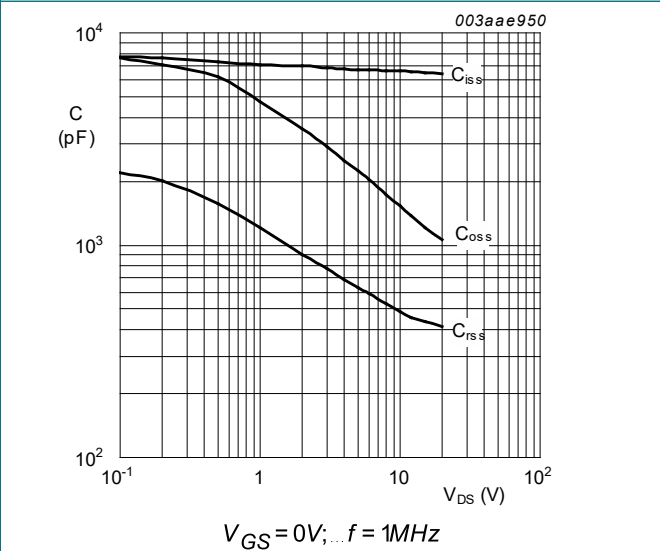


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

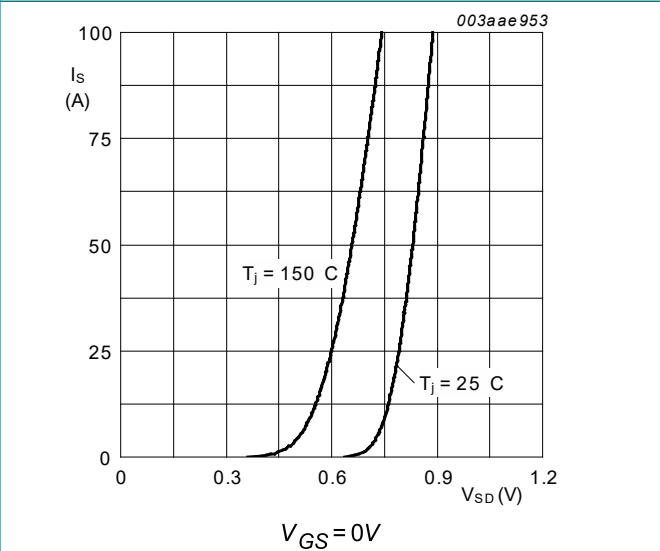
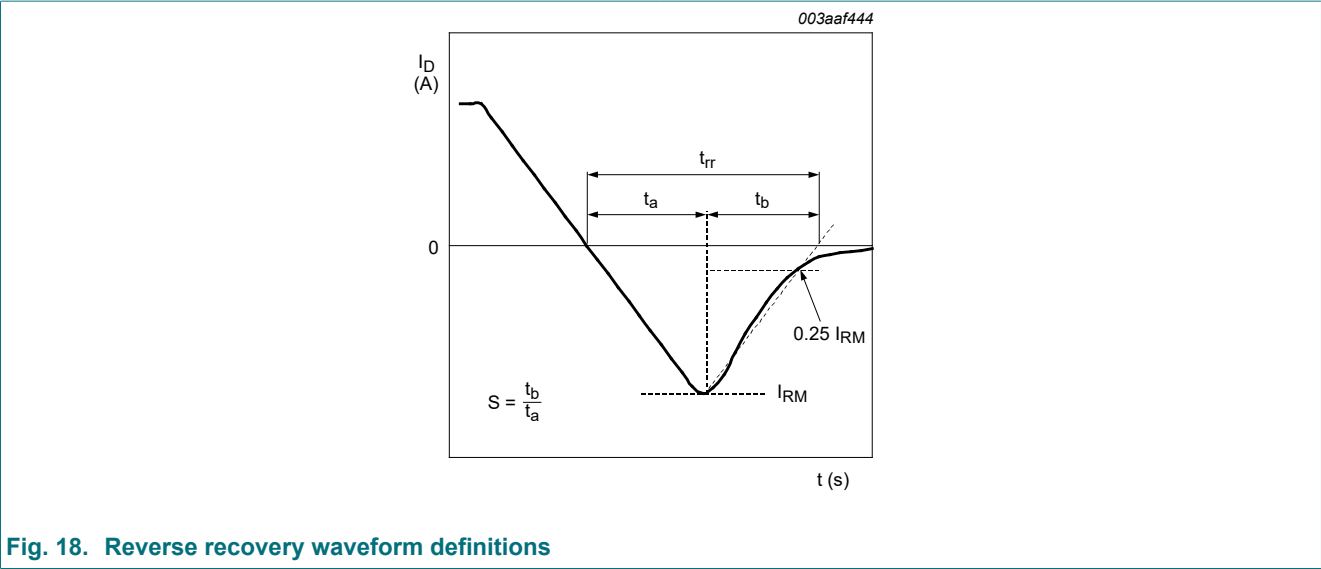


Fig. 17. Source current as a function of source-drain voltage; typical values



11. Package outline

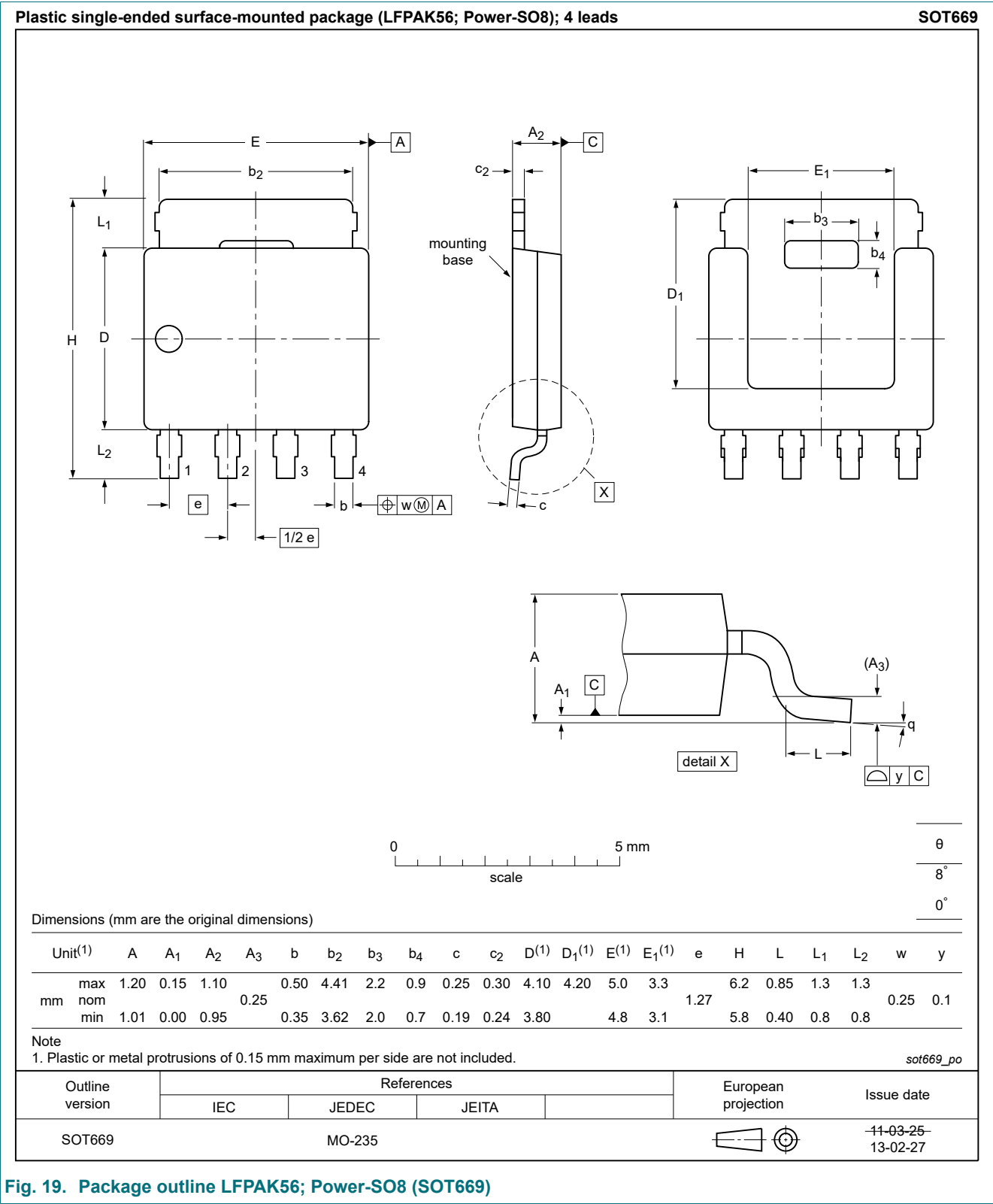


Fig. 19. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering

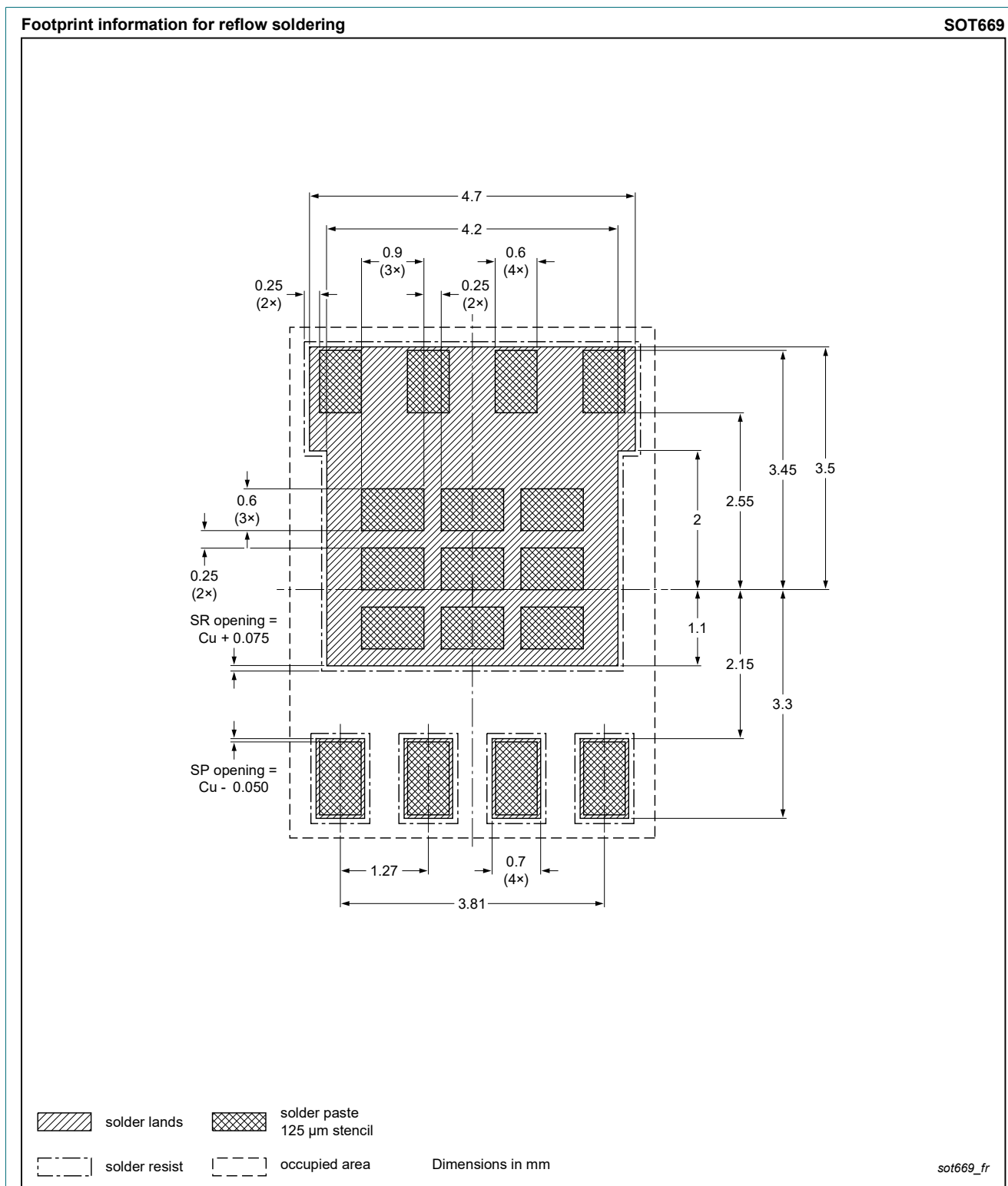
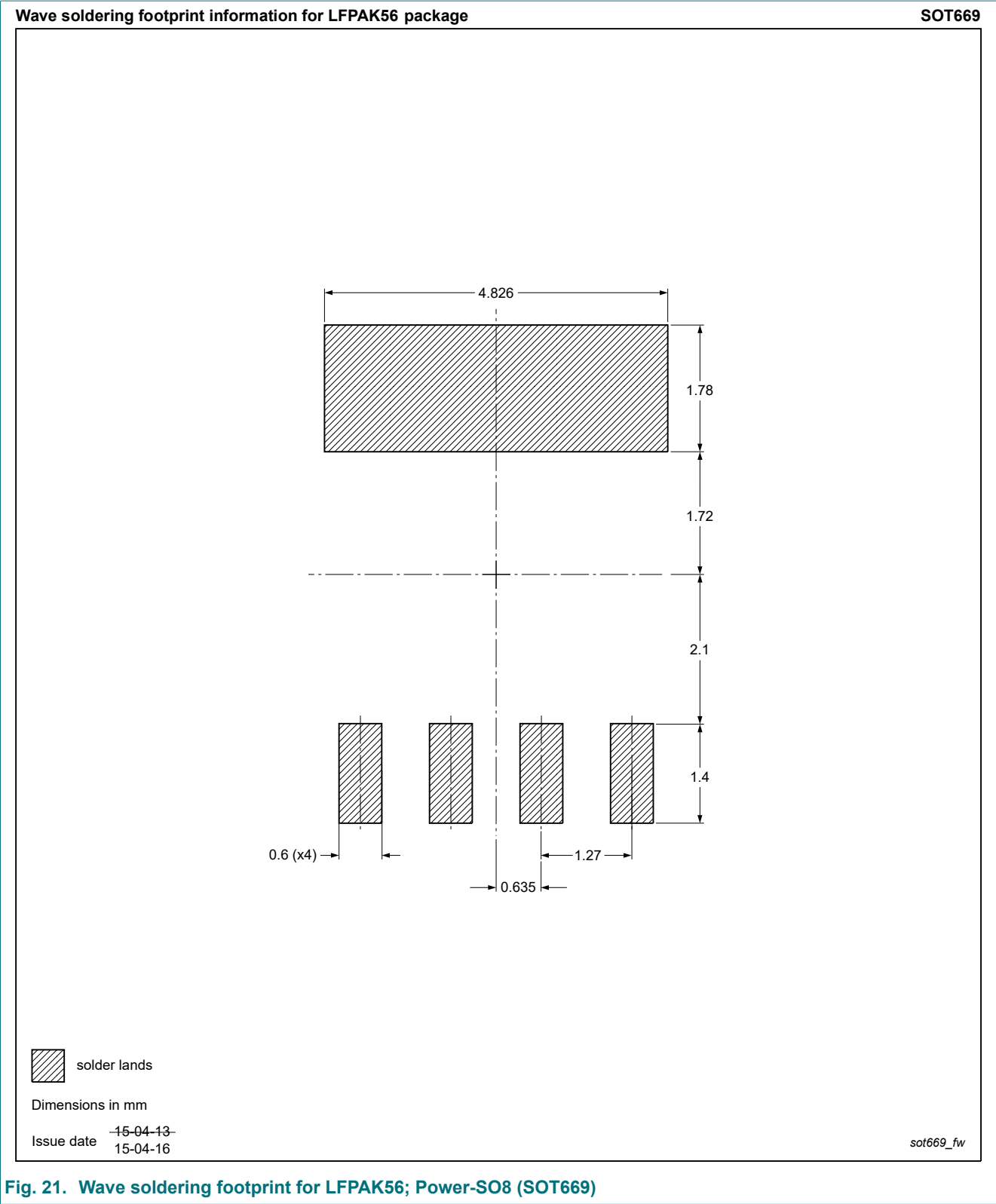


Fig. 20. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)



13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 7 June 2024