74HC74; 74HCT74

Dual D-type flip-flop with set and reset; positive edge-trigger

Rev. 9 — 2 April 2024 Product data sheet

1. General description

The 74HC74 and 74HCT74 are dual positive edge triggered D-type flip-flop. They have individual data (nD), clock (nCP), set (n$\overline{SD}$) and reset (n$\overline{RD}$) inputs, and complementary nQ and n$\overline{Q}$ outputs. Data at the nD-input, that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition, is stored in the flip-flop and appears at the nQ output. Schmitt-trigger action in the clock input, makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Input levels:
  - For 74HC74: CMOS level
  - For 74HCT74: TTL level
- Symmetrical output impedance
- High noise immunity
- Balanced propagation delays
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC74D 74HCT74D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC74PW 74HCT74PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HC74BQ 74HCT74BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

nexperia

Type number	Package			
	Temperature range	Name	Description	Version
74HC74BZ 74HCT74BZ	-40 °C to +125 °C	DHXQFN14	plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 14 terminals; 0.4 mm pitch; body 2 mm × 2 mm × 0.48 mm	SOT8014-1

4. Functional diagram

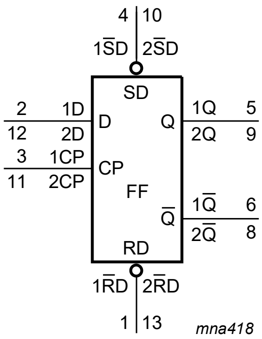


Fig. 1. Logic symbol

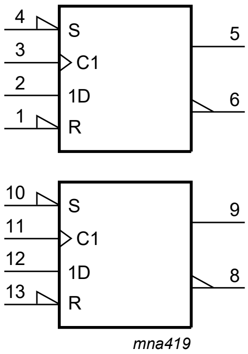


Fig. 2. IEC logic symbol

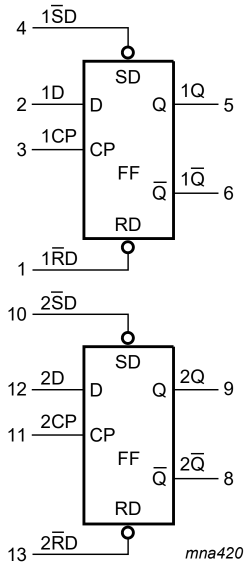


Fig. 3. Functional diagram

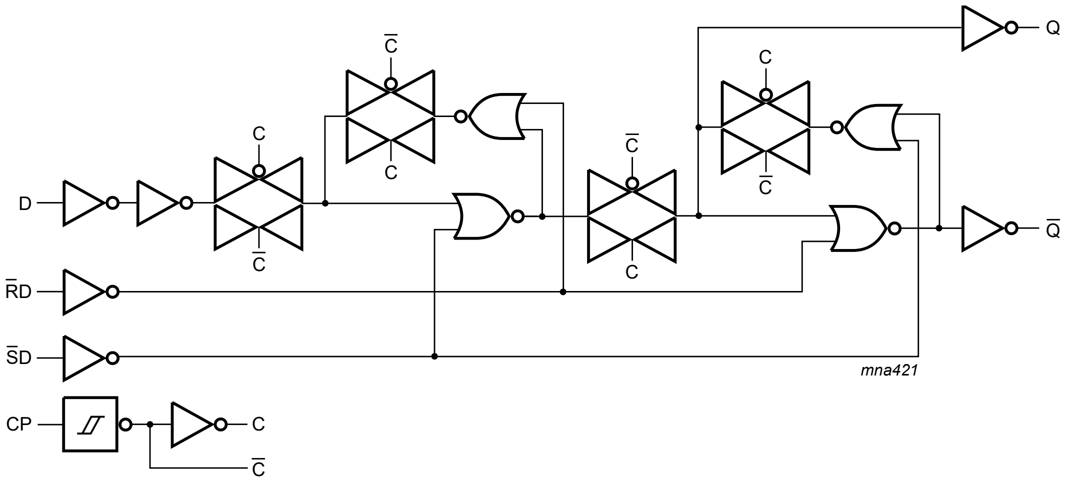
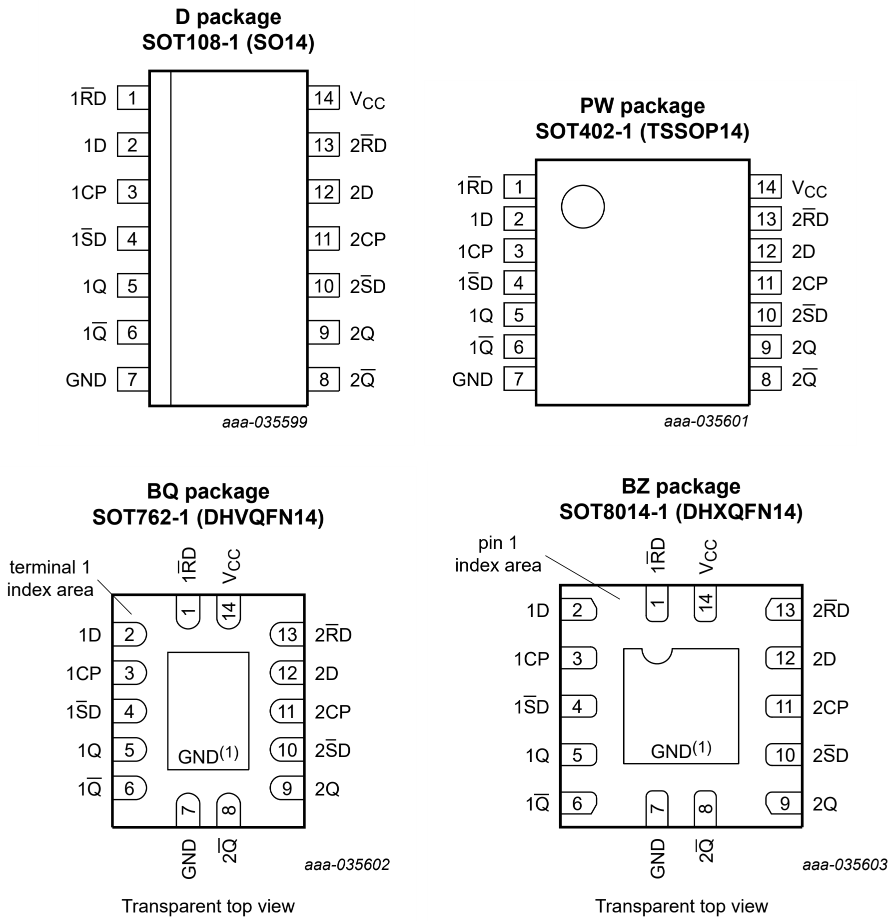


Fig. 4. Logic diagram for one flip-flop

5. Pinning information

5.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{\text{R}}$D	1	asynchronous reset-direct input (active LOW)
1D	2	data input
1CP	3	clock input (LOW-to-HIGH, edge-triggered)
1$\overline{\text{S}}$D	4	asynchronous set-direct input (active LOW)
1Q	5	output
1$\overline{\text{Q}}$	6	complement output
GND	7	ground (0 V)
2$\overline{\text{Q}}$	8	complement output
2Q	9	output
2$\overline{\text{S}}$D	10	asynchronous set-direct input (active LOW)
2CP	11	clock input (LOW-to-HIGH, edge-triggered)
2D	12	data input
2$\overline{\text{R}}$D	13	asynchronous reset-direct input (active LOW)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don’t care.

Input				Output	
n$\overline{\text{S}}$D	**n$\overline{\text{R}}$D**	**nCP**	**nD**	**nQ**	**n$\overline{\text{Q}}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don’t care;

↑ = LOW-to-HIGH transition; Q_{n+1} = state after the next LOW-to-HIGH CP transition.

Input				Output	
n$\overline{\text{S}}$D	**n$\overline{\text{R}}$D**	**nCP**	**nD**	**nQ_{n+1}**	**$n\overline{Q}_{n+1}$**
H	H	↑	L	L	H
H	H	↑	H	H	L

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V		-	±20	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V		-	±20	mA
I_O	output current	V_O = -0.5 V to (V_{CC} + 0.5 V)		-	±25	mA
I_{CC}	supply current			-	+100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C				
		SOT108-1 (SO14)	[1]	-	500	mW
		SOT402-1 (TSSOP14)	[2]			
		SOT762-1 (DHVQFN14)	[3]			
		SOT8014-1 (DHXQFN14)		-	250	mW

[1] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
[2] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
[3] For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC74			74HCT74			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
74HC74								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.84	4.32	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.34	5.81	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	40	-	80	μA
C_I	input capacitance		-	3.5	-	-	-	pF
74HCT74								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V						
		I_O = -4 mA	3.84	4.32	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V						
		I_O = 4.0 mA	-	0.15	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±1.0	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	40	-	80	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC}$ - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A						
		per input pin; nD, n$\overline{RD}$ inputs	-	70	315	-	343	μA
		per input pin; n$\overline{SD}$, nCP input	-	80	360	-	392	μA
C_I	input capacitance		-	3.5	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Fig. 7.

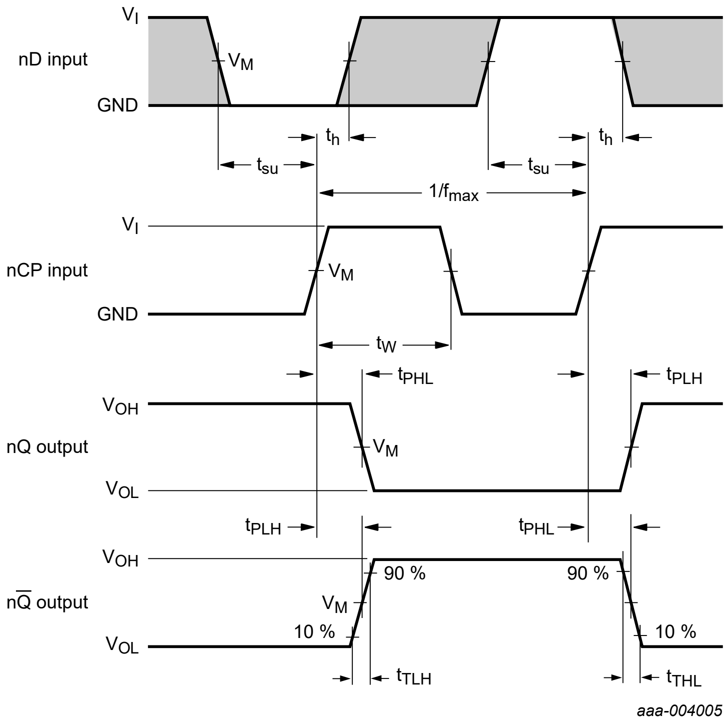
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
74HC74								
t_{pd}	propagation delay	nCP to nQ, n$\overline{Q}$; see Fig. 5 [2]						
		V_{CC} = 2.0 V	-	47	220	-	265	ns
		V_{CC} = 4.5 V	-	17	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	14	-	-	-	ns
		V_{CC} = 6.0 V	-	14	37	-	45	ns
		n$\overline{SD}$ to nQ, n$\overline{Q}$; see Fig. 6 [2]						
		V_{CC} = 2.0 V	-	50	250	-	300	ns
		V_{CC} = 4.5 V	-	18	50	-	60	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	-	-	ns
		V_{CC} = 6.0 V	-	14	43	-	51	ns
		n$\overline{RD}$ to nQ, n$\overline{Q}$; see Fig. 6 [2]						
		V_{CC} = 2.0 V	-	52	250	-	300	ns
		V_{CC} = 4.5 V	-	19	50	-	60	ns
		V_{CC} = 5 V; C_L = 15 pF	-	16	-	-	-	ns
		V_{CC} = 6.0 V	-	15	43	-	51	ns
t_t	transition time	nQ, n$\overline{Q}$; see Fig. 5 [3]						
		V_{CC} = 2.0 V	-	19	95	-	110	ns
		V_{CC} = 4.5 V	-	7	19	-	22	ns
		V_{CC} = 6.0 V	-	6	16	-	19	ns
t_W	pulse width	nCP HIGH or LOW; see Fig. 5						
		V_{CC} = 2.0 V	100	19	-	120	-	ns
		V_{CC} = 4.5 V	20	7	-	24	-	ns
		V_{CC} = 6.0 V	17	6	-	20	-	ns
		n$\overline{SD}$, n$\overline{RD}$ LOW; see Fig. 6						
		V_{CC} = 2.0 V	100	19	-	120	-	ns
		V_{CC} = 4.5 V	20	7	-	24	-	ns
		V_{CC} = 6.0 V	17	6	-	20	-	ns
t_{rec}	recovery time	n$\overline{SD}$, n$\overline{RD}$; see Fig. 6						
		V_{CC} = 2.0 V	40	3	-	45	-	ns
		V_{CC} = 4.5 V	8	1	-	9	-	ns
		V_{CC} = 6.0 V	7	1	-	8	-	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{su}	set-up time	nD to nCP; see Fig. 5						
		V_{CC} = 2.0 V	75	6	-	90	-	ns
		V_{CC} = 4.5 V	15	2	-	18	-	ns
		V_{CC} = 6.0 V	13	2	-	15	-	ns
t_h	hold time	nD to nCP; see Fig. 5						
		V_{CC} = 2.0 V	3	-6	-	3	-	ns
		V_{CC} = 4.5 V	3	-2	-	3	-	ns
		V_{CC} = 6.0 V	3	-2	-	3	-	ns
f_{max}	maximum frequency	nCP; see Fig. 5						
		V_{CC} = 2.0 V	4.8	23	-	4.0	-	MHz
		V_{CC} = 4.5 V	24	69	-	20	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	76	-	-	-	MHz
		V_{CC} = 6.0 V	28	82	-	24	-	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} [4]	-	24	-	-	-	pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
74HCT74								
t_{pd}	propagation delay	nCP to nQ, n$\overline{Q}$; see Fig. 5 [2]						
		V_{CC} = 4.5 V	-	18	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	-	-	ns
		n$\overline{SD}$ to nQ, n$\overline{Q}$; see Fig. 6 [2]						
		V_{CC} = 4.5 V	-	23	50	-	60	ns
		V_{CC} = 5 V; C_L = 15 pF	-	18	-	-	-	ns
		n$\overline{RD}$ to nQ, n$\overline{Q}$; see Fig. 6 [2]						
		V_{CC} = 4.5 V	-	24	50	-	60	ns
		V_{CC} = 5 V; C_L = 15 pF	-	18	-	-	-	ns
t_t	transition time	nQ, n$\overline{Q}$; see Fig. 5 [3]						
		V_{CC} = 4.5 V	-	7	19	-	22	ns
t_W	pulse width	nCP HIGH or LOW; see Fig. 5						
		V_{CC} = 4.5 V	23	9	-	27	-	ns
		n$\overline{SD}$, n$\overline{RD}$ LOW; see Fig. 6						
		V_{CC} = 4.5 V	20	9	-	24	-	ns
t_{rec}	recovery time	n$\overline{SD}$, n$\overline{RD}$; see Fig. 6						
		V_{CC} = 4.5 V	8	1	-	9	-	ns
t_{su}	set-up time	nD to nCP; see Fig. 5						
		V_{CC} = 4.5 V	15	5	-	18	-	ns
t_h	hold time	nD to nCP; see Fig. 5						
		V_{CC} = 4.5 V	3	-3	-	3	-	ns
f_{max}	maximum frequency	nCP; see Fig. 5						
		V_{CC} = 4.5 V	22	54	-	18	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	59	-	-	-	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} - 1.5 V [4]	-	29	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] t_t is the same as t_{THL} and t_{TLH}.
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

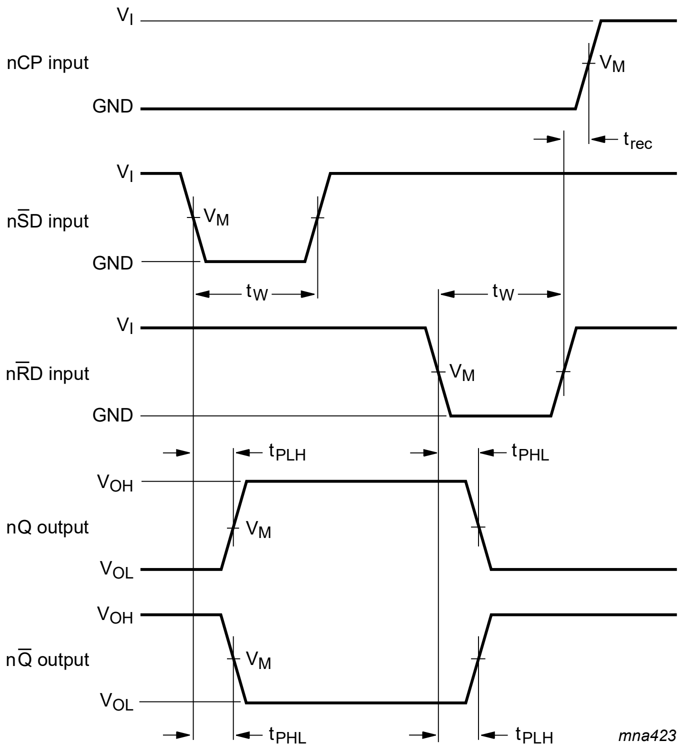
10.1. Waveforms and test circuit



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Propagation delay input (CP) to output (Qn), output transition time, clock input (CP) pulse width and the maximum frequency (CP)



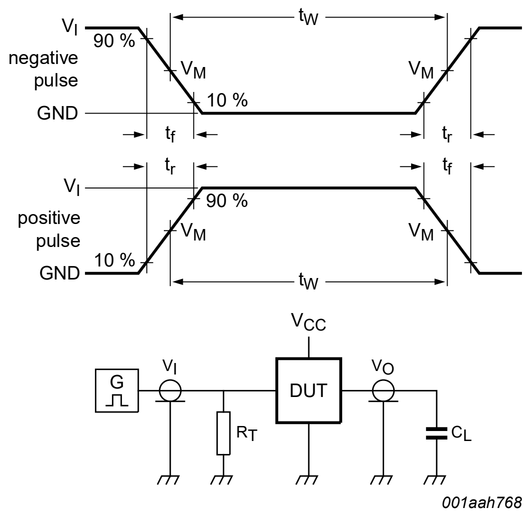
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. The set (nS̄D) and reset (nR̄D) input to output (nQ,nQ̄) propagation delays, set and reset pulse widths and the nS̄D, nR̄D to nCP recovery time

Table 9. Measurement points

Type	Input	Output
	V_M	**V_M**
74HC74	$0.5V_{CC}$	$0.5V_{CC}$
74HCT74	1.3 V	1.3 V



Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

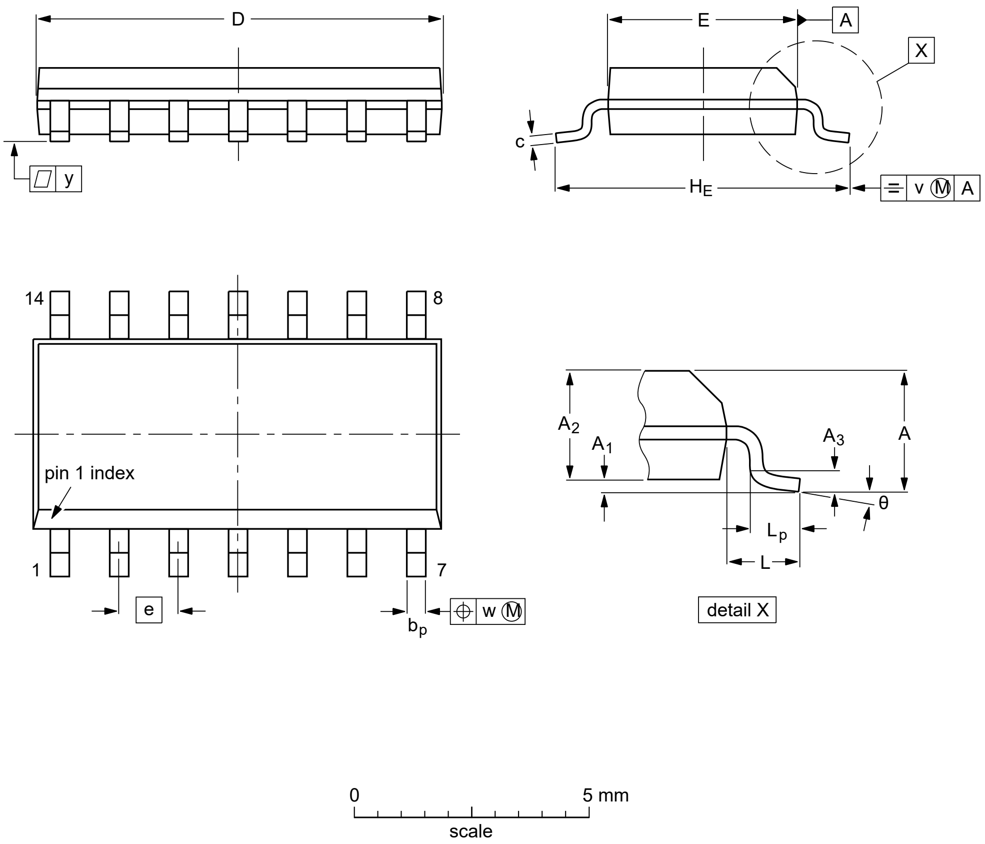
Fig. 7. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		Test
	V_I	t_r, t_f	C_L	R_L	
74HC74	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	t_{PLH}, t_{PHL}
74HCT74	3 V	6 ns	15 pF, 50 pF	1 kΩ	t_{PLH}, t_{PHL}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	8.75	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	8.55	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.344	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.337	0.15		0.228		0.016				0°

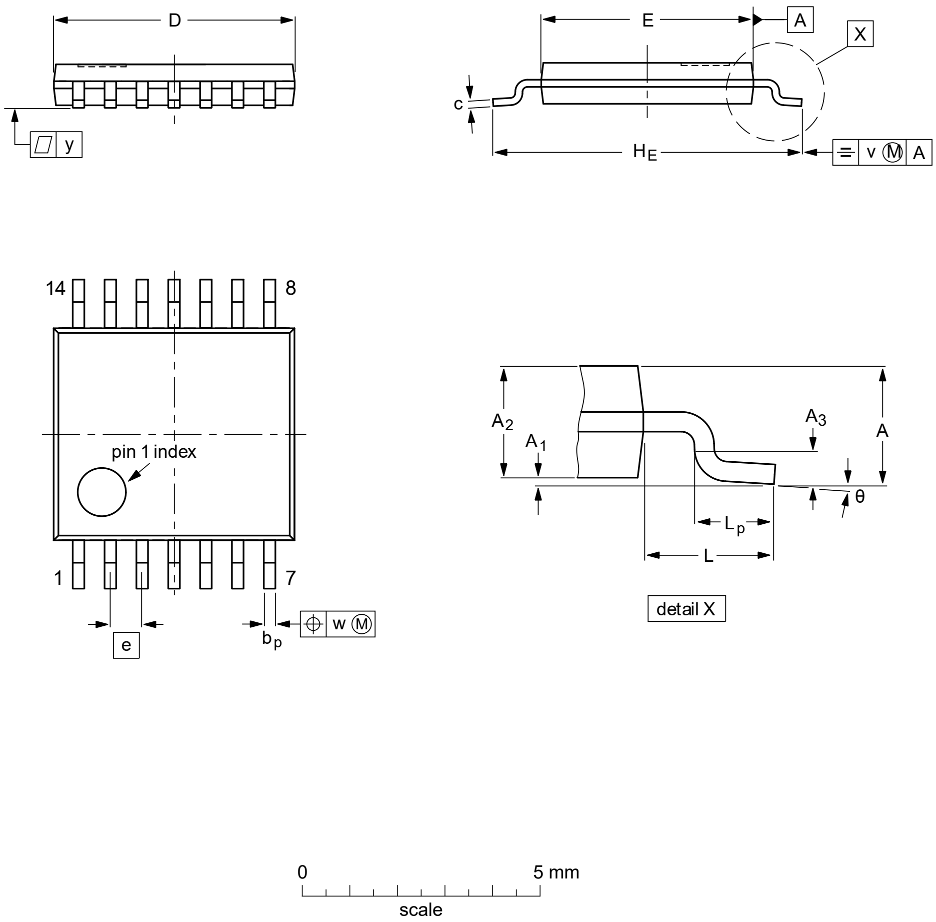
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot108-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT108-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	v	w	y	θ
	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
mm	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

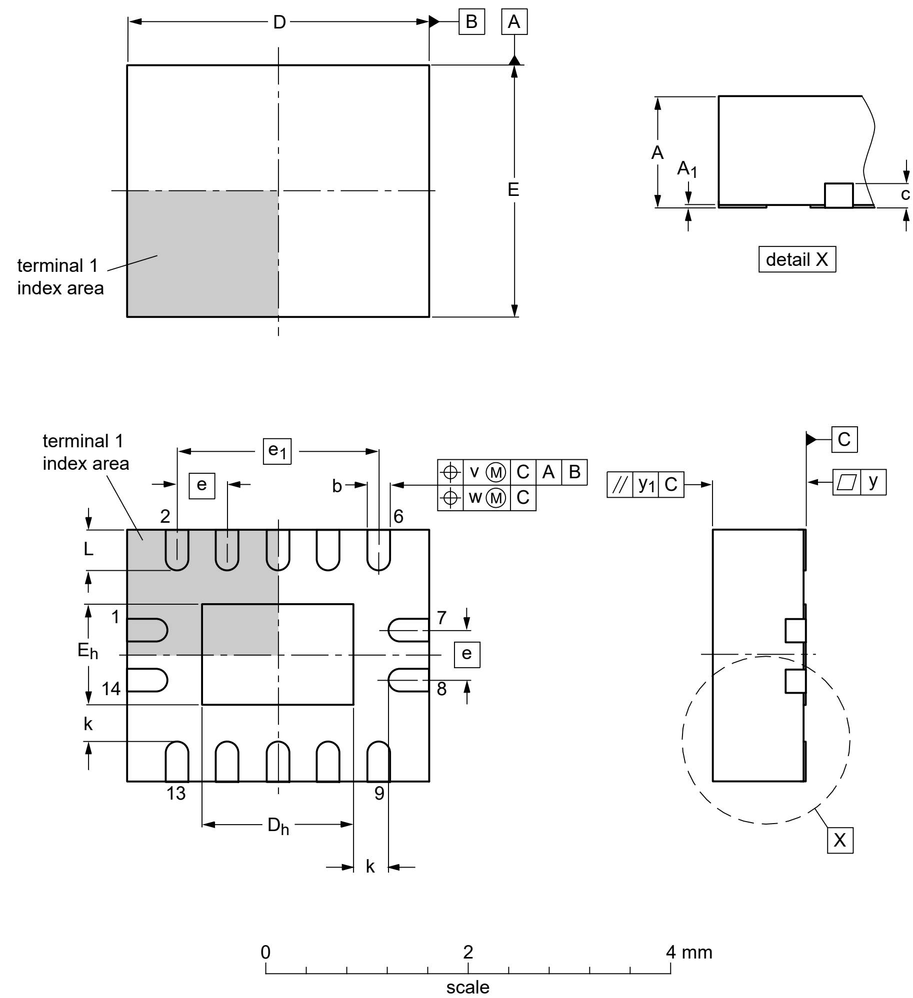
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	k	L	v	w	y	y_1
mm	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

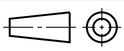
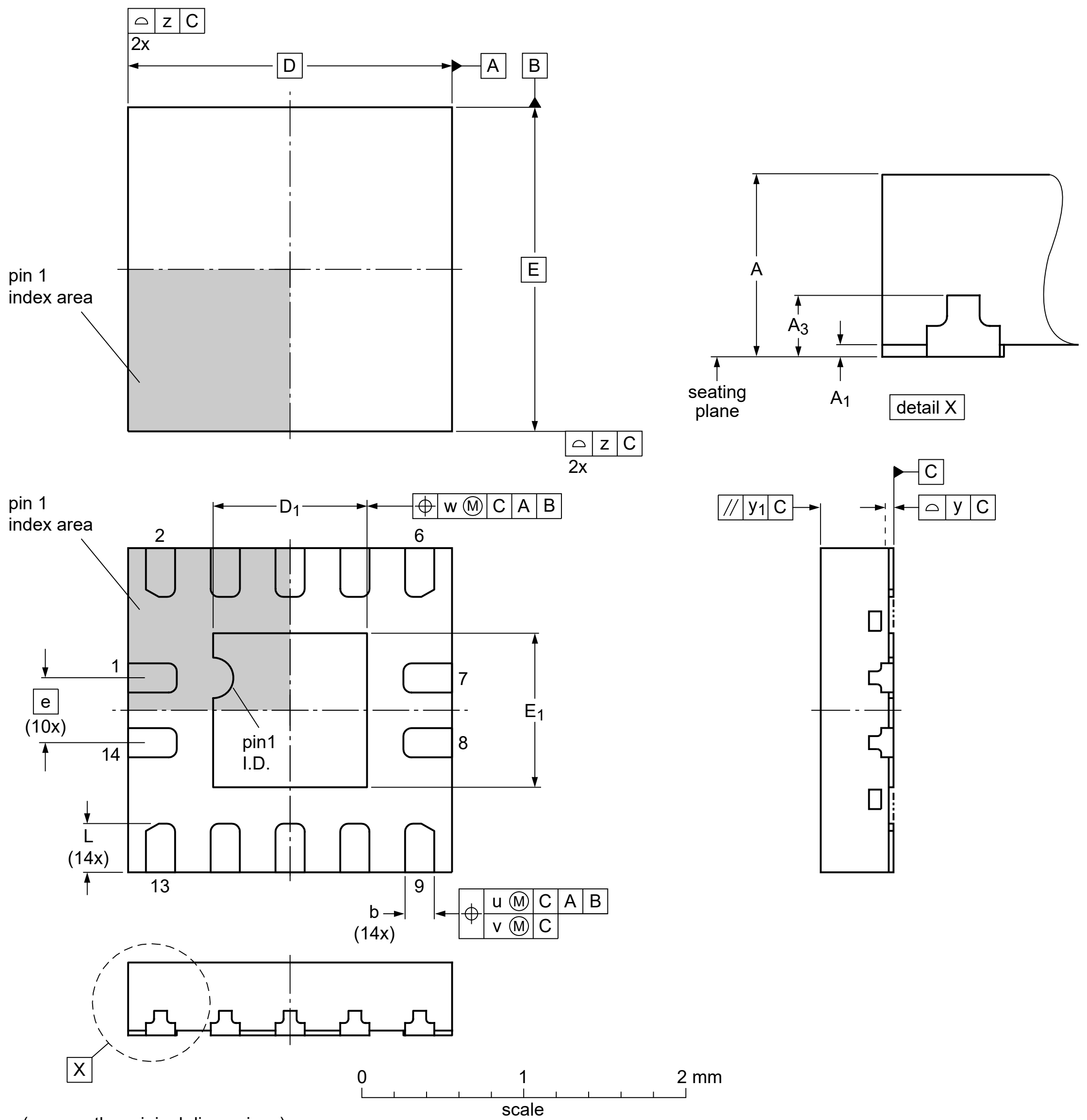
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig. 10. Package outline SOT762-1 (DHVQFN14)

DHXQFN14: plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 14 terminals; 0.4 mm pitch; body 2 mm x 2 mm x 0.48 mm **SOT8014-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_3	b	D	D_1	E	E_1	e	k	L	u	v	w	y	y_1	z
mm	max	0.48	0.05	0.15 (typ)	0.23		1.00		1.00			0.35						
	nom	0.45	0.02		0.18	2.0	0.95	2.0	0.95	0.4		0.30	0.1	0.05	0.1	0.05	0.05	0.05
	min	0.42	0.00		0.13		0.90		0.90		0.2	0.25						

sot8014-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8014-1						~~20-09-18~~ 20-09-22

Fig. 11. Package outline SOT8014-1 (DHXQFN14)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT74 v.9	20240402	Product data sheet	-	74HC_HCT74 v.8
Modifications:	• Fig. 8, Fig. 9: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT74 v.8	20230209	Product data sheet	-	74HC_HCT74 v.7
Modifications:	• Added type numbers 74HC74BZ and 74HCT74BZ (SOT8014-1/DHXQFN14).			
74HC_HCT74 v.7	20210913	Product data sheet	-	74HC_HCT74 v.6
Modifications:	• Type numbers 74HC74DB and 74HCTDB (SOT337-1/SSOP14) removed. • Section 2updated.			
74HC_HCT74 v.6	20200421	Product data sheet	-	74HC_HCT74 v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 5.1: Pin configuration for SOT762-1 (DHVQFN14) corrected (errata). • Table 5: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT74 v.5	20151203	Product data sheet	-	74HC_HCT74 v.4
Modifications:	• Type numbers 74HC74N and 74HCT74N (SOT27-1) removed.			
74HC_HCT74 v.4	20120827	Product data sheet	-	74HC_HCT74 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT74 v.3	20030710	Product data sheet	-	74HC_HCT74_CNV v.2
74HC_HCT74_CNV v.2	19980223	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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