General Description

The AGM30P10AP combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

This device is ideal for load switch and battery protection applications.

Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance
- 100% Avalanche tested
- 100% DVDS tested

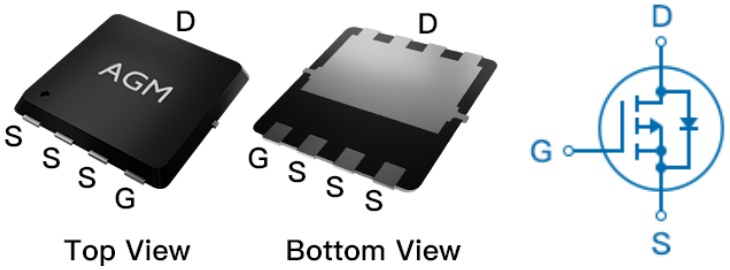
Application

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

Product Summary

BVDSS	RDSON	ID
-30V	9.6mΩ	-50A

PDFN3*3 Pin Configuration



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM30P10	AGM30P10AP	PDFN3.3*3.3	330mm	12mm	5000

Table 1. Absolute Maximum Ratings (TA=25℃)

Symbol	Parameter	Value	Unit
VDS	Drain-Source Voltage (VGS=0V)	-30	V
VGS	Gate-Source Voltage (VDS=0V)	±20	V
ID	Drain Current-Continuous(Tc=25℃) **(Note 1)**	-50	A
	Drain Current-Continuous(Tc=100℃)	-33	A
IDM (pluse)	Drain Current-Pulsed **(Note 2)**	-200	A
PD	Maximum Power Dissipation(Tc=25℃)	3.5	w
	Maximum Power Dissipation(Tc=100℃)	1.4	w
EAS	Avalanche energy **(Note 3)**	132	mJ
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	℃

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
RθJA	Thermal Resistance Junction-ambient (Steady State)[1]	---	50	℃/W
RθJC	Thermal Resistance Junction-Case[1]	---	35.7	℃/W

Table 3. Electrical Characteristics (TJ=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	VGS=0V ID=250μA	-30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	VDS=-30V,VGS=0V	--	--	-1.0	μA
I_{GSS}	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	VDS=VGS,ID=-250μA	-1.2	-1.7	-2.2	V
gFS	Forward Transconductance	VDS=-10V,ID=-10A	--	17	--	S
$R_{DS(on)}$	Drain-Source On-State Resistance	VGS=-10V, ID=-10A	--	9.6	12	mΩ
		VGS=-4.5V, ID=-5A	--	12	16	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	VDS=-15V,VGS=0V F=1MHZ	--	1460	--	pF
C_{oss}	Output Capacitance		--	199	--	pF
C_{rss}	Reverse Transfer Capacitance		--	147	--	pF
Rg	Gate resistance	VGS=0V, VDS=0V,f=1.0MHz	--	13.5	--	Ω
Switching Times						
$t_{d(on)}$	Turn-on Delay Time	VGS=-10V,VDS=-15V, ID=-25A,RGEN=3Ω	--	13	--	nS
t_r	Turn-on Rise Time		--	8.5	--	nS
$t_{d(off)}$	Turn-Off Delay Time		--	26	--	nS
t_f	Turn-Off Fall Time		--	12	--	nS
Q_g	Total Gate Charge	VGS=-10V, VDS=-15V, ID=-25A	--	32	--	nC
Q_{gs}	Gate-Source Charge		--	6.0	--	nC
Q_{gd}	Gate-Drain Charge		--	10	--	nC
Source-Drain Diode Characteristics						
I_{SD}	Source-Drain Current(Body Diode)		--	--	-50	A
V_{SD}	Forward on Voltage	VGS=0V,IS=-10A	--	--	-1.2	V
t_{rr}	Reverse Recovery Time	IF=-10A , dI/dt=100A/μs , TJ=25℃	--	32	--	ns
Q_{rr}	Reverse Recovery Charge		--	21	--	nc

Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature

Notes 3.EAS condition: TJ=25℃ , VDD=-15V,Vgs=-10V,ID=-23A,L=0.5mH,RG=25ohm

P- Channel Typical Characteristics

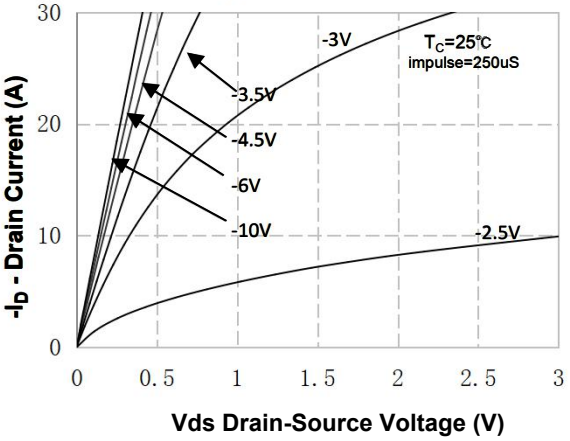


Figure 1. On-Region Characteristics

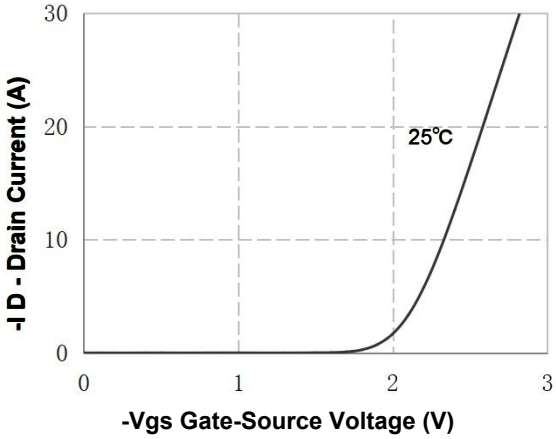


Figure 2. Transfer Characteristics

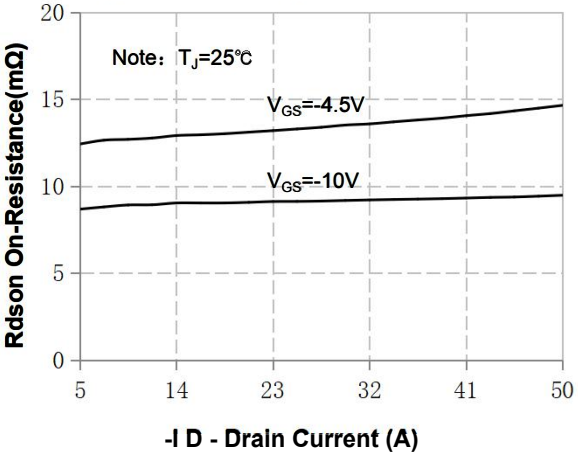


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

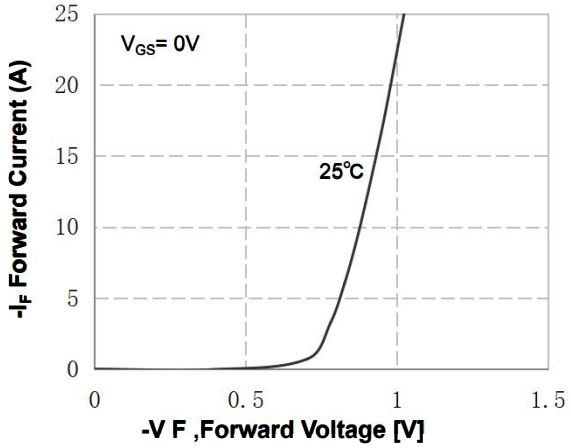


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

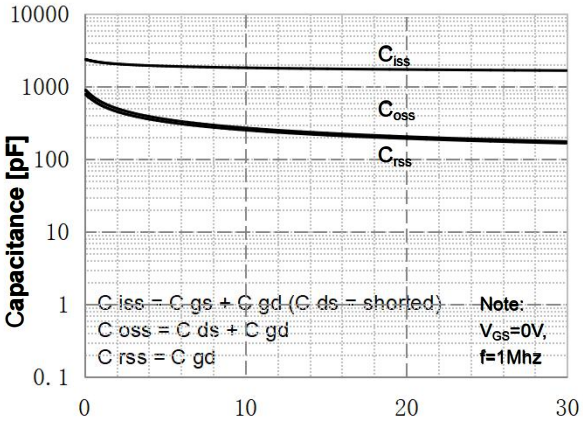


Figure 5. Capacitance Characteristics

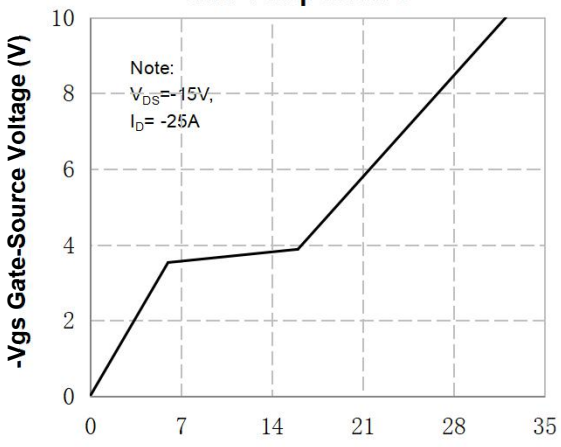


Figure 6. Gate Charge Characteristics

P- Channel Typical Characteristics (Continued)

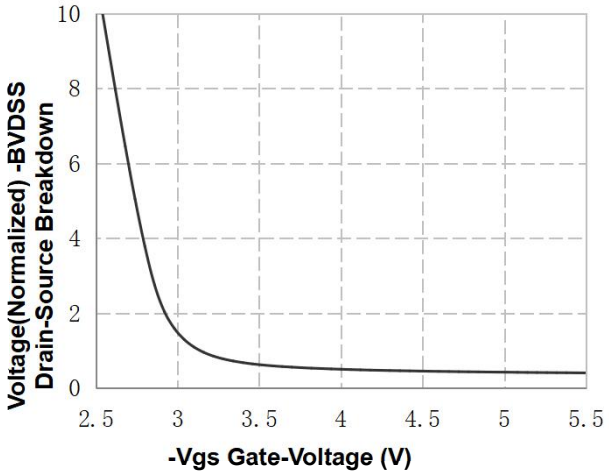


Figure 7. Breakdown Voltage Variation vs Gate-Voltage

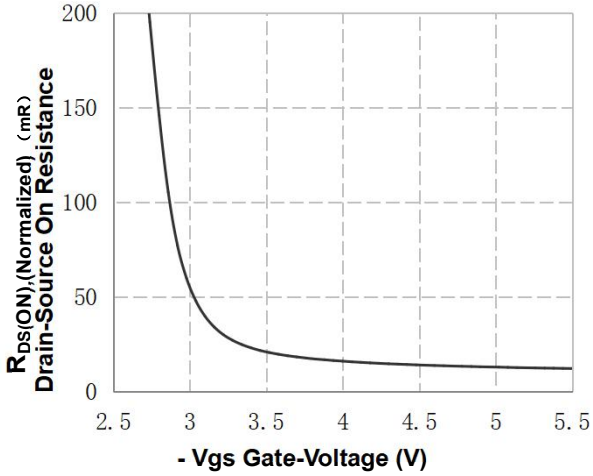


Figure 8. On-Resistance Variation vs Gate Voltage

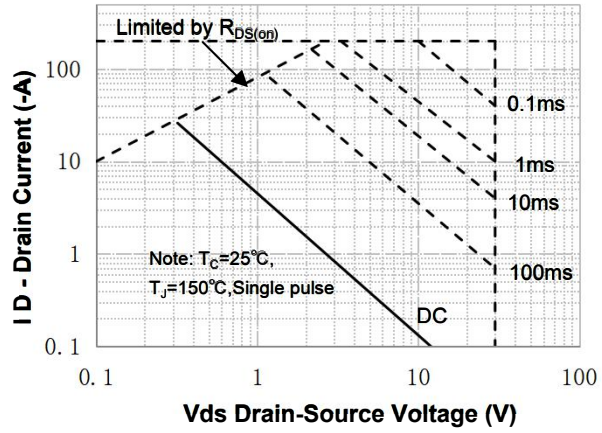


Figure 9. Maximum Safe Operating Area

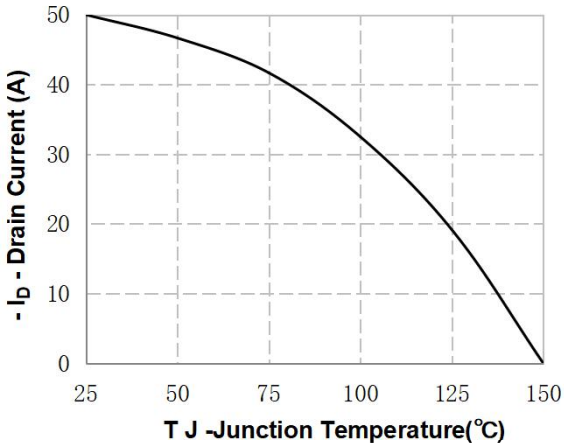


Figure 10. Maximum PContinuous Drain Currentvs Case Temperature

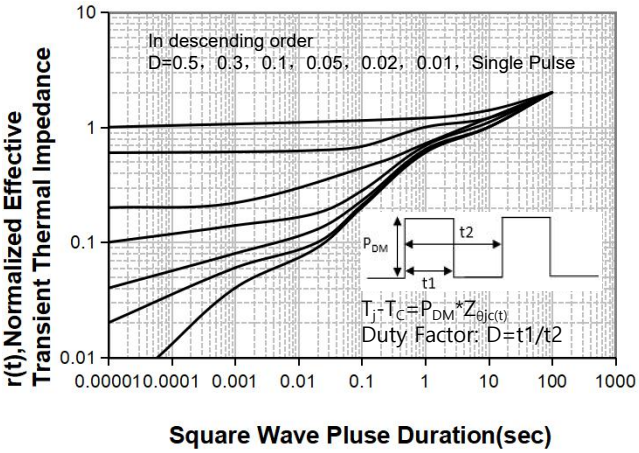
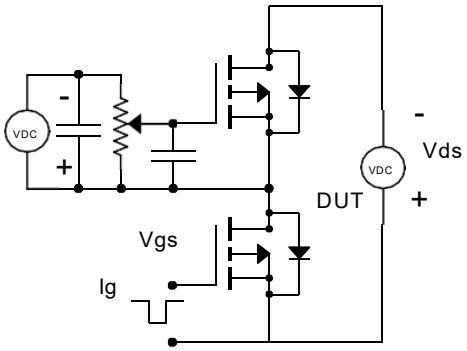
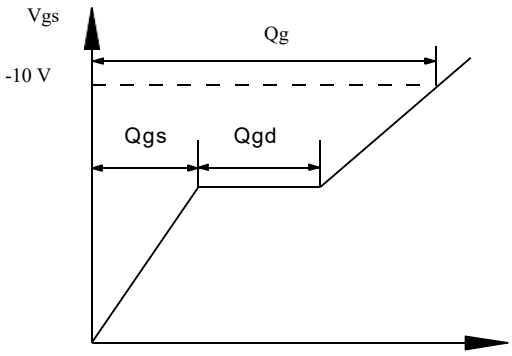


Figure 11. Transient Thermal Response Curve

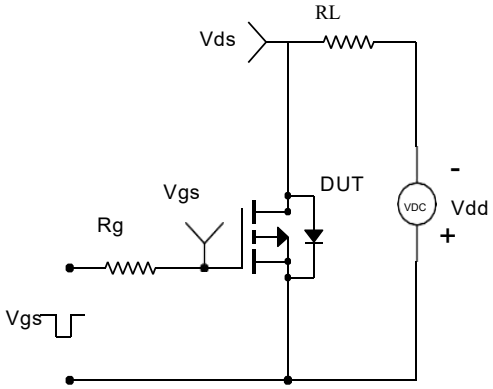
P- Channel

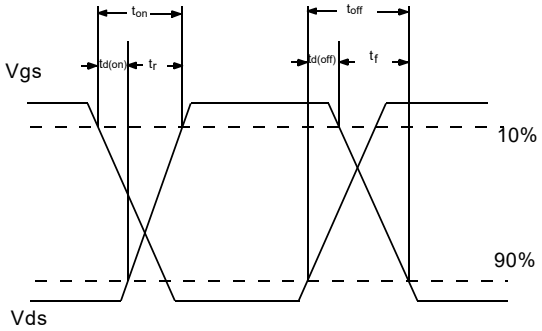
Gate Charge Test Circuit & Waveform



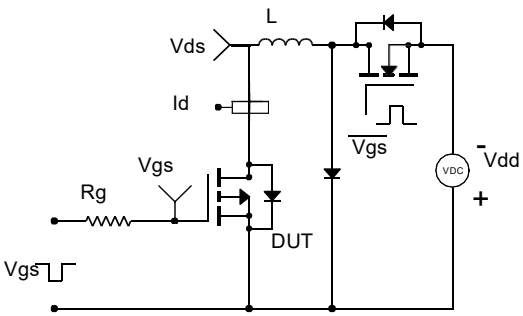


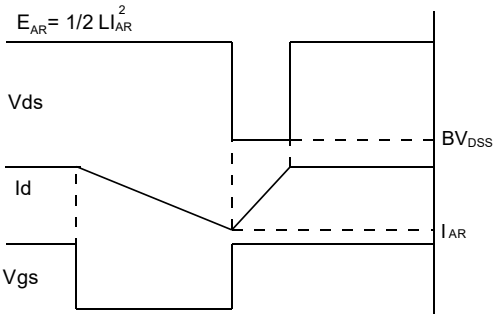
Resistive Switching Test Circuit & Waveforms





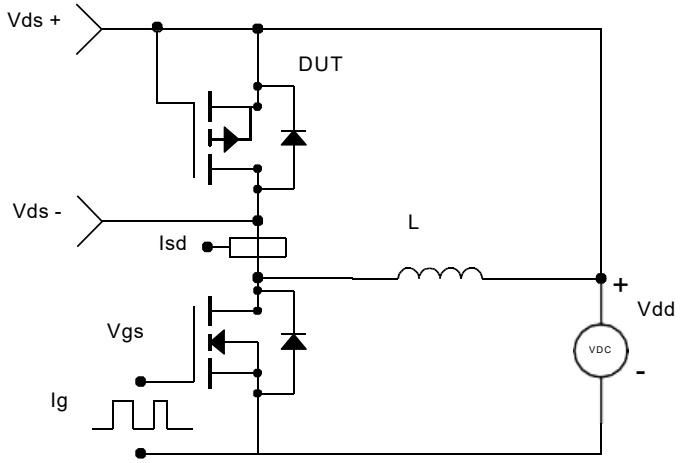
Unclamped Inductive Switching Test Circuit & Waveforms



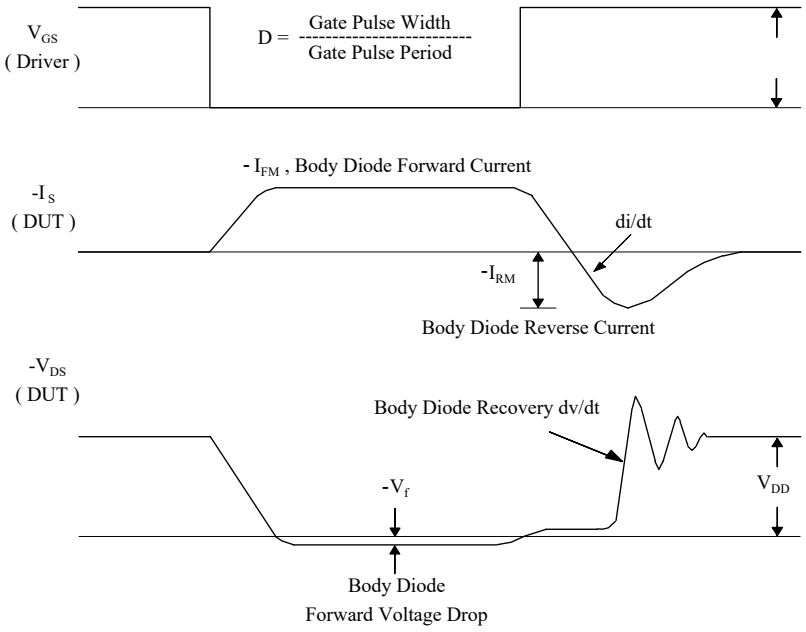


P- Channel

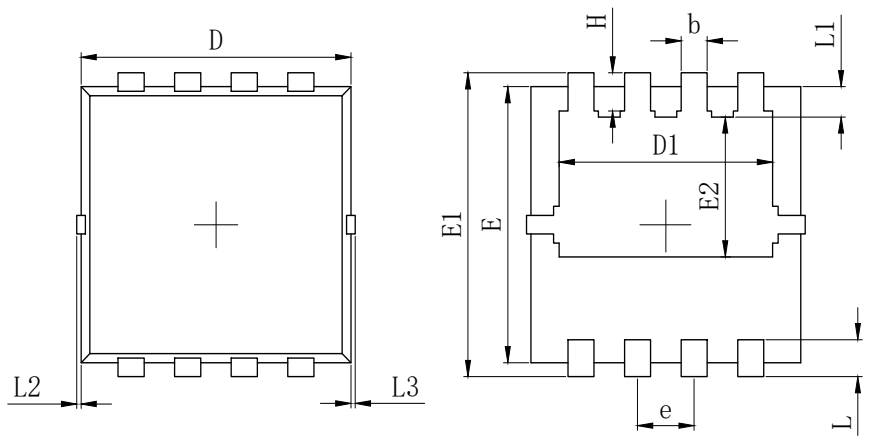
Peak Diode Recovery dv/dt Test Circuit & Waveforms



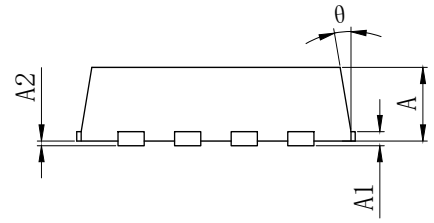
• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

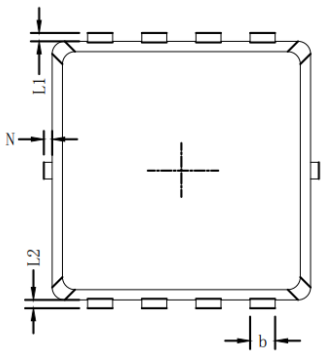


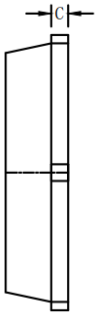
●Dimensions（PDFN3.3×3.3）

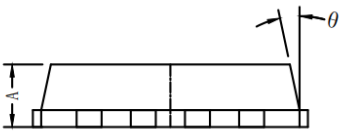


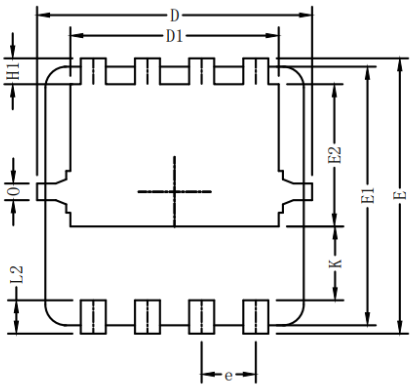
SYMBOL	MILLIMETER		
	MIN	Typ.	MAX
A	0.700	0.800	0.900
A1	0.152 REF.		
A2	0~0.05		
D	3.000	3.100	3.200
D1	2.300	2.450	2.600
E	2.900	3.000	3.100
E1	3.150	3.300	3.450
E2	1.320	1.520	1.720
b	0.200	0.300	0.400
e	0.550	0.650	0.750
L	0.300	0.400	0.500
L1	0.180	0.330	0.480
L2	0~0.100		
L3	0~0.100		
H	0.315	0.415	0.515
θ	8°	10°	12°











Symbols	Millimeters		
	MIN.	NOM.	MAX.
A	0.65	0.75	0.85
b	0.25	0.30	0.35
C	0.15	0.20	0.25
D	3.00	3.10	3.20
D1	2.40	2.50	2.60
E	3.20	3.30	3.40
E1	3.00	3.10	3.20
E2	1.60	1.70	1.80
e	0.65 BSC.		
H1	0.21	0.31	0.41
H2	0.30	0.40	0.50
K	0.78	0.88	0.98
L1/L2	0.10 REF.		
θ	11°	12°	13°
N	0	-	0.15
0	0.2 REF.		

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