74HC253; 74HCT253

Dual 4-input multiplexer; 3-state

Rev. 10 — 11 March 2024 Product data sheet

1. General description

The 74HC253; 74HCT253 is a dual 4-bit multiplexer, each with four binary inputs (nI0 to nI3), an output enable input ($n\overline{OE}$) and shared select inputs (S0 and S1). One of the four binary inputs is selected by the select inputs and routed to the output nY. A HIGH on $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Non-inverting data path
- 3-state outputs interface directly with system bus
- Common select inputs
- Separate output enable inputs
- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
  - For 74HC253: CMOS level
  - For 74HCT253: TTL level
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Applications

- Data selectors
- Data multiplexers

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC253D 74HCT253D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC253PW 74HCT253PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC253BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

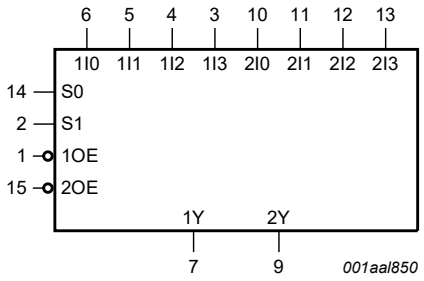


Fig. 1. Logic symbol

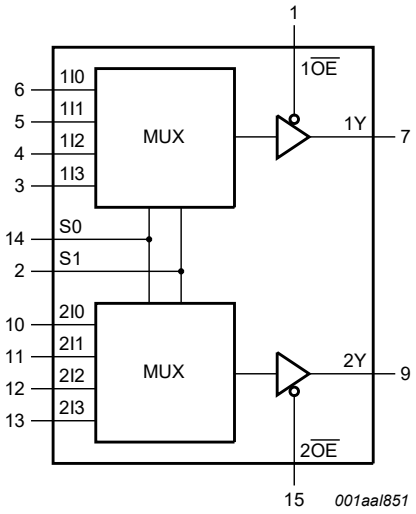


Fig. 2. Functional diagram

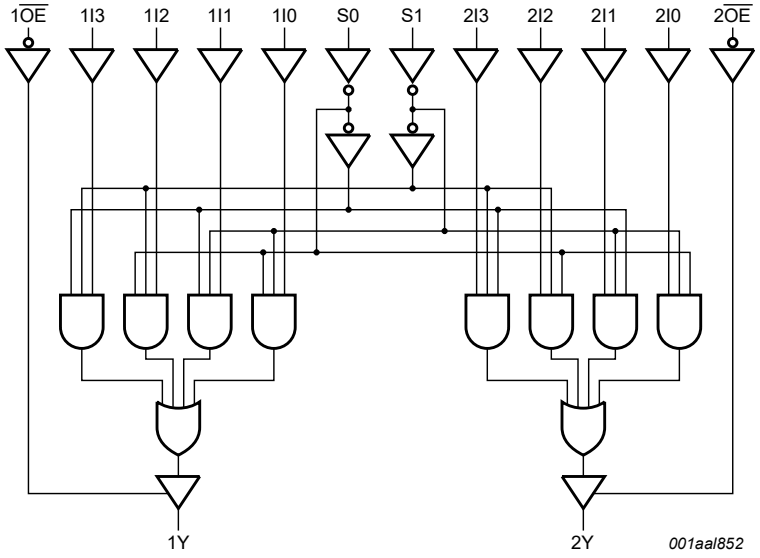
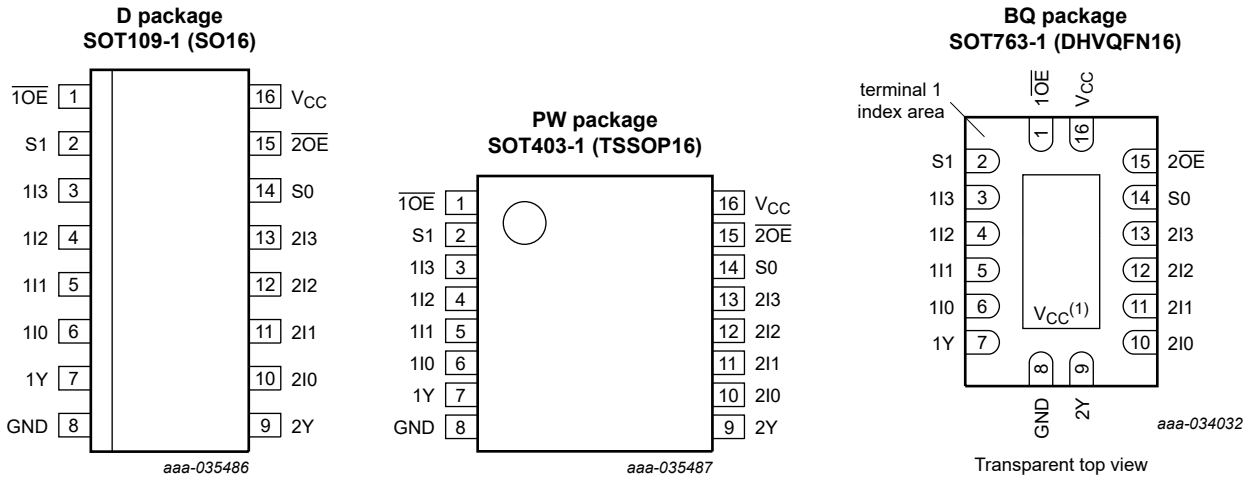


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning



(1) This is not a supply pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to V_{CC}.

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$	1, 15	output enable inputs (active LOW)
S0, S1	14, 2	data select inputs
1I0, 1I1, 1I2, 1I3	6, 5, 4, 3	data inputs source 1
1Y	7	multiplexer output source 1
GND	8	ground (0 V)
2Y	9	multiplexer output source 2
2I0, 2I1, 2I2, 2I3	10, 11, 12, 13	data inputs source 2
V_{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

select Inputs		data inputs				output enable	output
S0	**S1**	**nI0**	**nI1**	**nI2**	**nI3**	**n$\overline{OE}$**	**nY**
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±50	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V		-	±35	mA
I_{CC}	supply current			-	70	mA
I_{GND}	ground current			-70	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC253			74HCT253			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC253										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -7.8 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.5	-	±5.0	-	±10.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT253										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -6 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.5	-	±5.0	-	±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A								
		per input pin; 1In, 2In inputs	-	40	144	-	180	-	196	µA
		per input pin; n$\overline{OE}$ input	-	110	396	-	495	-	539	µA
		per input pin; Sn input	-	110	396	-	495	-	539	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

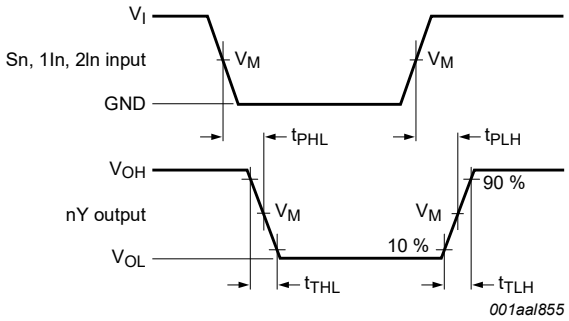
Voltages are referenced to GND (ground = 0 V); For test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
			Typ	Max	Max	Max	
74HC253							
t_{pd}	propagation delay	1In to 1Y or 2In to 2Y; see Fig. 4 [1]					
		V_{CC} = 2.0 V	55	175	220	265	ns
		V_{CC} = 4.5 V	20	35	44	53	ns
		V_{CC} = 5.0 V; C_L = 15 pF	17	-	-	-	ns
		V_{CC} = 6.0 V	16	30	37	45	ns
		Sn to nY; see Fig. 4					
		V_{CC} = 2.0 V	58	175	220	265	ns
		V_{CC} = 4.5 V	21	35	44	53	ns
		V_{CC} = 5.0 V; C_L = 15 pF	18	-	-	-	ns
		V_{CC} = 6.0 V	17	30	37	45	ns
t_{en}	enable time	n$\overline{OE}$ to nY; see Fig. 5 [2]					
		V_{CC} = 2.0 V	30	100	125	150	ns
		V_{CC} = 4.5 V	11	20	25	30	ns
		V_{CC} = 6.0 V	9	17	21	26	ns
t_{dis}	disable time	n$\overline{OE}$ to nY; see Fig. 5 [3]					
		V_{CC} = 2.0 V	41	150	190	225	ns
		V_{CC} = 4.5 V	15	30	38	45	ns
		V_{CC} = 6.0 V	12	26	33	38	ns
t_t	transition time	see Fig. 4 [4]					
		V_{CC} = 2.0 V	14	60	75	90	ns
		V_{CC} = 4.5 V	5	12	15	18	ns
		V_{CC} = 6.0 V	4	10	13	15	ns
C_{PD}	power dissipation capacitance	per multiplexer; V_I = GND to V_{CC} [5]	55	-	-	-	pF

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
			Typ	Max	Max	Max	
74HCT253							
t_{pd}	propagation delay	1In to 1Y or 2In to 2Y; see Fig. 4 [1]					
		V_{CC} = 4.5 V	20	38	48	57	ns
		V_{CC} = 5.0 V; C_L = 15 pF	17	-	-	-	ns
		Sn to nY; see Fig. 4					
		V_{CC} = 4.5 V	22	40	50	60	ns
		V_{CC} = 5.0 V; C_L = 15 pF	19	-	-	-	ns
t_{en}	enable time	n$\overline{OE}$ to nY; V_{CC} = 4.5 V; see Fig. 5 [2]	14	30	38	45	ns
t_{dis}	disable time	n$\overline{OE}$ to nY; V_{CC} = 4.5 V; see Fig. 5 [3]	13	30	38	45	ns
t_t	transition time	V_{CC} = 4.5 V; see Fig. 4	5	12	15	18	ns
C_{PD}	power dissipation capacitance	per multiplexer; V_I = GND to V_{CC} - 1.5 V [5]	55	-	-	-	pF

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.
[2] t_{en} is the same as t_{PZH}, t_{PZL}.
[3] t_{dis} is the same as t_{PHZ}, t_{PLZ}.
[4] t_t is the same as t_{THL}, t_{TLH}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

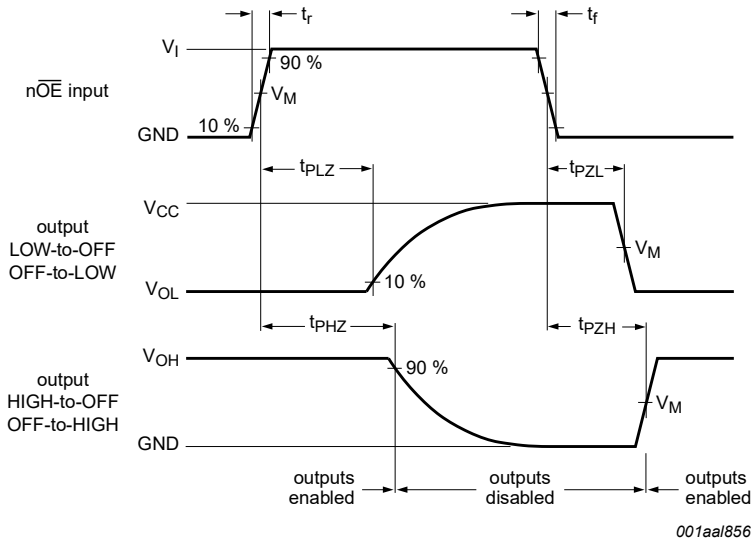
11.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. Propagation delays input (Sn, 1In, 2In) to output (nY) and output (nY) transition times



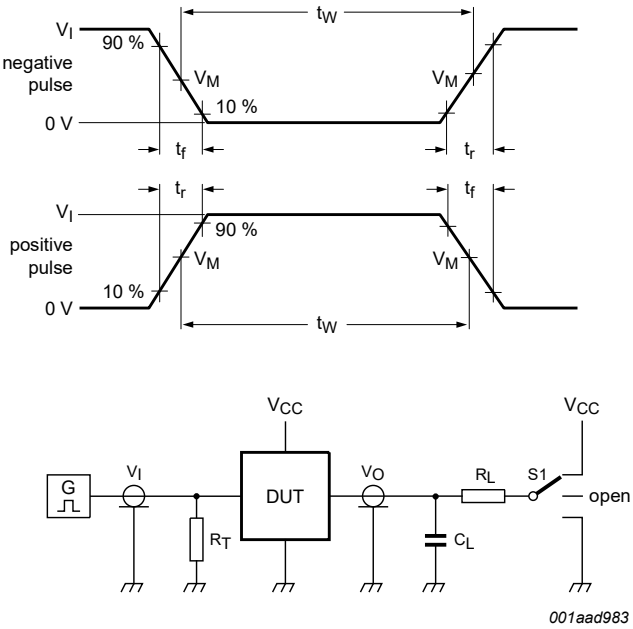
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. 3-state output enable and disable times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC253	0.5 × V_{CC}	0.5 × V_{CC}
74HCT253	1.3 V	1.3 V



Measurement points are given in Table 8 and test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistor.

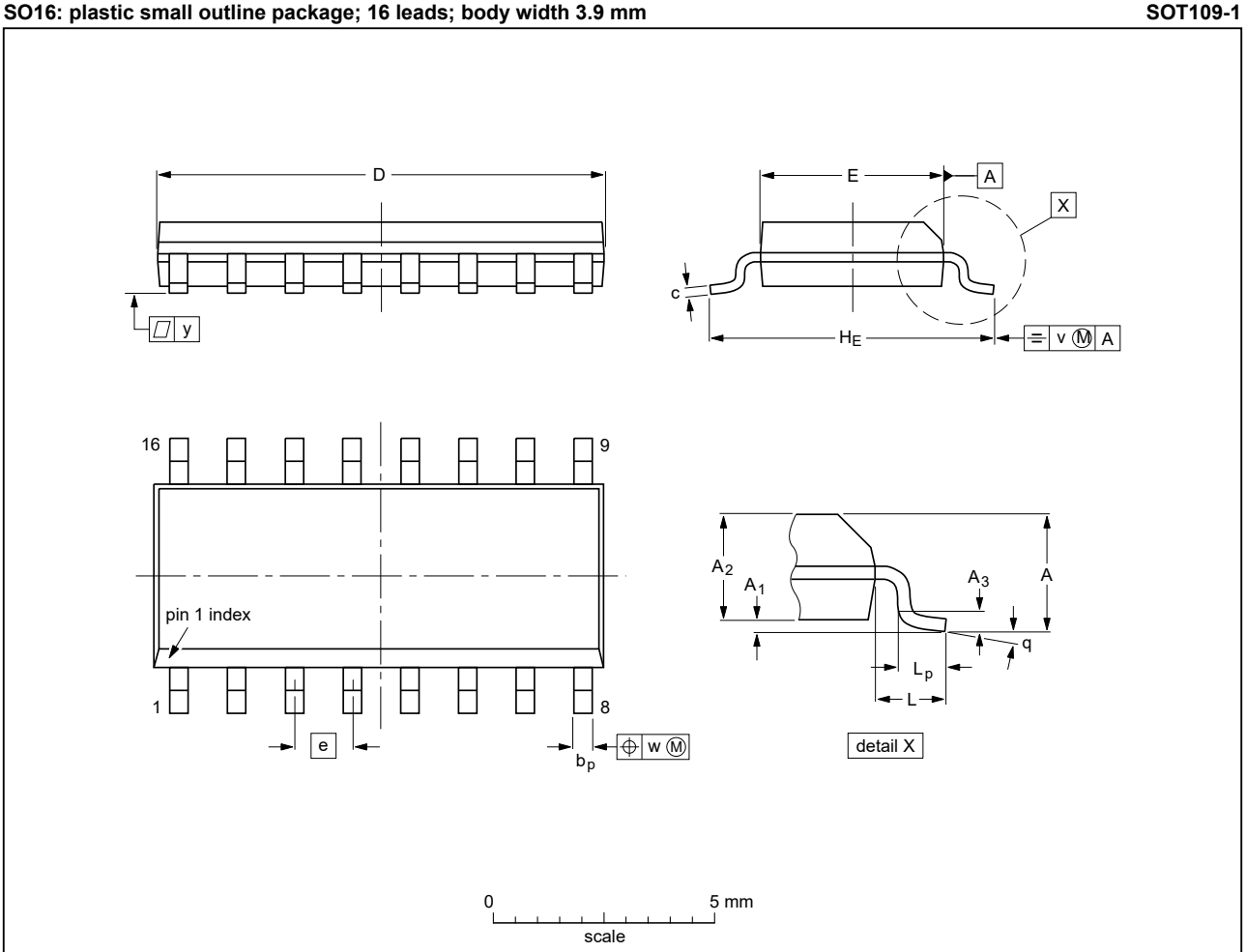
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		Switch position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC253	V_{CC}	6 ns	50 pF	1 kΩ	open	GND	V_{CC}
74HCT253	3 V	6 ns	50 pF	1 kΩ	open	GND	V_{CC}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

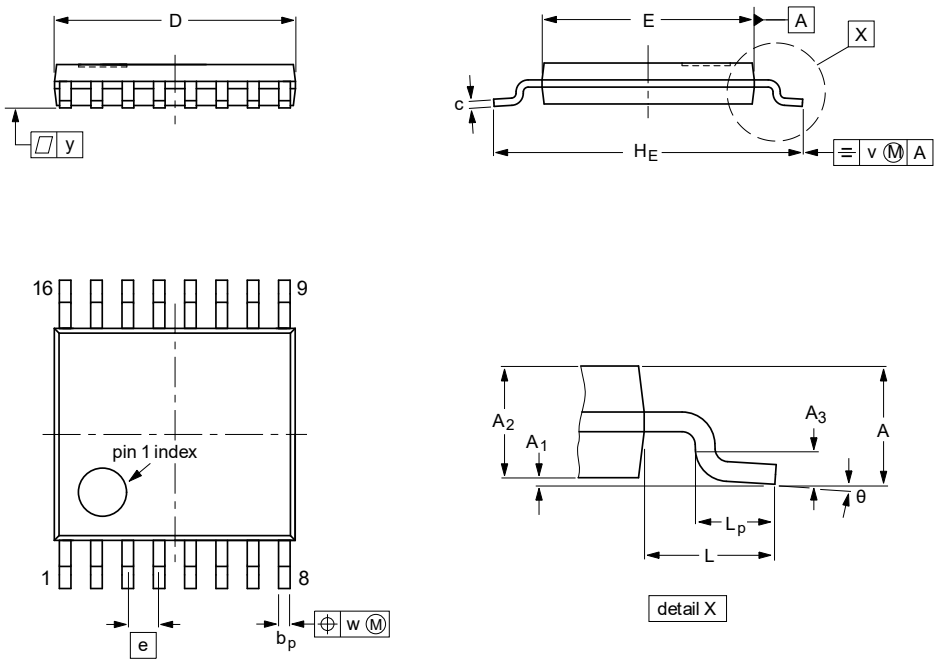
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

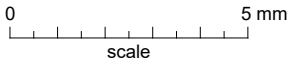
sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 7. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





Dimensions (mm are the original dimensions)

Unit	A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
mm nom				0.25					0.65		1		0.2	0.1	0.1	
min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

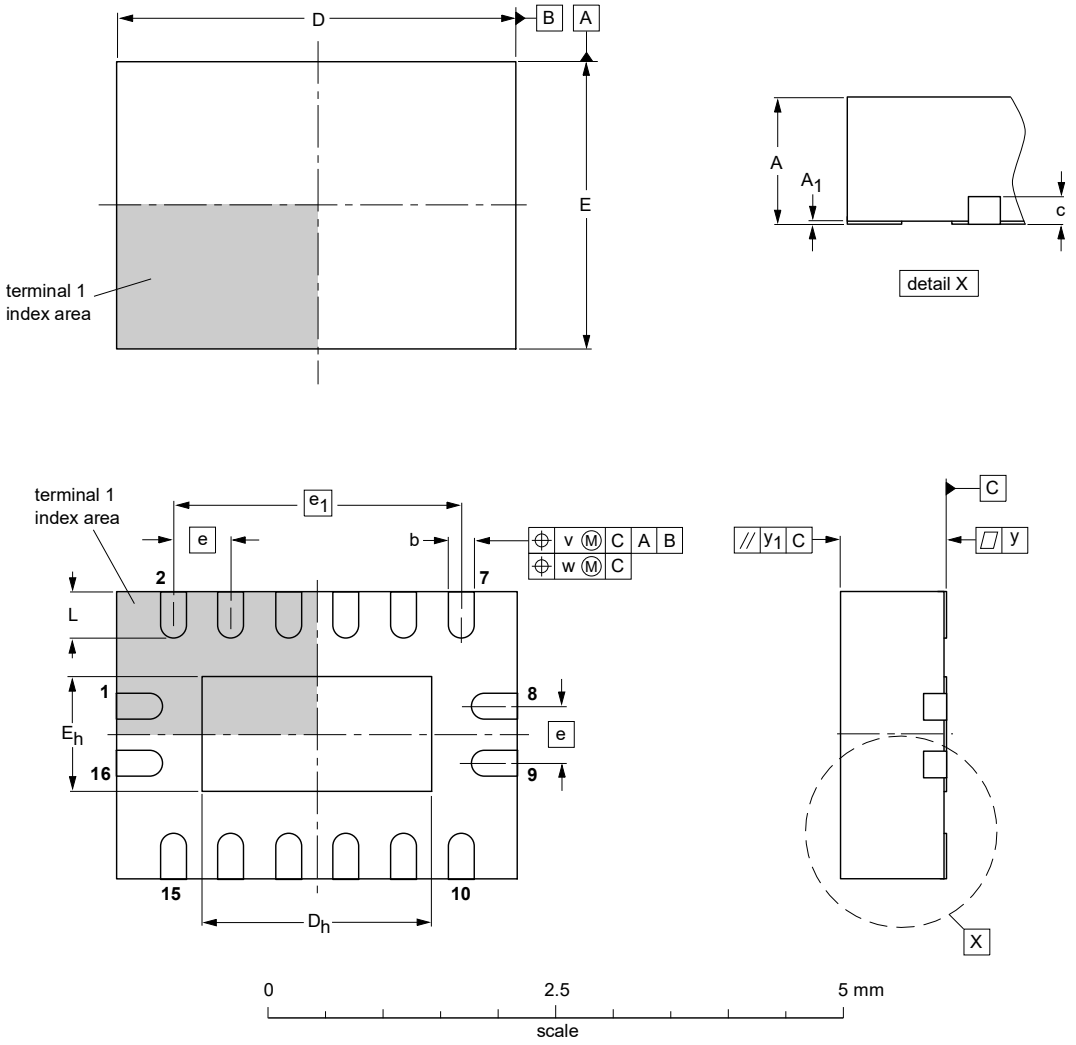
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 8. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 9. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT253 v.10	20240311	Product data sheet	-	74HC_HCT253 v.9
Modifications:	• Fig. 7, Fig. 8: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT253 v.9	20221020	Product data sheet	-	74HC_HCT253 v.8
Modifications:	• Type number 74HC253BQ (SOT763-1/DHVQFN16) added.			
74HC_HCT253 v.8	20211018	Product data sheet	-	74HC_HCT253 v.7
Modifications:	• Type number 74HCT253PW (SOT403-1/TSSOP16) added.			
74HC_HCT253 v.7	20210816	Product data sheet	-	74HC_HCT253 v.6
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC253DB and 74HCT253DB (SOT338-1/SSOP16) removed. • Type number 74HC253PW (SOT403-1/TSSOP16) added. • Section 2 updated. • Section 8: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT253 v.6	20160201	Product data sheet	-	74HC_HCT253 v.5
Modifications:	• Type numbers 74HC253N and 74HCT253N (SOT38-4) removed.			
74HC_HCT253 v.5	20150121	Product data sheet	-	74HC_HCT253 v.4
Modifications:	• Table 7: Power dissipation capacitance condition for 74HCT253 is corrected.			
74HC_HCT253 v.4	20111212	Product data sheet	-	74HC_HCT253 v.3
Modifications:	• Legal pages updated.			
74HC_HCT253 v.3	20100422	Product data sheet	-	74HC_HCT253_CNV v.2
74HC_HCT253_CNV v.2	970828	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 11 March 2024