74ALVC574

Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 4 — 11 July 2023 Product data sheet

1. General description

The 74ALVC574 is an 8-bit positive-edge triggered D-type flip-flop with 3-state outputs. The device features a clock (CP) and output enable ($\overline{OE}$) inputs. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Schmitt trigger action on all inputs makes the device tolerant of slow rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 3.6 V
- CMOS low power dissipation
- Overvoltage tolerant inputs to 3.6 V
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD78 Class II.A
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVC574D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ALVC574PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74ALVC574BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram

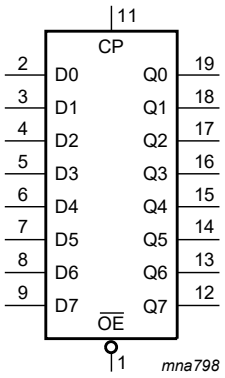


Fig. 1. Logic symbol

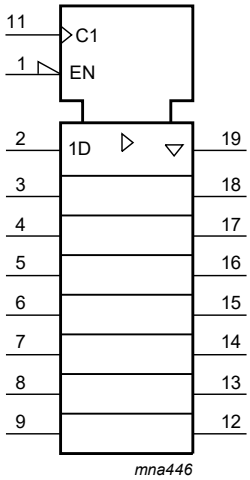


Fig. 2. IEC logic symbol

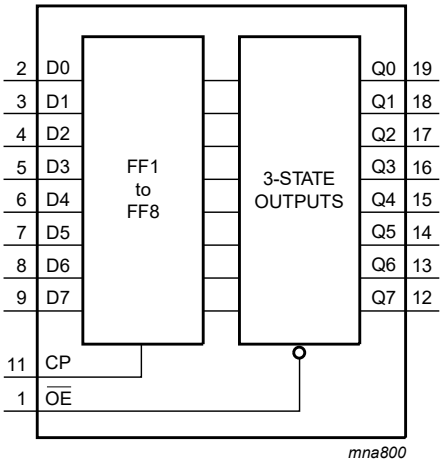


Fig. 3. Functional diagram

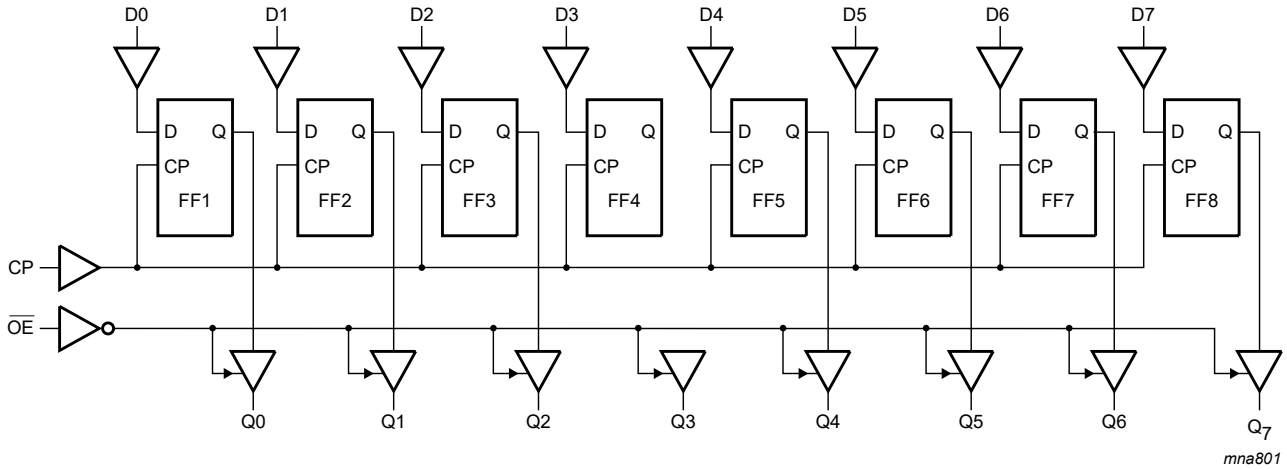
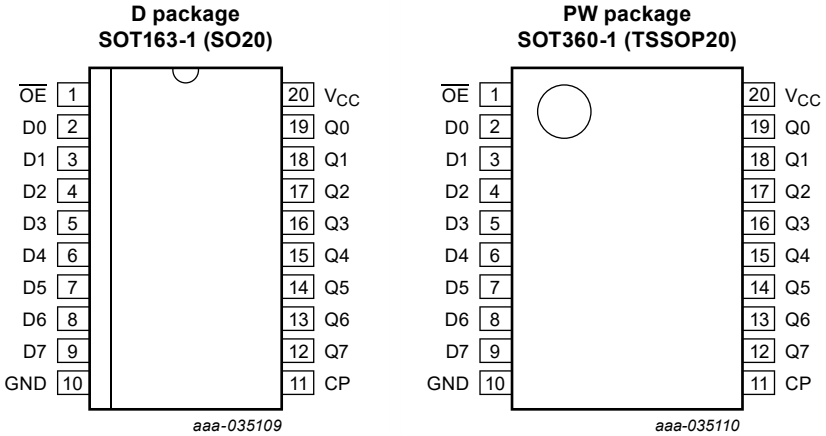
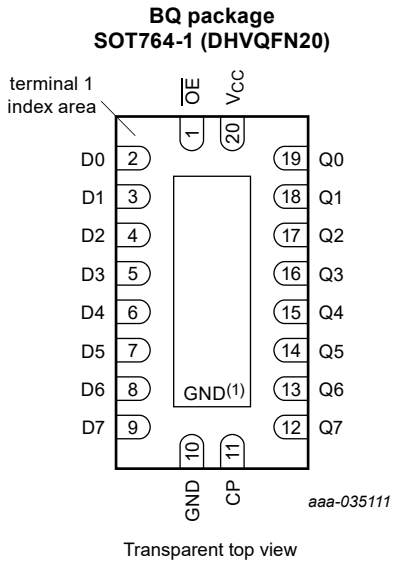


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning





Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
D0, D1, D2, D3, D4, D5, D6, D7	2, 3, 4, 5, 6, 7, 8, 9	data input
CP	11	clock input (LOW to HIGH, edge-triggered)
$\overline{OE}$	1	output enable input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	19, 18, 17, 16, 15, 14, 13, 12	3-state flip-flop output
V_{CC}	20	supply voltage
GND	10	ground (0 V)

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW to HIGH CP transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW to HIGH CP transition;
Z = high-impedance OFF-state; ↑ = LOW to HIGH clock transition.

Operating mode	Input			Internal flip-flop	Output
	$\overline{OE}$	CP	Dn		Qn
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+4.6	V
V_O	output voltage	output HIGH or LOW state [1]	-0.5	V_{CC} + 0.5	V
		output 3-state	-0.5	+4.6	V
		power-down mode; V_{CC} = 0 V	-0.5	+4.6	V
I_{IK}	input clamping current	V_I < 0 V	-50	-	mA
I_{OK}	output clamping current	V_O > V_{CC} or V_O < 0 V	-	±50	mA
I_O	output current	V_O = 0 V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.
For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.
For SOT764-1 (DHVQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	3.6	V
		power-down mode; V_{CC} = 0 V	0	3.6	V
T_{amb}	ambient temperature	in free air	-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	0.65 × V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -100 µA; V_{CC} = 1.65 V to 3.6 V	V_{CC} - 0.2	-	-	V_{CC} - 0.2	-	V
		I_O = -6 mA; V_{CC} = 1.65 V	1.25	1.51	-	1.25	-	V
		I_O = -12 mA; V_{CC} = 2.3 V	1.8	2.10	-	1.8	-	V
		I_O = -18 mA; V_{CC} = 2.3 V	1.7	2.01	-	1.7	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	2.2	2.53	-	2.2	-	V
		I_O = -18 mA; V_{CC} = 3.0 V	2.4	2.76	-	2.4	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	2.2	2.68	-	2.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.2	V
		I_O = 6 mA; V_{CC} = 1.65 V	-	0.11	0.3	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.3 V	-	0.17	0.4	-	0.4	V
		I_O = 18 mA; V_{CC} = 2.3 V	-	0.25	0.6	-	0.6	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	0.16	0.4	-	0.4	V
		I_O = 18 mA; V_{CC} = 3.0 V	-	0.23	0.4	-	0.45	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	0.30	0.55	-	0.55	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 3.6 V or GND	-	±0.1	±5	-	±20	µA

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 1.65 V to 3.6 V; V_O = 3.6 V or GND	-	±0.1	±10	-	±80	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 3.6 V	-	±0.1	±10	-	±80	µA
I_{CC}	supply current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	0.2	10	-	80	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3.0 V to 3.6 V; $V_I = V_{CC}$ - 0.6 V; I_O = 0 A	-	5	750	-	750	µA
C_I	input capacitance		-	3.5	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 8.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	CP to Qn; see Fig. 5 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.0	3.1	6.4	1.0	7.4	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.3	3.9	1.0	4.5	ns
		V_{CC} = 2.7 V	1.0	2.5	3.6	1.0	4.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.5	3.6	1.0	4.1	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Fig. 6 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.0	3.2	6.4	1.0	7.4	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.6	4.5	1.0	5.2	ns
		V_{CC} = 2.7 V	1.0	3.2	4.6	1.0	5.3	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.4	4.0	1.0	4.6	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 6 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.5	3.6	7.0	1.5	8.1	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.3	4.4	1.0	5.1	ns
		V_{CC} = 2.7 V	1.5	2.9	4.4	1.5	5.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.8	4.4	1.0	5.1	ns
t_W	pulse width	clock HIGH or LOW; see Fig. 5						
		V_{CC} = 1.65 V to 1.95 V	3.8	1.1	-	3.8	-	ns
		V_{CC} = 2.3 V to 2.7 V	3.3	0.9	-	3.3	-	ns
		V_{CC} = 2.7 V	3.3	0.8	-	3.3	-	ns
		V_{CC} = 3.0 V to 3.6 V	3.3	1.2	-	3.3	-	ns

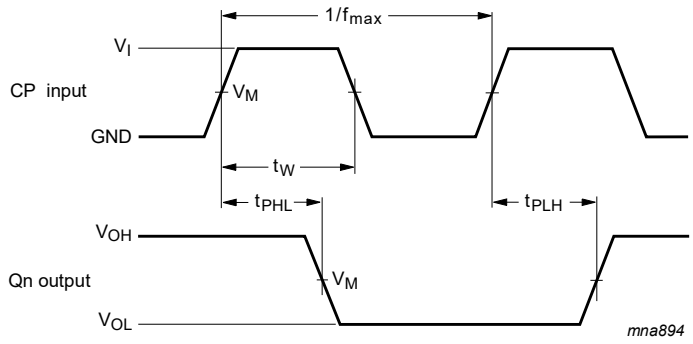
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{su}	set-up time	Dn to CP; see Fig. 7						
		V_{CC} = 1.65 V to 1.95 V	0.8	-0.1	-	0.8	-	ns
		V_{CC} = 2.3 V to 2.7 V	0.8	0.1	-	0.8	-	ns
		V_{CC} = 2.7 V	0.8	0.3	-	0.8	-	ns
		V_{CC} = 3.0 V to 3.6 V	0.8	0.0	-	0.8	-	ns
t_h	hold time	Dn to CP; see Fig. 7						
		V_{CC} = 1.65 V to 1.95 V	0.8	-0.1	-	0.8	-	ns
		V_{CC} = 2.3 V to 2.7 V	0.8	0.1	-	0.8	-	ns
		V_{CC} = 2.7 V	0.8	0.4	-	0.8	-	ns
		V_{CC} = 3.0 V to 3.6 V	0.7	-0.1	-	0.7	-	ns
f_{max}	maximum frequency	see Fig. 5						
		V_{CC} = 1.65 V to 1.95 V	50	100	-	50	-	MHz
		V_{CC} = 2.3 V to 2.7 V	100	200	-	100	-	MHz
		V_{CC} = 2.7 V	100	200	-	100	-	MHz
		V_{CC} = 3.0 V to 3.6 V	150	300	-	150	-	MHz
C_{PD}	power dissipation capacitance	per flip-flop; V_I = GND to V_{CC}; V_{CC} = 3.3 V [3]						
		outputs HIGH or LOW state	-	21	-	-	-	pF
		outputs 3-state	-	13	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
t_{en} is the same as t_{PZH} and t_{PZL}.
t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms and test circuit

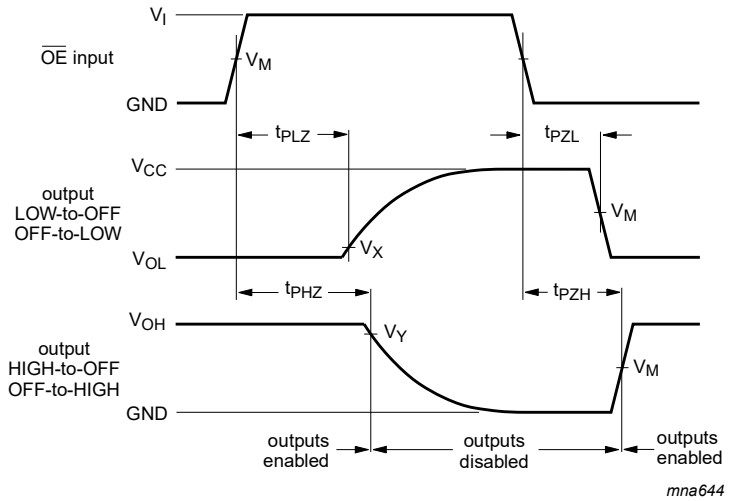


Measurement points are given in Table 8.
V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig. 5. Clock (CP) to output (Qn) propagation delays, the clock pulse width, and the maximum frequency

Table 8. Measurement points

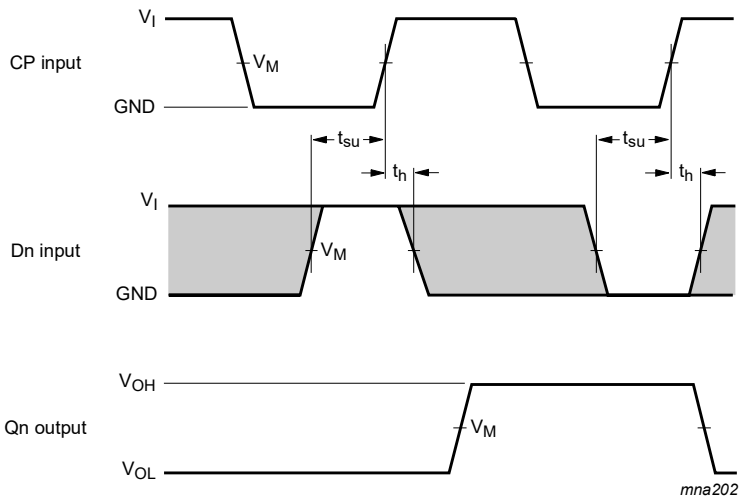
Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.3 V to 2.7 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Measurement points are given in Table 8.

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig. 6. Enable and disable times

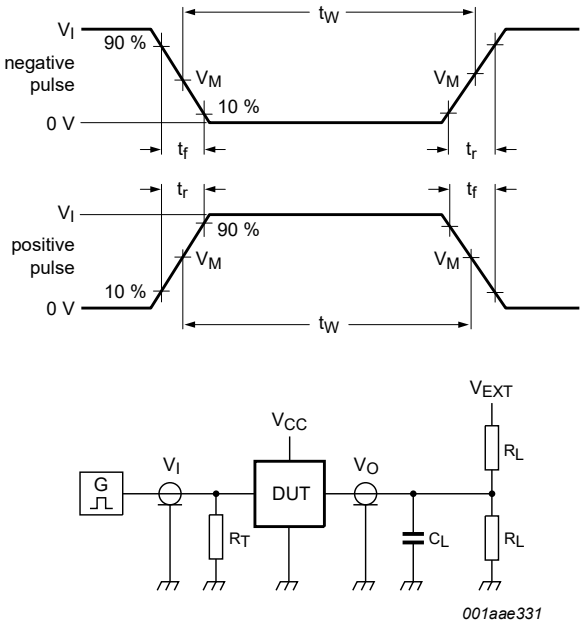


Measurement points are given in Table 8.

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predicable output performance.

Fig. 7. Data set-up and hold times for the Dn input to the CP input



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

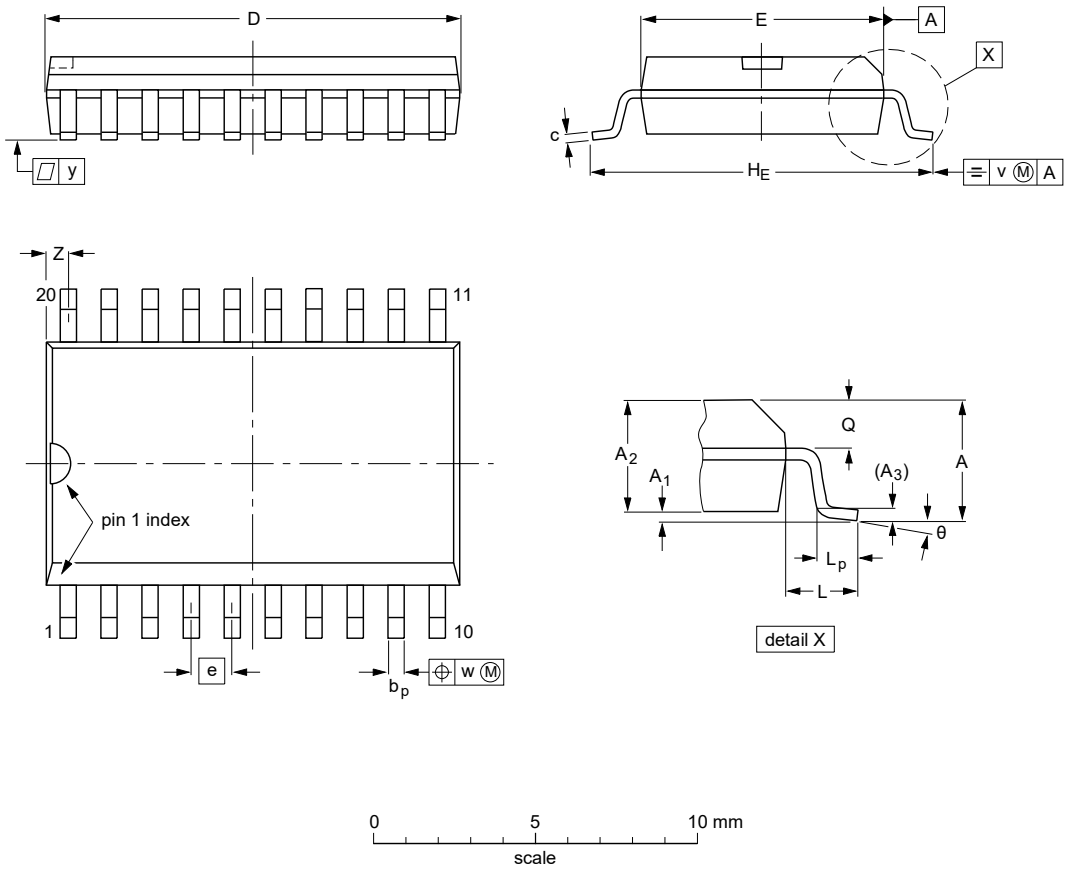
Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

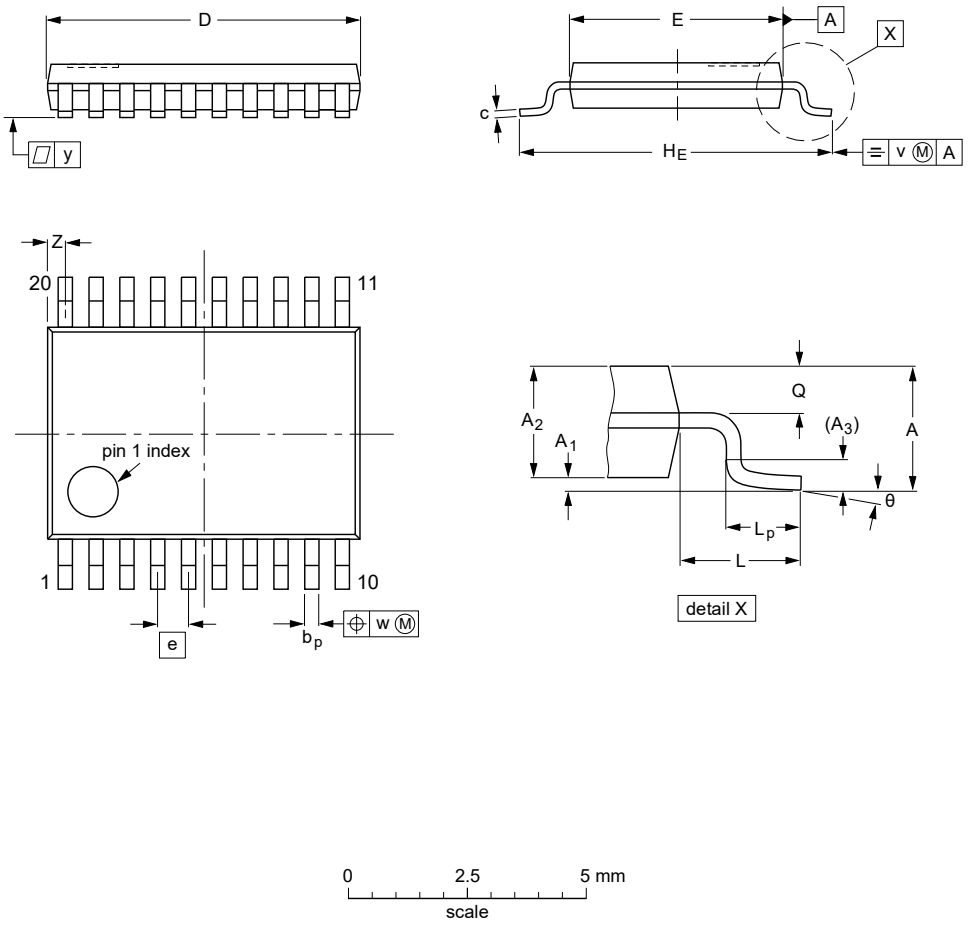
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig. 9. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

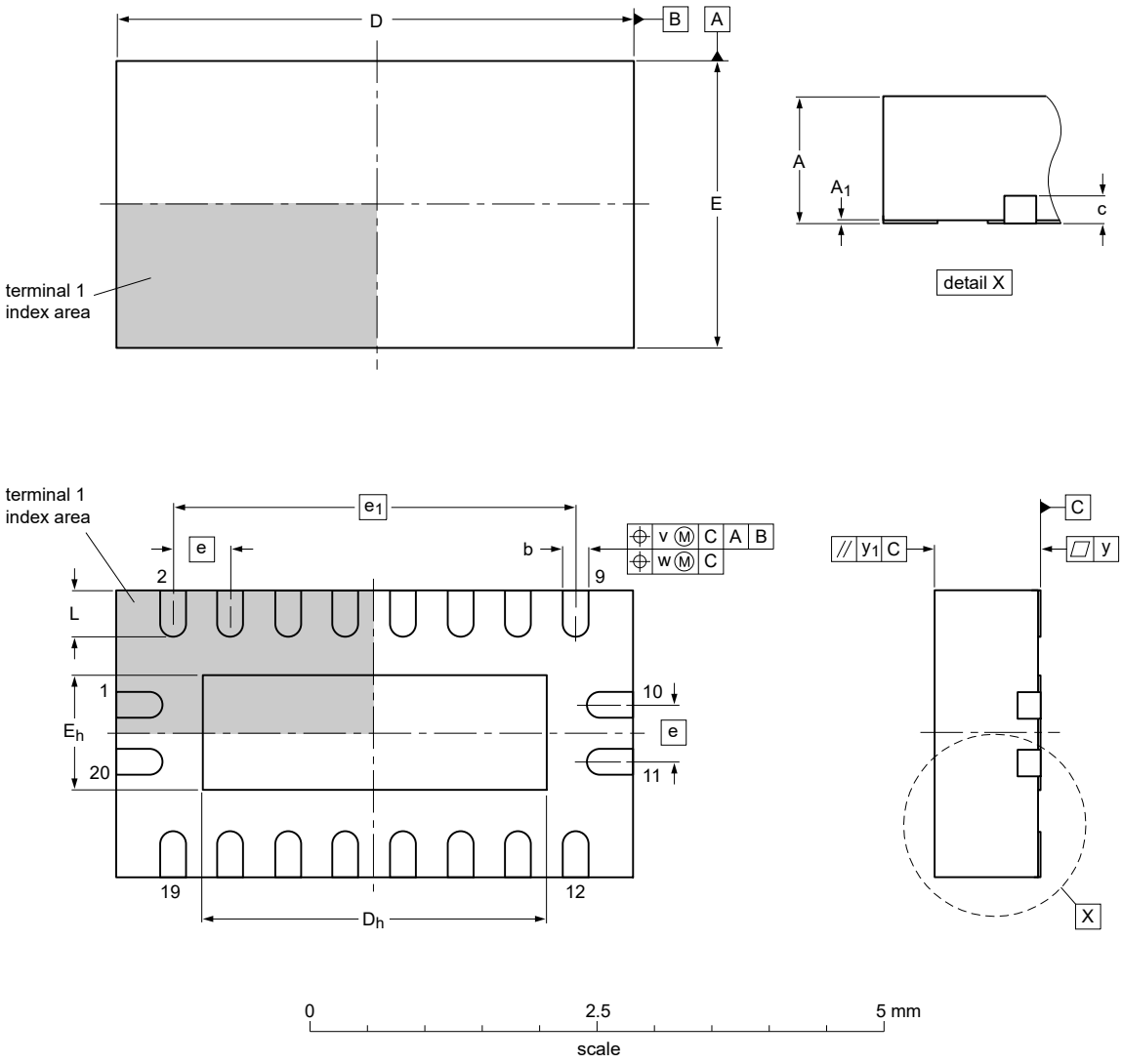
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 10. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
	max	1.00	0.05	0.30		4.6	3.15	2.6	1.15			0.5				
mm	nom	0.90	0.02	0.25	0.2	4.5	3.00	2.5	1.00	0.5	3.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		4.4	2.85	2.4	0.85			0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot764-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~03-01-27~~ 14-12-12

Fig. 11. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC574 v.4	20230711	Product data sheet	-	74ALVC574 v.3
Modifications:	• Specifications for -40 °C to +125 °C added. • Section 1 updated. • Section 2 updated; ESD specification updated according to the latest JEDEC standard.			
74ALVC574 v.3	20210430	Product data sheet	-	74ALVC574 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 2: Reference to JESD36 removed. • Section 7: Derating values for P_{tot} total power dissipation removed (errata). • Package outline drawing of SOT764-1 (Fig. 11) updated.			
74ALVC574 v.2	20071108	Product data sheet	-	74ALVC574 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 3: DHVQFN20 package added. • Section 7: derating values added for DHVQFN20 package. • Section 11: outline drawing added for DHVQFN20 package.			
74ALVC574 v.1	20020304	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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