DAVICOM Semiconductor, Inc.

DM8203 / DM8203I

10/100 Mbps 3-port Ethernet Switch Controller with MII / RMII Interface

DATASHEET

Preliminary Datasheet
Version: DM8203 / DM8203I -18-DS-M1-P01
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CONTENT

1. General Description

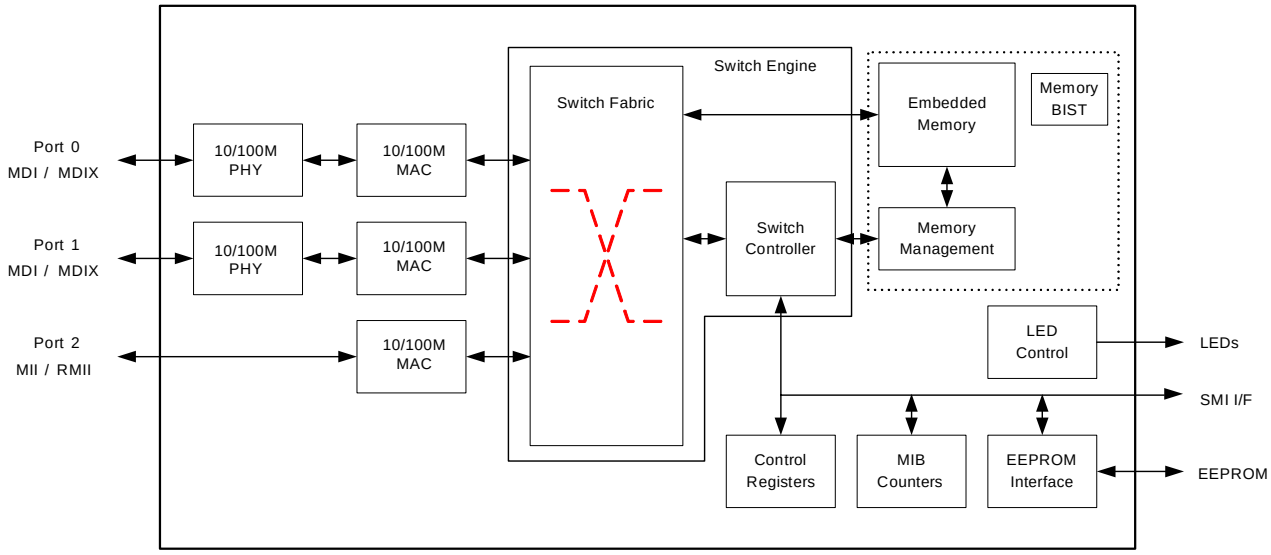
The DM8203 / DM8203I is Davicom's new fully integrated three-port 10M/100Mbps Fast Ethernet Switch Controller which supports industrial temperature with Fiber interface. As a fast Ethernet switch, the DM8203 / DM8203I consists of two PHY ports and a third port with either MII or RMII interface. As the DM8203 / DM8203I was designed with our customers' requirements in mind, the switch is optimized for high performance while being highly cost-effective.

The two PHY ports on the DM8203 / DM8203I are IEEE 802.3u standards compliant. Aside for the first two PHY ports and in an effort for maximum application flexibility, the third port on the DM8203 / DM8203I offers the options to either connect with an MII, reversed MII, or RMII. The reversed MII configuration is used to connect with SoC's with a MII interface. The RMII interface is the alternative interface configuration in case of the need to connect a lower pin count Ethernet PHY or SoC.

To maximize the performance of each port, the DM8203 / DM8203I was designed with a number of features. For proper bandwidth, each port also supports ingress and/or egress rate control. In support of efficient packet forwarding, the DM8203 / DM8203I have port-based VLAN with tag/un-tag functions for up to 16 groups of 802.1Q. Each port includes MIB counters, loop-back capability, built in memory self-test (BIST) for the system, and board level diagnostic.

In designing for the requirements of various data, voice, and video applications, enough internal memory has been provided for usage of the DM8203 / DM8203I's three ports, and the internal memory supports up to 1K uni-cast MAC address table. Then to meet the demands of various bandwidth and latency issues in data, voice, and video applications, each port of the DM8203 / DM8203I has four priority transmit queues. These queues can be defined either through port-based operation, 802.1p VLAN, or the IP packet TOS field automatically.

2. Block Diagram

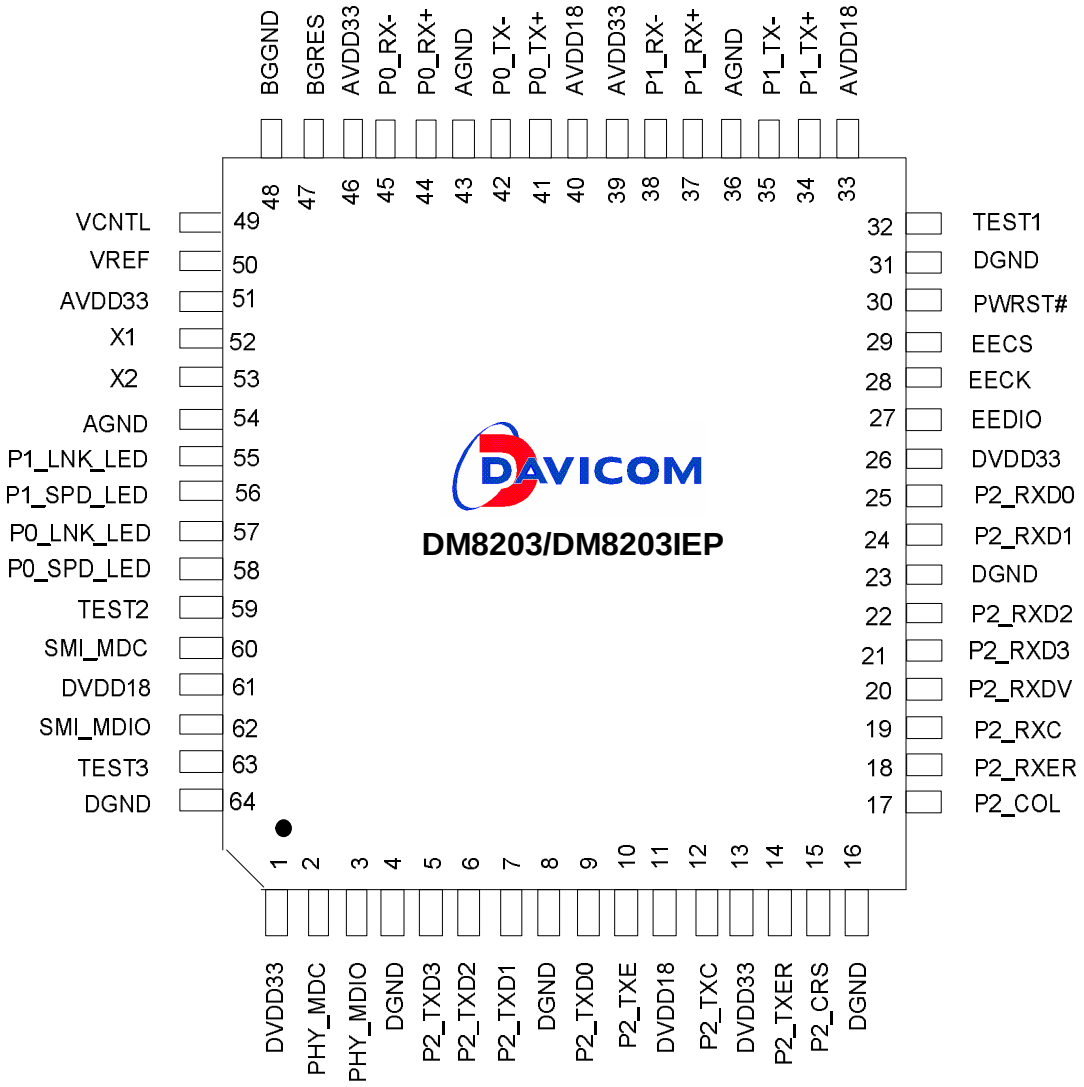


3. Features

- IEEE 802.3/u 10Base-T/100Base-TX compatible
- Ethernet Switch Ports:
  - Two 10/100Mbps PHY
  - One MII/RMII interface with Reversed - MII support
- Supports auto crossover function - HP Auto-MDIX
- Flow Control
  - Supports IEEE 802.3x Flow Control in Full-duplex mode
  - Supports Back Pressure Flow Control in Half-duplex mode
- Per port support bandwidth, ingress and egress rate control
- Per port support priority queues
  - Each port with four queues
  - Port-based, 802.1P VLAN, or IP TOS priority
- Supports 802.1Q VLAN for up-to 16 VLAN groups
- Supports VLAN ID tag/untag options
- Supports up-to 1K Unicast/Multicast shared MAC addresses
- Supports store and forward switching approach
- Supports Broadcast Storming filter function
- Supports Serial Data Management Interface
- Automatic aging scheme
- Supports MIB counters for diagnostic
- EEPROM Interface
  - Power up configurations
  - 93C46 or 93C56 auto detection
- Commercial temperature -0°C ~+70°C
- Supports industrial temperature -40°C ~+85°C (DM8203I)
- 64-pin LQFP package
- 1.8V/3.3V Dual Power supply
- 3.3V I/O with 5V tolerance

4. Pin Configuration

64 pin LQFP:



5. Pin Description

I = Input, O = Output, I/O = Input / Output, O/D = Open Drain, P = Power,
# = Asserted Low PD=internal pull-low (about 50K Ohm)

5.1 P2 MII / Reduce MII / Reverse MII

5.1.1 MII

Pin No.	Pin Name	I/O	Description
2	PHY_MDC	O,PD	MII Serial Management Data Clock
3	PHY_MDIO	I/O	MII Serial Management Data
5 6 7 9	P2_TXD3 P2_TXD2 P2_TXD1 P2_TXD0	O,PD	Port 2 MII Transmit Data 4-bit nibble data outputs (synchronous to the P2_TXC)
10	P2_TXE	O,PD	Port 2 MII Transmit Enable
12	P2_TXC	I/O	Port 2 MII Transmit Clock
14	P2_TXER	O,PD	Port 2 MII Transmit Error
15	P2_CRS	I/O	Port 2 MII Carrier Sense
17	P2_COL	I/O	Port 2 MII Collision Detect
18	P2_RXER	I	Port 2 MII Receive Error
19	P2_RXC	I	Port 2 MII Receive Clock
20	P2_RXDV	I	Port 2 MII Receive Data Valid
21 22 24 25	P2_RXD3 P2_RXD2 P2_RXD1 P2_RXD0	I	Port 2 MII Receive Data 4-bit nibble data input (synchronous to P2_RXC)

5.1.2 Reduce MII

Pin No.	Pin Name	I/O	Description
2	PHY_MDC	O,PD	MII Serial Management Data Clock
3	PHY_MDIO	I/O	MII Serial Management Data
5 6	P2_TXD3 P2_TXD2	O,PD	Not Used
7 9	P2_TXD1 P2_TXD0	O,PD	Port 2 RMII Transmit Data
10	P2_TXE	O,PD	Port 2 RMII Transmit Enable
12	P2_TXC	O	50MHz Clock Output
14	P2_TXER	O	Not Used
15	P2_CRS	I	Port 2 RMII CRS_DV
17	P2_COL	I	Not Used, tie to ground in application
18	P2_RXER	I	Not Used, tie to ground in application
19	P2_RXC	I	Port 2 RMII 50MHz Reference Clock Input
20	P2_RXDV	I	Not Used, tie to ground in application
21 22	P2_RXD3 P2_RXD2	I	Not Used, tie to ground in application
24 25	P2_RXD1 P2_RXD0	I	Port 2 RMII Receive Data

5.1.3 Reverse MII

Pin No.	Pin Name	I/O	Description
2	PHY_MDC	O,PD	Not Used
3	PHY_MDIO	I/O	Not Used
5 6 7 9	P2_TXD3 P2_TXD2 P2_TXD1 P2_TXD0	O,PD	Port 2 RevMII Transmit Data 4-bit nibble data outputs (synchronous to the P2_TXC)
10	P2_TXE	O,PD	Port 2 RevMII Transmit Enable
12	P2_TXC	O	Port 2 RevMII Transmit Clock
14	P2_TXER	O,PD	Port 2 RevMII Transmit Error
15	P2_CRS	O	Port 2 RevMII Carrier Sense Output when P2_TXE or P2_RXDV are asserted
17	P2_COL	O	Port 2 RevMII Collision Output when P2_TXE and P2_RXDV are asserted
18	P2_RXER	I	Port 2 RevMII Receive Error
19	P2_RXC	I	Port 2 RevMII Receive Clock
20	P2_RXDV	I	Port 2 RevMII Receive Data Valid
21 22 24 25	P2_RXD3 P2_RXD2 P2_RXD1 P2_RXD0	I	Port 2 RevMII Receive Data 4-bit nibble data input (synchronous to P2_RXC)

5.2 EEPROM Interface

Pin No.	Pin Name	I/O	Description
27	EEDIO	I/O	EEPROM Data In/Out
28	EECK	O,PD	EEPROM Serial Clock This pin is used as the clock for the EEPROM data transfer
29	EECS	O,PD	EEPROM Chip Selection

5.3 LED Pins

Pin No.	Pin Name	I/O	Description
55	P1_LNK_LED	O	Port 1 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY1
56	P1_SPD_LED	O	Port 1 Speed LED Its low output indicates that the internal PHY1 is operated in 100M/S, or it is floating for the 10M mode of the internal PHY1
57	P0_LNK_LED	O	Port 0 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY0
58	P0_SPD_LED	O	Port 0 Speed LED Its low output indicates that the internal PHY0 is operated in 100M/S, or it is floating for the 10M mode of the internal PHY0

5.4 Clock Interface

Pin No.	Pin Name	I/O	Description
52	X1	I	Crystal or OSC 25MHz Input
53	X2	O	Crystal 25MHz Output

5.5 Network Interface

Pin No.	Pin Name	I/O	Description
34 35	P1_TX+ P1_TX -	I/O	Port 1 TP TX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode
37 38	P1_RX+ P1_RX-	I/O	Port 1 TP RX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode
41 42	P0_TX+ P0_TX-	I/O	Port 0 TP TX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode
44 45	P0_RX+ P0_RX -	I/O	Port 0 TP RX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode
47	BGRES	I/O	Band-Gap Pin Connect a 6.8K±1% ohm resistor to BGGND in application
48	BGGND	P	Band-Gap Ground
49	VCNTL	I/O	1.8V Voltage Control
50	VREF	O	Voltage Reference Connect a 0.1uF capacitor to ground in application

5.6 Miscellaneous Pins

Pin No.	Pin Name	I/O	Description
30	PWRST#	I	Power on Reset Low active with minimum 1ms
60	SMI_MDC	I	Serial Data Management Interface Clock
62	SMI_MDIO	I/O	Serial Data Management Interface Data In/Out
32	TEST1	I,PD	Test Pin 1 Tie to DVDD33 in application
59	TEST2	I,PD	Test Pin 2 Tie to DVDD33 in application
63	TEST3	I,PD	Test Pin 3 Tie to DVDD33 in application

5.7 Power Pins

Pin No.	Pin Name	I/O	Description
1,13,26	DVDD33	P	Digital 3.3V Power
11,61	DVDD18	P	Digital 1.8V Power
4,8,16,23,31,64	DGND	P	Digital GND
39,46,51	AVDD33	P	Analog 3.3V Power
33,40	AVDD18	P	Analog 1.8V Power
36,43,54	AGND	P	Analog GND

5.8 Strap Pins Table

Pin No.	Pin Name	Description
10	P2_TXE	Port 2 Force Mode Enable 0: Port 2 is normal mode 1: Port 2 is force mode
28	EECK	Port 2 Speed Selection in Force Mode 0: Port 2 is forced in 10 Mbps mode 1: Port 2 is forced in 100 Mbps mode
29	EECS	Port 0 Fiber Mode Enable 0: Port 0 is TP mode 1: Port 0 is Fiber mode
14	P2_TXER	Port 1 Fiber Mode Enable 0: Port 1 is TP mode 1: Port 1 is Fiber mode
5 6	P2_TXD3 P2_TXD2	P2 Mode Configuration P2_TXD3 P2_TXD2 0 0 Port 2 is MII mode 0 1 Port 2 is Reverse MII mode 1 0 Port 2 is RMII mode 1 1 LFP function is enabled (Port 2 is MII mode)

Note:

1 = External pull-high with resistor 1K~10K ohm

0 = Internal pull-low (default) or External pull-low

6. PHY Registers

6.1 PHY Registers Map

PHY_ADR	REG_ADR	ABS_ADR	Register Description	Default
02h	00h	040h	Port 0 PHY Basic Mode Control Register	3100h
	01h	041h	Port 0 PHY Basic Mode Status Register	7849h
	02h	042h	Port 0 PHY Identifier 1 Register	0181h
	03h	043h	Port 0 PHY Identifier 2 Register	B8B0h
	04h	044h	Port 0 PHY Auto-negotiation Advertisement Register	01E1h
	05h	045h	Port 0 PHY Auto-negotiation Link Partner Ability Register	0000h
	06h	046h	Port 0 PHY Auto-negotiation Expansion Register	0000h
	14h	054h	Port 0 PHY Specified Configuration Register	-
	1Dh	05Dh	Port 0 PHY Power Saving Control Register	0000h
03h	00h	060h	Port 1 PHY Basic Mode Control Register	3100h
	01h	061h	Port 1 PHY Basic Mode Status Register	7849h
	02h	062h	Port 1 PHY Identifier 1 Register	0181h
	03h	063h	Port 1 PHY Identifier 2 Register	B8B0h
	04h	064h	Port 1 PHY Auto-negotiation Advertisement Register	01E1h
	05h	065h	Port 1 PHY Auto-negotiation Link Partner Ability Register	0000h
	06h	066h	Port 1 PHY Auto-negotiation Expansion Register	0000h
	14h	074h	Port 1 PHY Specified Configuration Register	-
	1Dh	07Dh	Port 1 PHY Power Saving Control Register	0000h

Note:

PHY_ADR = <PHY Address> fields of SMI frame

REG_ADR = <Register Address> fields of SMI frame

ABS_ADR = { PHY_ADR[4:0], REG_ADR[4:0] }

Key to Default
In the register description that follows, the default column takes the form:
<Access Type> / <Attribute(s)>, <Reset Value>

Where:
<Access Type>
RO = Read only, RW = Read/Write

<Attribute (s)>
SC = Self clearing, P = Value permanently set

<Reset Value>:
1 = Bit set to logic one
0 = Bit set to logic zero
* = No default value

6.2 Basic Mode Control Register (040h, 060h)

PHY_ADR	REG_ADR	ABS_ADR
02h, 03h	00h	040, 060h

Bit	Bit Name	Default	Description
15	Reset	RW/SC 0b	Reset This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed 1 = Software reset 0 = Normal operation
14	Loopback	RW 0b	Loopback Loop-back control register. When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appears at the MII receive outputs 1 = Loop-back enabled 0 = Normal operation
13	Speed selection	RW 1b	Speed Select Link speed may be selected either by this bit or by auto-negotiation. When auto-negotiation is enabled and bit 12 is set, this bit will return auto-negotiation selected medium type 1 = 100Mbps 0 = 10Mbps
12	Auto-negotiation enable	RW 1b	Auto-negotiation Enable 1 = Auto-negotiation is enabled, bit 8 and 13 will be in auto-negotiation status 0 = Auto-negotiation is disabled.
11	Power down	RW 0b	Power Down While in the power-down state, the PHY should respond to management transactions. During the transition to power-down state and while in the power-down state, the PHY should not generate spurious signals on the MII 1 = Power down 0 = Normal operation
10	Isolate	RW 0b	Isolate Force to 0 in application.
9	Restart Auto-negotiation	RW/SC 0b	Restart Auto-negotiation Re-initiates the auto-negotiation process. When auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning to a value of 1 until auto-negotiation is initiated by the DM8203 / DM8203I. The operation of the auto-negotiation process will not be affected by the management entity that clears this bit 1 = Restart auto-negotiation. 0 = Normal operation
8	Duplex mode	RW 1b	Duplex Mode Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With auto-negotiation enabled, this bit reflects the duplex capability selected by auto-negotiation 1 = Full duplex operation. 0 = Normal operation

7	Collision test	RW 0b	Collision Test When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN in internal MII interface. 1 = Collision test enabled. 0 = Normal operation
6:0	RESERVED	RO 0h	Reserved Write as 0h, ignore when read

6.3 Basic Mode Status Register (041h, 061h)

PHY_ADR	REG_ADR	ABS_ADR
02h, 03h	01h	041, 061h

Bit	Bit Name	Default	Description
15	100BASE-T4	RO/P 0b	100BASE-T4 Capable 1 = DM8203 / DM8203I is able to perform in 100BASE-T4 mode 0 = DM8203 / DM8203I is not able to perform in 100BASE-T4 mode
14	100BASE-TX full-duplex	RO/P 1b	100BASE-TX Full Duplex Capable 1 = DM8203 / DM8203I is able to perform 100BASE-TX in full duplex mode 0 = DM8203 / DM8203I is not able to perform 100BASE-TX in full duplex mode
13	100BASE-TX half-duplex	RO/P 1b	100BASE-TX Half Duplex Capable 1 = DM8203 / DM8203I is able to perform 100BASE-TX in half duplex mode 0 = DM8203 / DM8203I is not able to perform 100BASE-TX in half duplex mode
12	10BASE-T full-duplex	RO/P 1b	10BASE-T Full Duplex Capable 1 = DM8203 / DM8203I is able to perform 10BASE-T in full duplex mode 0 = DM8203 / DM8203I is not able to perform 10BASE-TX in full duplex mode
11	10BASE-T half-duplex	RO/P 1b	10BASE-T Half Duplex Capable 1 = DM8203 / DM8203I is able to perform 10BASE-T in half duplex mode 0 = DM8203 / DM8203I is not able to perform 10BASE-T in half duplex mode
10:7	RESERVED	RO 0h	Reserved Write as 0h, ignore when read
6	MF preamble suppression	RO 1b	MII Frame Preamble Suppression 1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed
5	Auto-negotiation Complete	RO 0b	Auto-negotiation Complete 1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed
4	Remote fault	RO 0b	Remote Fault 1 = Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM8203 / DM8203I implementation specific. This bit will set after the RF bit in the ANLPAR (REG 02h/03h.05h.[13]) is set

			0 = No remote fault condition detected
3	Auto-negotiation ability	RO/P 1b	Auto Configuration Ability 1 = DM8203 / DM8203I is able to perform auto-negotiation 0 = DM8203 / DM8203I is not able to perform auto-negotiation
2	Link status	RO 0b	Link Status The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface. 1 = Valid link is established (for either 10Mbps or 100Mbps operation) 0 = Link is not established
1	Jabber detect	RO 0b	Jabber Detect This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a DM8203 / DM8203I reset. This bit works only in 10Mbps mode 1 = Jabber condition detected 0 = No jabber
0	Extended capability	RO/P 1b	Extended Capability 1 = Extended register capable 0 = Basic register capable only

6.4 PHY ID Identifier Register 1 (042h, 062h)

PHY_ADR	REG_ADR	ABS_ADR
02h, 03h	02h	042h, 062h

Bit	Bit Name	Default	Description
15:0	OUI_MSB	RO 0181h	OUI Most Significant Bits This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM8203 / DM8203I. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

6.5 PHY ID Identifier Register 2 (043h, 063h)

PHY_ADR	REG_ADR	ABS_ADR
02h, 03h	03h	043h, 063h

Bit	Bit Name	Default	Description
15:10	OUI_LSB	RO/P 101110b	OUI Least Significant Bits Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
9:4	VNDR_MDL	RO/P 001011b	Vendor Model Number Five bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3:0	MDL_REV	RO/P 0001b	Model Revision Number Five bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 4)

6.6 Auto-negotiation Advertisement Register (044h, 064h)

PHY_ADR	REG_ADR	ABS_ADR
02h, 03h	04h	044h, 064h

Bit	Bit Name	Default	Description
15	NP	RO/P 0b	Next page Indication The DM8203 / DM8203I has no next page, so this bit is permanently set to 0. 0 = No next page available 1 = Next page available
14	ACK	RO 0b	Acknowledge The DM8203 / DM8203I's auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the auto-negotiation process. Software should not attempt to write to this bit. 1 = Link partner ability data reception acknowledged 0 = Not acknowledged
13	RF	RW 0b	Remote Fault 1 = Local device senses a fault condition 0 = No fault detected
12:11	RESERVED	RW 00b	Reserved Write as 00b, ignore when read
10	FCS	RW 0b	Flow Control Support 1 = Controller chip supports flow control ability 0 = Controller chip doesn't support flow control ability
9	T4	RO/P 0b	100BASE-T4 Support The DM8203 / DM8203I does not support 100BASE-T4 so this bit is permanently set to 0 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 is not supported
8	TX_FDX	RW 1b	100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the local device 0 = 100BASE-TX full duplex is not supported
7	TX_HDX	RW 1b	100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the local device 0 = 100BASE-TX half duplex is not supported
6	10_FDX	RW 1b	10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the local device 0 = 10BASE-T full duplex is not supported
5	10_HDX	RW 1b	10BASE-T Support 1 = 10BASE-T half duplex is supported by the local device 0 = 10BASE-T half duplex is not supported
4:0	Selector	RW 00001b	Protocol Selection Bits These bits contain the binary encoded protocol selector supported by this node <00001> indicates that this device supports IEEE 802.3 CSMA/CD

6.7 Auto-negotiation Link Partner Ability Register (045h, 065h)

PHY_ADR	REG_ADR	ABS_ADR
02h, 03h	05h	045h, 065h

Bit	Bit Name	Default	Description
15	NP	RO 0b	Next Page Indication 0 = Link partner, no next page available 1 = Link partner, next page available
14	ACK	RO 0b	Acknowledge The DM8203 / DM8203I's auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit 1 = Link partner ability data reception acknowledged 0 = Not acknowledged
13	RF	RO 0b	Remote Fault 1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner
12:11	RESERVED	RO 00b	Reserved Write as 00b, ignore when read
10	FCS	RO 0b	Flow Control Support 1 = Controller chip supports flow control ability by link partner 0 = Controller chip doesn't support flow control ability by link partner
9	T4	RO 0b	100BASE-T4 Support 1 = 100BASE-T4 is supported by the link partner 0 = 100BASE-T4 is not supported by the link partner
8	TX_FDX	RO 0b	100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the link partner 0 = 100BASE-TX full duplex is not supported by the link partner
7	TX_HDX	RO 0b	100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the link partner 0 = 100BASE-TX half duplex is not supported by the link partner
6	10_FDX	RO 0b	10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the link partner 0 = 10BASE-T full duplex is not supported by the link partner
5	10_HDX	RO 0b	10BASE-T Support 1 = 10BASE-T half duplex is supported by the link partner 0 = 10BASE-T half duplex is not supported by the link partner
4:0	Selector	RO 0h	Protocol Selection Bits Link partner's binary encoded protocol selector

6.8 Auto-negotiation Expansion Register (046h, 066h)

PHY_ADR	REG_ADR	ABS_ADR
02h, 03h	06h	046h, 066h

Bit	Bit Name	Default	Description
15:5	RESERVED	RO 0h	Reserved Write as 0h, ignore when read
4	PDF	RO/LH 0b	Local Device Parallel Detection Fault 1 = A fault detected via parallel detection function. 0 = No fault detected via parallel detection function
3	LP_NP_ABLE	RO 0b	Link Partner Next Page Ability 1 = Link partner, next page available 0 = Link partner, no next page
2	NP_ABLE	RO/P 0b	Local Device Next Page Ability DM8203 / DM8203I does not support this function, so this bit is always 0
1	PAGE_RX	RO 0b	New Page Received A new link code word page received. This bit will be automatically cleared when the register (register 6) is read by management
0	LP_AN_ABLE	RO 0b	Link Partner Auto-negotiation Ability A “1” in this bit indicates that the link partner supports Auto-negotiation

6.9 Specified Configuration Register (054h, 074h)

PHY_ADR	REG_ADR	ABS_ADR
02h, 03h	14h	054h, 074h

Bit	Bit Name	Default	Description
15:12	RESERVED	RW 0000b	Reserved Write as 0000b, ignore when read
11	PREAMBLEX	RW 0b	Preamble Saving Control 0 = When bit 10 is set, the 10BASE-T transmit preamble count is reduced. When REG 02h/03h.1Dh.[11] is set, 12-bit preamble is reduced; otherwise 22-bit preamble is reduced. 1 = Transmit preamble bit count is normal in 10BASE-T mode
10	TX10M_PWR	RW 0b	10BASE-T mode Transmit Power Saving Control 1 = Enable transmit power saving in 10BASE-T mode 0 = Disable transmit power saving in 10BASE-T mode
9	NWAY_PWR	RW 0b	Auto-negotiation Power Saving Control 1 = Disable power saving during auto-negotiation period 0 = Enable power saving during auto-negotiation period
8	RESERVED	RO 0b	Reserved Read as 0, ignore on write
7	MDIX_CNTL	RO *	The Polarity of MDI/MDIX value 1 = MDIX mode 0 = MDI mode
6	RESERVED	RW 0b	Reserved Write as 0b, ignore when read
5	Mdix_fix Value	RW 0b	MDIX_CNTL force value: When Mdix_down = 1, MDIX_CNTL value depend on the register value
4	Mdix_down	RW 0b	MDIX Down Manual force MDI/MDIX. MDIX_CNTL value depend on REG 02h/03h.14h.[5] 0 = Enable *HP* Auto-MDIX 1 = Disable *HP* Auto-MDIX
3:0	RESERVED	RW 0000b	Reserved Write as 0000b, ignore when read

6.10 Power Saving Control Register (05Dh, 07Dh)

PHY_ADR	REG_ADR	ABS_ADR
02h, 03h	1Dh	05Dh, 07Dh

Bit	Bit Name	Default	Description
15:12	RESERVED	RO 0000b	Reserved Write as 0000b, ignore when read
11	PREAMBLEX	RW 0b	Preamble Saving Control when both bit REG 02h/03h.14h.[11:10] are set, the 10BASE-T transmit preamble count is reduced. 1 = 12-bit preamble is reduced. 0 = 22-bit preamble is reduced.
10	RESERVED	RW 0b	Reserved Write as 0b, ignore when read
9	TX_PWR	RW 0b	Transmit Power Saving Control Disabled 1 = When cable is unconnected with link partner, the driving current of transmit is reduced for power saving. 0 = Disable transmit driving power saving function
8:0	RESERVED	RO 0h	Reserved Write as 0h, ignore when read

7. Switch Registers

7.1 Switch Registers Map

PHY_ADR	REG_ADR	ABS_ADR	Register Description	Default
08h	00h~0Fh	100h~10Fh	Reserved	-
	10h	110h	Port 0 Status Register	-
	11h	111h	Port 0 Basic Control Register 1	0000h
	12h	112h	Port 0 Basic Control Register 2	0000h
	13h	113h	Port 0 Block Control Register 1	0000h
	14h	114h	Port 0 Block Control Register 2	0000h
	15h	115h	Port 0 Bandwidth Control Register	0000h
	16h	116h	Port 0 VLAN Tag Register	0001h
	17h	117h	Port 0 Priority & VLAN Control Register	0000h
	18h	118h	Reserved	-
	19h	119h	Port 0 Advanced Control Register	0000h
	1Ah~1Fh	11Ah~11Fh	Reserved	-
09h	00h~0Fh	120~12F	Reserved	-
	10h	130h	Port 1 Status Register	0000h
	11h	131h	Port 1 Basic Control Register 1	0000h
	12h	132h	Port 1 Basic Control Register 2	0000h
	13h	133h	Port 1 Block Control Register 1	0000h
	14h	134h	Port 1 Block Control Register 2	0000h
	15h	135h	Port 1 Bandwidth Control Register	0001h
	16h	136h	Port 1 VLAN Tag Register	0000h
	17h	137h	Port 1 Priority & VLAN Control Register	-
	18h	138h	Reserved	0000h
	19h	139h	Port 1 Advanced Control Register	093Ah
	1Ah~1Fh	13Ah~13Fh	Reserved	-
0Ah	00h~0Fh	140h~14Fh	Reserved	-
	10h	150h	Port 2 Status Register	0000h
	11h	151h	Port 2 Basic Control Register 1	0000h
	12h	152h	Port 2 Basic Control Register 2	0000h
	13h	153h	Port 2 Block Control Register 1	0000h
	14h	154h	Port 2 Block Control Register 2	0000h
	15h	155h	Port 2 Bandwidth Control Register	0001h
	16h	156h	Port 2 VLAN Tag Register	0000h
	17h	157h	Port 2 Priority & VLAN Control Register	-
	18h	158h	Reserved	0000h
	19h	159h	Port 2 Advanced Control Register	093Ah
	1Ah~1Fh	15Ah~15Fh	Reserved	-
10h	00h~0Fh	200h~20Fh	Reserved	-
	10h	210h	Switch Status Register	-
	11h	211h	Switch Reset Register	0000h
	12h	212h	Switch Control Register	0000h

	13h	213h	Mirror Control Register	0000h
	15h	215h	Global Learning & Aging Control Register	0000h
	16h	216h	Reserved	-
	17h	217h	VLAN Priority Map Register	FA50h
	18h	218h	TOS Priority Map Register 1	FA50h
	19h	219h	TOS Priority Map Register 2	0000h
	1Ah	21Ah	TOS Priority Map Register 3	5555h
	1Bh	21Bh	TOS Priority Map Register 4	5555h
	1Ch	21Ch	TOS Priority Map Register 5	AAAAh
	1Dh	21Dh	TOS Priority Map Register 6	AAAAh
	1Eh	21Eh	TOS Priority Map Register 7	FFFFh
	1Fh	21Fh	TOS Priority Map Register 8	FFFFh
11h	00h~0Fh	220h~22Fh	Reserved	
	10h	230h	MIB Counter Disable Register	0000h
	11h	231h	MIB Counter Control Register	0000h
	12h	232h	MIB Counter Data Register 1	0000h
	13h	233h	MIB Counter Data Register 2	0000h
	14h~1Dh	234h~23Dh	Reserved	-
	1Eh	23Eh	VLAN Mode & Rule Control Register	0000h
	1Fh	23Fh	Reserved	-
13h	00h~0Fh	260h~26Fh	Reserved	-
	10h	270h	VLAN Table Register 0	0007h
	11h	271h	VLAN Table Register 1	0007h
	12h	272h	VLAN Table Register 2	0007h
	13h	273h	VLAN Table Register 3	0007h
	14h	274h	VLAN Table Register 4	0007h
	15h	275h	VLAN Table Register 5	0007h
	16h	276h	VLAN Table Register 6	0007h
	17h	277h	VLAN Table Register 7	0007h
	18h	278h	VLAN Table Register 8	0007h
	19h	279h	VLAN Table Register 9	0007h
	1Ah	27Ah	VLAN Table Register 10	0007h
	1Bh	27Bh	VLAN Table Register 11	0007h
	1Ch	27Ch	VLAN Table Register 12	0007h
	1Dh	27Dh	VLAN Table Register 13	0007h
	1Eh	27Eh	VLAN Table Register 14	0007h
	1Fh	27Fh	VLAN Table Register 15	0007h
18h	00h~0Fh	300h~30Fh	Reserved	-
	10h	310h	Vendor ID Register	0A46h
	12h~14h	312h~314h	Reserved	-
	15h	315h	Port 2 MAC Control Register	0100h
	16h~19h	316h~319h	Reserved	-
	1Ah	31Ah	EEPROM Control & Address Register	0040h
	1Bh	31Bh	EEPROM Data Register	0000h
	1Ch	31Ch	Strap Pin Control & Status Register	-

	1Dh~1Fh	31Dh~31Fh	Reserved	-
19h	00h~0Fh	320h~32Fh	Reserved	-
	10h~18h	330h~338h		-
	19h	339h	SMI Bus Error Check Register	0000h
	1Ah	33Ah	SMI Bus Control Register	0000h
	1Bh~1Dh	33Bh~33Dh	Reserved	-
	1Eh	33Eh	PHY Control Register	0003h
	1Fh	33Fh	Reserved	-
1Ch	00h~1Fh	380h~39Fh	Reserved	-

Key to Default

In the register description that follows, the default column takes the form:

<Access Type>, <Reset Type>, <Default Value>

Where:

<Access Type>:
RO = Read only
RW = Read/Write
R/C = Read and Clear
RW/C1=Read/Write and Cleared by write 1
WO = Write only
Reserved bits should be written with 0
Reserved bits are undefined on read access

<Reset Type>
P = Register will be set to default value after hardware reset (Power-ON Reset) is de-asserted
S = Register will be set to default value after software reset (Write REG 10h.11h.[0] to 1) is done
E = The value reflect upon EEPROM setting
T = The value reflect upon strap pin setting

<Default Value>:
1 = Logic one
0 = Logic zero
* = No default value

7.2 Per Port Switch Register

7.2.1 Per Port Status Register (110h, 130h, 150h)

PHY_ADR	REG_ADR	ABS_ADR
08h, 09h, 0Ah	10h	110h, 130h, 150h

Bit	ROM	Type	Default	Description
15:5	---	RO	0h	RESERVED Write as 0h, ignore when read
4	---	P, RO	*	LP_FCS Link Partner Flow Control Support Status 0: Link partner don't support IEEE 802.3x flow control 1: Link partner support IEEE 802.3x flow control
3	---	RO	0b	RESERVED Write as 0b, ignore when read
2	---	P, RO	*	SPEED Port Speed Status 0: 10Mbps 1: 100Mbps
1	---	P, RO	*	FDX Port Duplex Status 0: Half-duplex 1: Full-duplex
0	---	P, RO	*	LINK Port Link Status 0: Link Off 1: Link On

7.2.2 Per Port Basic Control Register 1 (111h, 131h, 151h)

PHY_ADR	REG_ADR	ABS_ADR
08h, 09h, 0Ah	11h	111h, 131h, 151h

Bit	ROM	Type	Default	Description
15	---	RO	0b	RESERVED Write as 0b, ignore when read
14	80h.[14] 90h.[14] A0h.[14]	PSE,RW	0b	UNPLUG_CLS Unplug Clear Address Enable Automatically clear address record in address table after cable is unplugged 0: Disable, retaining address record 1: Enable, clearing address record
13	80h.[13] 90h.[13] A0h.[13]	PSE,RW	0b	AGE_DIS Address Table Aging 0: Age function is enabled 1: Age function is disabled
12	80h.[12] 90h.[12] A0h.[12]	PSE,RW	0b	ADR_DIS Address Learning Disabled 0: Address learning function is enabled 1: Address learning function is disabled

11	80h.[11] 90h.[11] A0h.[11]	PSE,RW	0b	DIS_PAUSE Maximum Pause Packet from Link Partner 0: Always care pause packet from link partner 1: Pause packet by passed after 7 continued pause packet from link partner
10	---	RO	0b	RESERVED Write as 0b, ignore when read
9	80h.[9] 90h.[9] A0h.[9]	PSE,RW	0b	HOLBP_EN Head-of-Line Blocking Prevent Control 0: Disable 1: Enable
8	80h.[8] 90h.[8] A0h.[8]	PSE,RW	0b	LOOPBACK Loop-Back Mode The transmitted packet will be forward to this port itself 0: Look-back is disabled 1: Look-back is enabled
7	80h.[7] 90h.[7] A0h.[7]	PSE,RW	0b	PAUSE_CON Send PAUSE Continuously If buffer congestion occur on full duplex, switch will send PAUSE frames: 0: Up to 8-times 1: Continuously until alleviation
6	80h.[6] 90h.[6] A0h.[6]	PSE,RW	0b	PARTI_EN Partition Detection Enable 0: Disable 1: Enable
5	80h.[5] 90h.[5] A0h.[5]	PSE,RW	0b	FCBP_DIS Backpressure Flow-Control in Half Duplex Disable 0: Backpressure is enabled 1: Backpressure is disabled
4	80h.[4] 90h.[4] A0h.[4]	PSE,RW	0b	FC3X_DIS IEEE 802.3x Flow Control in Full Duplex Mode 0: 802.3x flow-control is enabled 1: 802.3x flow-control is disabled
3:2	80h.[3:2] 90h.[3:2] A0h.[3:2]	PSE,RW	00b	MAX_PKTLEN[1:0] Max accept packet length by RX from this port 00: 1536-bytes 01: 1552-bytes 10: 1800-bytes 11: 2032-bytes
1	80h.[1] 90h.[1] A0h.[1]	PSE,RW	0b	RX_DIS Packet Receive Disable 0: Receive ability is enabled 1: Receive ability is disabled
0	80h.[0] 90h.[0] A0h.[0]	PSE,RW	0b	TX_DIS Packet Transmit Disable 0: Transmit ability is enabled 1: Transmit ability is disabled

7.2.3 Per Port Basic Control Register 2 (112h, 132h, 152h)

PHY_ADR	REG_ADR	ABS_ADR
08h, 09h, 0Ah	12h	112h, 132h, 152h

Bit	ROM	Type	Default	Description
15	81h.[15] 91h.[15] A1h.[15]	PSE,RW	0b	NO_DIS_RX Not Discard RX Packets when Ingress Bandwidth Control When received packets bandwidth reach Ingress bandwidth threshold, the packets over the threshold are not discarded but with flow control.
14	81h.[14] 91h.[14] A1h.[14]	PSE,RW	0b	BANDWIDTH Bandwidth Control Mode 0: Separate mode. Bandwidth control with ingress and egress is separated, the threshold defined in REG 08/09/0Ah.15h.[15:8] 1: Combined mode. Bandwidth control with ingress or egress is combined, the threshold defined in REG 08/09/0Ah.15h.[3:0]
13	81h.[13] 91h.[13] A1h.[13]	PSE,RW	0b	STORM_UUP Broadcast Storm Enable for Unlearned Unicast Packets 0: Disable 1: Enable
12	81h.[12] 91h.[12] A1h.[12]	PSE,RW	0b	STORM_MP Broadcast Storm Filtering for Multicast Packets Treat multicast packet as source of storm 0: Disable 1: Enable
11	81h.[11] 91h.[11] A1h.[11]	PSE,RW	0b	MIRR_DBP Don't Mirror Broadcast/Multicast Packets If Mirror Function is Enabled 0: Broadcast/Multicast would be mirrored 1: Broadcast/Multicast would not be mirrored
10:9	---	RO	00b	RESERVED Write as 00b, ignore when read
8	81h.[8] 91h.[8] A1h.[8]	PSE,RW	0b	FIR_UUDMAC Filter Packets with Unlearned Unicast DMAC 0: Disable 1: Enable
7	81h.[7] 91h.[7] A1h.[7]	PSE,RW	0b	FIR_UMDMAC Filter Packets with Unlearned Multicast DMAC 0: Disable 1: Enable
6	81h.[6] 91h.[6] A1h.[6]	PSE,RW	0b	FIR_BDMAC Filter Packets with Broadcast DMAC 0: Disable 1: Enable
5	81h.[5] 91h.[5] A1h.[5]	PSE,RW	0b	FIR_MDMAC Filter Packets with Multicast DMAC 0: Disable 1: Enable
4	81h.[4] 91h.[4] A1h.[4]	PSE,RW	0b	FIR_MSMAC Filter Packets with Multicast SMAC 0: Disable 1: Enable

3	---	RO	0b	RESERVED Write as 0b, ignore when read
2	81h.[2] 91h.[2] A1h.[2]	PSE,RW	0b	MIRR_TX TX Packet is Mirrored. The received packets are also forward to sniffer port. 0: Don't mirror 1: All transmitted packets is mirrored
1	---	RO	0b	RESERVED Write as 0b, ignore when read
0	81h.[0] 91h.[0] A1h.[0]	PSE,RW	0b	MIRR_RX RX Packet is Mirrored. The received packets are also forward to sniffer port. 0: Don't mirror 1: All received packets is mirrored

7.2.4 Per Port Block Control Register 1 (113h, 133h, 153h)

PHY_ADR	REG_ADR	ABS_ADR
08h, 09h, 0Ah	13h	113h, 133h, 153h

Bit	ROM	Type	Default	Description
15:11	---	RO	0h	RESERVED Write as 0h, ignore when read
10:8	82h.[10:8] 92h.[10:8] A2h.[10:8]	PSE,RW	000b	BLK_MP[2:0] Block Packet with Multicast DMAC [10]: Block such packet forward to port 2 [09]: Block such packet forward to port 1 [08]: Block such packet forward to port 0 0: Disable 1: Enable
7:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	82h.[2:0] 92h.[2:0] A2h.[2:0]	PSE,RW	000b	BLK_BP[2:0] Block Packet with Broadcast DMAC [02]: Block such packet forward to port 2 [01]: Block such packet forward to port 1 [00]: Block such packet forward to port 0 0: Disable 1: Enable

7.2.5 Per Port Block Control Register 2 (114h, 134h, 154h)

PHY_ADR	REG_ADR	ABS_ADR
08h, 09h, 0Ah	14h	114h, 134h, 154h

Bit	ROM	Type	Default	Description
15:11	---	RO	0h	RESERVED Write as 0h, ignore when read
10:8	83h.[10:8] 93h.[10:8] A3h.[10:8]	PSE,RW	000b	BLK_UKP[2:0] Block Packet with Unlearned Unicast DMAC [10]: Block such packet forward to port 2 [09]: Block such packet forward to port 1 [08]: Block such packet forward to port 0 0: Disable 1: Enable
7:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	83h.[2:0] 93h.[2:0] A3h.[2:0]	PSE,RW	000b	BLK_UP[2:0] Block Packet with Unicast DMAC The received unicast packets are not forward to the assigned ports. [02]: Block such packet forward to port 2 [01]: Block such packet forward to port 1 [00]: Block such packet forward to port 0 0: Disable 1: Enable

7.2.6 Per Port Bandwidth Control Register (115h, 135h, 155h)

PHY_ADR	REG_ADR	ABS_ADR
08h, 09h, 0Ah	15h	115h, 135h, 155h

Bit	ROM	Type	Default	Description
15:12	84h.[15:12] 94h.[15:12] A4h.[15:12]	PSE,RW	0000b	INGRESS[3:0] Ingress Rate Control (Separated mode) These bits define the bandwidth threshold that received packets over the threshold are discarded. 0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps
11:8	84h.[11:8] 94h.[11:8] A4h.[11:8]	PSE,RW	0000b	EGRESS[3:0] Egress Rate Control These bits define the bandwidth threshold that transmitted packets over the threshold are discarded. 0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps

7:4	84h.[7:4] 94h.[7:4] A4h.[7:4]	PSE,RW	0000b	BSTH[3:0] Broadcast Storm Threshold These bits define the bandwidth threshold that received broadcast packets over the threshold are discarded 0000: no broadcast storm control 0001: 8K packets/sec 0010: 16K packets/sec 0011: 64K packets/sec 0100: 5% 0101: 10% 0110: 20% 0111: 30% 1000: 40% 1001: 50% 1010: 60% 1011: 70% 1100: 80% 1101: 90% 111X: no broadcast storm control
3:0	84h.[3:0] 94h.[3:0] A4h.[3:0]	PSE,RW	0000b	BW_CTRL[3:0] Ingress and Egress Rate Control (Combined mode) Received and Transmitted Bandwidth Control These bits define the bandwidth threshold that transmitted or received packets over the threshold are discarded 0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps

7.2.7 Per Port VLAN Tag Register (116h, 136h, 156h)

PHY_ADR	REG_ADR	ABS_ADR
08h, 09h, 0Ah	16h	116h, 136h, 156h

Bit	ROM	Type	Default	Description
15:13	85h.[15:13] 95h.[15:13] A5h.[15:13]	PSE,RW	000b	PPRI[2:0] Port VLAN Priority
12	85h.[12] 95h.[12] A5h.[12]	PSE,RW	0b	PCFI Port VLAN CFI
11:0	85h.[11:0] 95h.[11:0] A5h.[11:0]	PSE,RW	001h	PVID[11:0] Port VLAN Identification

7.2.8 Per Port Priority & VLAN Control Register (117h, 137h, 157h)

PHY_ADR	REG_ADR	ABS_ADR
08h, 09h, 0Ah	17h	117h, 137h, 157h

Bit	ROM	Type	Default	Description
15	---	RO	0b	RESERVED Write as 0b, ignore when read
14	86h.[14] 96h.[14] A6h.[14]	PSE,RW	0b	TAG_OUT Output Packet Tagging Enable The transmitted packets are containing VLAN tagged field 0: Disable 1: Enable
13	86h.[13] 96h.[13] A6h.[13]	PSE,RW	0b	FIR_VIPORT Enable to Filter Packet with Incoming Port is Non-member in VLAN 0: Disable 1: Enable
12	86h.[12] 96h.[12] A6h.[12]	PSE,RW	0b	NOTAG_IN Input Force No Tag Assume all received frame are untagged 0: Disable 1: Enable
11:10	---	RO	00b	RESERVED Write as 00b, ignore when read
9:8	86h.[9:8] 96h.[9:8] A6h.[9:8]	PSE,RW	00b	VLAN_IAC[1:0] VLAN Ingress Admit Control 00: Accept all frames 01: Accept VLAN-tagged frames only Untagged or priority tagged(VID=0) frames will be dropped 10: Accept untagged frames only 11: Accept frame's VID equal to ingress PVID
7	---	RO	0b	RESERVED Write as 0b, ignore when read

6	86h.[6] 96h.[6] A6h.[6]	PSE,RW	0b	PRI_DIS Priority Queue Disable Only one transmit queue is supported in this port 0: Priority Queue is enabled 1: Priority Queue is disabled
5	86h.[5] 96h.[5] A6h.[5]	PSE,RW	0b	WRR_EN Priority Scheduling Algorithm 0: Strict Priority Queuing(SPQ) 1: Weighted Round Robin(WRR)
4	86h.[4] 96h.[4] A6h.[4]	PSE,RW	0b	TOS_PRI Priority Classification IP ToS over VLAN If a IP packet with VLAN tag, the priority of this packet is decode from ToS field. 0: Priority Classification base on VLAN 1: Priority Classification base on IP ToS
3	86h.[3] 96h.[3] A6h.[3]	PSE,RW	0b	TOS_OFF IP ToS Priority Classification Disable 0: Classification is enabled 1: Classification is disabled
2	86h.[2] 96h.[2] A6h.[2]	PSE,RW	0b	PRI_OFF VLAN Priority Classification Disable 0: Classification is enabled 1: Classification is disabled
1:0	86h.[1:0] 96h.[1:0] A6h.[1:0]	PSE,RW	00b	P_PRI[1:0] Port-based Priority Queue Number 00: Queue 0 01: Queue 1 10: Queue 2 11: Queue 3

7.3 Global Switch Register

7.3.1 Switch Status Register (210h)

PHY_ADR	REG_ADR	ABS_ADR
10h	10h	210h

Bit	ROM	Type	Default	Description
15:2	---	RO	0h	RESERVED Write as 0h, ignore when read
1	---	PS, RO	*	BIST_1 Top-Memory BIST Status 0: Pass 1: Fail
0	---	PS, RO	*	BIST_0 Packet-Memory BIST Status 0: Pass 1: Fail

7.3.2 Switch Reset Register (211h)

PHY_ADR	REG_ADR	ABS_ADR
10h	11h	211h

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2	---	P, RW	0b	PD_ANLG Power down all analog PHY
1	---	P, RW	0b	RST_ANLG Analog PHY Core Reset Auto clear after 10us
0	---	P, RW	0b	RST_SW Switch Core Reset Auto clear after 10us

7.3.3 Switch Control Register (212h)

PHY_ADR	REG_ADR	ABS_ADR
10h	12h	212h

Bit	ROM	Type	Default	Description
15:6	---	RO	0h	RESERVED Write as 0h, ignore when read
5	12h.[5]	PSE,RW	0b	FDX_FLOW Flow Control Option When set In full duplex mode, if link partner's flow control capability is disabled, the flow control of DM8203 / DM8203I corresponding port is also disabled. When this is "0", the flow control is controlled by REG 08~0Ah.11h.[4].
4:3	---	RO	00b	RESERVED Write as 00b, ignore when read
2	12h.[2]	PSE,RW	0b	DIS_CRCC CRC Checking Disable 0: CRC checking is enabled 1: CRC checking is disabled
1:0	---	RO	00b	RESERVED Write as 00b, ignore when read

7.3.4 Mirror Control Register (213h)

PHY_ADR	REG_ADR	ABS_ADR
10h	13h	213h

Bit	ROM	Type	Default	Description
15:11	---	RO	0h	RESERVED Write as 0h, ignore when read
10	13h.[10]	PSE, RW	0b	MIRR_PAIR Mirror RX/TX Pair Mode Enable 0: Disable (default) 1: Enable
9:8	---	RO	00b	RESERVED Write as 00b, ignore when read
4:3	13h.[4:3]	PSE, RW	00b	SNF_PORT[1 :0] Sniffer Port Number 00: Sniffer Port is Port 0 01: Sniffer Port is Port 1 10: Sniffer Port is Port 2 11: Reserved
2:0	---	RO	000b	RESERVED Write as 000b, ignore when read

7.3.5 Global Learning & Aging Control Register (215h)

PHY_ADR	REG_ADR	ABS_ADR
10h	15h	215h

Bit	ROM	Type	Default	Description
15:6	---	RO	0h	RESERVED Write as 0h, ignore when read
5	15h.[5]	PSE,RW	0b	LRN_PAUSE Learn PAUSE Frame 0: Disable (default) 1: Enable
4	15h.[4]	PSE,RW	0b	LRN_VLAN Address Learning Consider VLAN Member 0: Address learning despite VLAN member (default) 1: Address learning is disable, if incoming port doesn't exist in its member set.
3:2	---	RO	00b	RESERVED Write as 00b, ignore when read
1:0	15h.[1:0]	PSE,RW	00b	AGE_TIME[1:0] Aging Time Value 00: 512 sec 01: 256 sec 10: 128 sec 11: 64 sec

7.3.6 VLAN Priority Map Register (217h)

PHY_ADR	REG_ADR	ABS_ADR
10h	17h	217h

Bit	ROM	Type	Default	Description
15:14	1Ch.[15:14]	PSE,RW	11b	VLAN_PM7[1:0] VLAN tag priority value = 07h
13:12	1Ch.[13:12]	PSE,RW	11b	VLAN_PM6[1:0] VLAN tag priority value = 06h
11:10	1Ch.[11:10]	PSE,RW	10b	VLAN_PM5[1:0] VLAN tag priority value = 05h
9:8	1Ch.[9:8]	PSE,RW	10b	VLAN_PM4[1:0] VLAN tag priority value = 04h
7:6	1Ch.[7:6]	PSE,RW	01b	VLAN_PM3[1:0] VLAN tag priority value = 03h
5:4	1Ch.[5:4]	PSE,RW	01b	VLAN_PM2[1:0] VLAN tag priority value = 02h
3:2	1Ch.[3:2]	PSE,RW	00b	VLAN_PM1[1:0] VLAN tag priority value = 01h
1:0	1Ch.[1:0]	PSE,RW	00b	VLAN_PM0[1:0] VLAN tag priority value = 00h

7.3.7 TOS Priority Map Register 1 (218h)

PHY_ADR	REG_ADR	ABS_ADR
10h	18h	218h

Bit	ROM	Type	Default	Description
15:14	1Dh.[15:14]	PSE,RW	11b	TOS_PM07[1:0] TOS value = 07h
13:12	1Dh.[13:12]	PSE,RW	11b	TOS_PM06[1:0] TOS value = 06h
11:10	1Dh.[11:10]	PSE,RW	10b	TOS_PM05[1:0] TOS value = 05h
9:8	1Dh.[9:8]	PSE,RW	10b	TOS_PM04[1:0] TOS value = 04h
7:6	1Dh.[7:6]	PSE,RW	01b	TOS_PM03[1:0] TOS value = 03h
5:4	1Dh.[5:4]	PSE,RW	01b	TOS_PM02[1:0] TOS value = 02h
3:2	1Dh.[3:2]	PSE,RW	00b	TOS_PM01[1:0] TOS value = 01h
1:0	1Dh.[1:0]	PSE,RW	00b	TOS_PM00[1:0] TOS value = 00h

7.3.8 TOS Priority Map Register 2 (219h)

PHY_ADR	REG_ADR	ABS_ADR
10h	19h	219h

Bit	ROM	Type	Default	Description
15:14	1Eh.[15:14]	PSE,RW	00b	TOS_PM0F[1:0] TOS value = 0Fh
13:12	1Eh.[13:12]	PSE,RW	00b	TOS_PM0E[1:0] TOS value = 0Eh
11:10	1Eh.[11:10]	PSE,RW	00b	TOS_PM0D[1:0] TOS value = 0Dh
9:8	1Eh.[9:8]	PSE,RW	00b	TOS_PM0C[1:0] TOS value = 0Ch
7:6	1Eh.[7:6]	PSE,RW	00b	TOS_PM0B[1:0] TOS value = 0Bh
5:4	1Eh.[5:4]	PSE,RW	00b	TOS_PM0A[1:0] TOS value = 0Ah
3:2	1Eh.[3:2]	PSE,RW	00b	TOS_PM09[1:0] TOS value = 09h
1:0	1Eh.[1:0]	PSE,RW	00b	TOS_PM08[1:0] TOS value = 08h

7.3.9 TOS Priority Map Register 3 (21Ah)

PHY_ADR	REG_ADR	ABS_ADR
10h	1Ah	21Ah

Bit	ROM	Type	Default	Description
15:14	1Fh.[15:14]	PSE,RW	01b	TOS_PM17[1:0] TOS value = 17h
13:12	1Fh.[13:12]	PSE,RW	01b	TOS_PM16[1:0] TOS value = 16h
11:10	1Fh.[11:10]	PSE,RW	01b	TOS_PM15[1:0] TOS value = 15h
9:8	1Fh.[9:8]	PSE,RW	01b	TOS_PM14[1:0] TOS value = 14h
7:6	1Fh.[7:6]	PSE,RW	01b	TOS_PM13[1:0] TOS value = 13h
5:4	1Fh.[5:4]	PSE,RW	01b	TOS_PM12[1:0] TOS value = 12h
3:2	1Fh.[3:2]	PSE,RW	01b	TOS_PM11[1:0] TOS value = 11h
1:0	1Fh.[1:0]	PSE,RW	01b	TOS_PM10[1:0] TOS value = 10h

7.3.10 TOS Priority Map Register 4 (21Bh)

PHY_ADR	REG_ADR	ABS_ADR
10h	1Bh	21Bh

Bit	ROM	Type	Default	Description
15:14	20h.[15:14]	PSE,RW	01b	TOS_PM1F[1:0] TOS value = 1Fh
13:12	20h.[13:12]	PSE,RW	01b	TOS_PM1E[1:0] TOS value = 1Eh
11:10	20h.[11:10]	PSE,RW	01b	TOS_PM1D[1:0] TOS value = 1Dh
9:8	20h.[9:8]	PSE,RW	01b	TOS_PM1C[1:0] TOS value = 1Ch
7:6	20h.[7:6]	PSE,RW	01b	TOS_PM1B[1:0] TOS value = 1Bh
5:4	20h.[5:4]	PSE,RW	01b	TOS_PM1A[1:0] TOS value = 1Ah
3:2	20h.[3:2]	PSE,RW	01b	TOS_PM19[1:0] TOS value = 19h
1:0	20h. [1:0]	PSE,RW	01b	TOS_PM18[1:0] TOS value = 18h

7.3.11 TOS Priority Map Register 5 (21Ch)

PHY_ADR	REG_ADR	ABS_ADR
10h	1Ch	21Ch

Bit	ROM	Type	Default	Description
15:14	21h.[15:14]	PSE,RW	10b	TOS_PM27[1:0] TOS value = 27h
13:12	21h.[13:12]	PSE,RW	10b	TOS_PM26[1:0] TOS value = 26h
11:10	21h.[11:10]	PSE,RW	10b	TOS_PM25[1:0] TOS value = 25h
9:8	21h.[9:8]	PSE,RW	10b	TOS_PM24[1:0] TOS value = 24h
7:6	21h.[7:6]	PSE,RW	10b	TOS_PM23[1:0] TOS value = 23h
5:4	21h.[5:4]	PSE,RW	10b	TOS_PM22[1:0] TOS value = 22h
3:2	21h.[3:2]	PSE,RW	10b	TOS_PM21[1:0] TOS value = 21h
1:0	21h.[1:0]	PSE,RW	10b	TOS_PM20[1:0] TOS value = 20h

7.3.12 TOS Priority Map Register 6 (21Dh)

PHY_ADR	REG_ADR	ABS_ADR
10h	1Dh	21Dh

Bit	ROM	Type	Default	Description
15:14	22h.[15:14]	PSE,RW	10b	TOS_PM2F[1:0] TOS value = 2Fh
13:12	22h.[13:12]	PSE,RW	10b	TOS_PM2E[1:0] TOS value = 2Eh
11:10	22h.[11:10]	PSE,RW	10b	TOS_PM2D[1:0] TOS value = 2Dh
9:8	22h.[9:8]	PSE,RW	10b	TOS_PM2C[1:0] TOS value = 2Ch
7:6	22h.[7:6]	PSE,RW	10b	TOS_PM2B[1:0] TOS value = 2Bh
5:4	22h.[5:4]	PSE,RW	10b	TOS_PM2A[1:0] TOS value = 2Ah
3:2	22h.[3:2]	PSE,RW	10b	TOS_PM29[1:0] TOS value = 29h
1:0	22h.[1:0]	PSE,RW	10b	TOS_PM28[1:0] TOS value = 28h

7.3.13 TOS Priority Map Register 7 (21Eh)

PHY_ADR	REG_ADR	ABS_ADR
10h	1Eh	21Eh

Bit	ROM	Type	Default	Description
15:14	23h.[15:14]	PSE,RW	11b	TOS_PM37[1:0] TOS value = 37h
13:12	23h.[13:12]	PSE,RW	11b	TOS_PM36[1:0] TOS value = 36h
11:10	23h.[11:10]	PSE,RW	11b	TOS_PM35[1:0] TOS value = 35h
9:8	23h.[9:8]	PSE,RW	11b	TOS_PM34[1:0] TOS value = 34h
7:6	23h.[7:6]	PSE,RW	11b	TOS_PM33[1:0] TOS value = 33h
5:4	23h.[5:4]	PSE,RW	11b	TOS_PM32[1:0] TOS value = 32h
3:2	23h.[3:2]	PSE,RW	11b	TOS_PM31[1:0] TOS value = 31h
1:0	23h.[1:0]	PSE,RW	11b	TOS_PM30[1:0] TOS value = 30h

7.3.14 TOS Priority Map Register 8 (21Fh)

PHY_ADR	REG_ADR	ABS_ADR
10h	1Fh	21Fh

Bit	ROM	Type	Default	Description
15:14	24h.[15:14]	PSE,RW	11b	TOS_PM3F[1:0] TOS value = 3Fh
13:12	24h.[13:12]	PSE,RW	11b	TOS_PM3E[1:0] TOS value = 3Eh
11:10	24h.[11:10]	PSE,RW	11b	TOS_PM3D[1:0] TOS value = 3Dh
9:8	24h.[9:8]	PSE,RW	11b	TOS_PM3C[1:0] TOS value = 3Ch
7:6	24h.[7:6]	PSE,RW	11b	TOS_PM3B[1:0] TOS value = 3Bh
5:4	24h.[5:4]	PSE,RW	11b	TOS_PM3A[1:0] TOS value = 3Ah
3:2	24h.[3:2]	PSE,RW	11b	TOS_PM39[1:0] TOS value = 39h
1:0	24h.[1:0]	PSE,RW	11b	TOS_PM38[1:0] TOS value = 38h

7.3.15 MIB Counter Disable Register (230h)

PHY_ADR	REG_ADR	ABS_ADR
11h	10h	230h

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	16h.[2:0]	PSE,RW	000b	MIB_DIS[2:0] Per-Port MIB Counter Disable [2] Port2 MIB counter disabled [1] Port1 MIB counter disabled [0] Port0 MIB counter disabled 0: Enable 1: Disable

7.3.16 MIB Counter Control Register (231h)

PHY_ADR	REG_ADR	ABS_ADR
11h	11h	231h

Bit	ROM	Type	Default	Description
15	---	PS,RO	0b	MIB_READY Counter Data is Ready
14:10	---	RO	0h	RESERVED Write as 0h, ignore when read
9:8	---	PS,RW	00b	MIB_CMD[1:0] Command 00: Clear after read 01: Read only 10: Clear specified port 11: Clear all ports
7	---	RO	0b	RESERVED Write as 0b, ignore when read
6:5	---	PS,RW	00b	MIB_PORT[1:0] Port Index (0~2)
4:0	---	PS,RW	00000b	MIB_OFFSET[4:0] Counter Offset (0~9)

7.3.17 MIB Counter Data Register 1 (232h)

PHY_ADR	REG_ADR	ABS_ADR
11h	12h	232h

Bit	ROM	Type	Default	Description
15:0	---	PS,RW	0h	MIB_DL[15:0] Counter Data Low Byte (Bit 15:00)

7.3.18 MIB Counter Data Register 2 (233h)

PHY_ADR	REG_ADR	ABS_ADR
11h	13h	233h

Bit	ROM	Type	Default	Description
15:0	---	PS,RW	0h	MIB_DH[15:0] Counter Data High Byte(Bit 31:16)

MIB Counter (OFFSET 00h): RX Byte Counter Register

MIB Counter (OFFSET 01h): RX Uni-cast Packet Counter Register

MIB Counter (OFFSET 02h): RX Multi-cast Packet Counter Register

MIB Counter (OFFSET 03h): RX Discard Packet Counter Register

MIB Counter (OFFSET 04h): RX Error Packet Counter Register

MIB Counter (OFFSET 05h): TX Byte Counter Register

MIB Counter (OFFSET 06h): TX Uni-cast Packet Counter Register

MIB Counter (OFFSET 07h): TX Multi-cast Packet Counter Register

MIB Counter (OFFSET 08h): TX Discard Packet Counter Register

MIB Counter (OFFSET 09h): TX Error Packet Counter Register

7.3.19 VLAN Mode & Rule Control Register (23Eh)

PHY_ADR	REG_ADR	ABS_ADR
11h	1Eh	23Eh

Bit	ROM	Type	Default	Description
15	31h.[15]	PSE,RW	0b	FIR_VIDFFF Drop Packet with VID==0xFFF Enable Drop incoming packet, if its VID is equal to 0xFFF 0: Disable 1: Enable
14	31h.[14]	PSE,RW	0b	FIR_CFI Drop Packet with Nonzero CFI Enable Drop incoming packet, if the CFI field is not equal to zero. 0: Disable 1: Enable
13:9	---	RO	0h	RESERVED Write as 0h, ignore when read
8	31h.[8]	PSE,RW	0b	QINQ_EN VLAN Stacking Enable (QinQ) 0: Disable 1: Enable
7	31h.[7]	PSE,RW	0b	TOS6 Full IP ToS Field for Priority Queue 0: check most significant 3-bit only of TOS 1: check most significant 6-bit of TOS
6	---	RO	0b	RESERVED Write as 0b, ignore when read
5	31h.[5]	PSE,RW	0b	UCROSS Unicast Packet Can Across VLAN Boundary 0: Unicast packet obeys VLAN rule 1: Unicast packet can across VLAN boundary
4	31h.[4]	PSE,RW	0b	VIDFFF Replace VID = 0xFFF When receive a VLAN tagged packet and VID equals to “0xFFF”, the outgoing packet's VID will be replaced by PVID. 0: Disable 1: Enable
3	31h.[3]	PSE,RW	0b	VID1 When receive a VLAN tagged packet and VID equals to “0x001”, the outgoing packet's VID will be replaced by PVID. 0: Disable 1: Enable
2	31h.[2]	PSE,RW	0b	VID0 Replace VID = 0x000 When receive a VLAN tagged packet and VID equals to “0x000”, the outgoing packet's VID will be replaced by PVID. 0: Disable 1: Enable

1	31h.[1]	PSE,RW	0b	VLAN_RPRI Replace VLAN Priority Replace the received packet's VLAN priority by REG 08h/09h/0Ah.16h.[15:13] 0: Disable 1: Enable
0	31h.[0]	PSE,RW	0b	VLAN Mode Selection 0: Port-based VLAN 1: Tag-based VLAN

7.3.20 VLAN Table Register 0 (270h)

PHY_ADR	REG_ADR	ABS_ADR
13h	10h	270h

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	43h.[2:0]	PSE,RW	111b	VTAB_VMB0[2:0] VLAN Entry 0 VLAN Member

7.3.21 VLAN Table Register 1 (271h)

PHY_ADR	REG_ADR	ABS_ADR
13h	11h	271h

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	44h.[2:0]	PSE,RW	111b	VTAB_VMB1[2:0] VLAN Entry 1 VLAN Member

7.3.22 VLAN Table Register 2 (272h)

PHY_ADR	REG_ADR	ABS_ADR
13h	12h	272h

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	45h.[2:0]	PSE,RW	111b	VTAB_VMB2[2:0] VLAN Entry 2 VLAN Member

7.3.23 VLAN Table Register 3 (273h)

PHY_ADR	REG_ADR	ABS_ADR
13h	13h	273h

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	46h.[2:0]	PSE,RW	111b	VTAB_VMB3[2:0] VLAN Entry 3 VLAN Member

7.3.24 VLAN Table Register 4 (274h)

PHY_ADR	REG_ADR	ABS_ADR
13h	14h	274h

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	47h.[2:0]	PSE,RW	111b	VTAB_VMB4[2:0] VLAN Entry 4 VLAN Member

7.3.25 VLAN Table Register 5 (275h)

PHY_ADR	REG_ADR	ABS_ADR
13h	15h	275h

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	48h.[2:0]	PSE,RW	111b	VTAB_VMB5[2:0] VLAN Entry 5 VLAN Member

7.3.26 VLAN Table Register 6 (276h)

PHY_ADR	REG_ADR	ABS_ADR
13h	16h	276h

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	49h.[2:0]	PSE,RW	111b	VTAB_VMB6[2:0] VLAN Entry 6 VLAN Member

7.3.27 VLAN Table Register 7 (277h)

PHY_ADR	REG_ADR	ABS_ADR
13h	17h	277h

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	4Ah.[2:0]	PSE,RW	111b	VTAB_VMB7[2:0] VLAN Entry 7 VLAN Member

7.3.28 VLAN Table Register 8 (278h)

PHY_ADR	REG_ADR	ABS_ADR
13h	18h	278h

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	4Bh.[2:0]	PSE,RW	111b	VTAB_VMB8[2:0] VLAN Entry 8 VLAN Member

7.3.29 VLAN Table Register 9 (279h)

PHY_ADR	REG_ADR	ABS_ADR
13h	19h	279h

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	4Ch.[2:0]	PSE,RW	111b	VTAB_VMB9[2:0] VLAN Entry 9 VLAN Member

7.3.30 VLAN Table Register 10 (27Ah)

PHY_ADR	REG_ADR	ABS_ADR
13h	1Ah	27Ah

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	4Dh.[2:0]	PSE,RW	111b	VTAB_VMB10[2:0] VLAN Entry 10 VLAN Member

7.3.31 VLAN Table Register 11 (27Bh)

PHY_ADR	REG_ADR	ABS_ADR
13h	1Bh	27Bh

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	4Eh.[2:0]	PSE,RW	111b	VTAB_VMB11[2:0] VLAN Entry 11 VLAN Member

7.3.32 VLAN Table Register 12 (27Ch)

PHY_ADR	REG_ADR	ABS_ADR
13h	1Ch	27Ch

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	4Fh.[2:0]	PSE,RW	111b	VTAB_VMB12[2:0] VLAN Entry 12 VLAN Member

7.3.33 VLAN Table Register 13 (27Dh)

PHY_ADR	REG_ADR	ABS_ADR
13h	1Ch	27Dh

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	50h.[2:0]	PSE,RW	111b	VTAB_VMB13[2:0] VLAN Entry 13 VLAN Member

7.3.34 VLAN Table Register 14 (27Eh)

PHY_ADR	REG_ADR	ABS_ADR
13h	1Eh	27Eh

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	51h.[2:0]	PSE,RW	111b	VTAB_VMB14[2:0] VLAN Entry 14 VLAN Member

7.3.35 VLAN Table Register 15 (27Fh)

PHY_ADR	REG_ADR	ABS_ADR
13h	1Fh	27Fh

Bit	ROM	Type	Default	Description
15:3	---	RO	0h	RESERVED Write as 0h, ignore when read
2:0	52h.[2:0]	PSE,RW	111b	VTAB_VMB15[2:0] VLAN Entry 15 VLAN Member

7.3.36 Vendor ID Register (310h)

PHY_ADR	REG_ADR	ABS_ADR
18h	10h	310h

Bit	ROM	Type	Default	Description
15:0	04H.[15:0]	PE,RO	0A46h	VID[15:0] Vendor ID

7.3.37 EEPROM Control & Address Register (31Ah)

PHY_ADR	REG_ADR	ABS_ADR
18h	1Ah	31Ah

Bit	ROM	Type	Default	Description
15:8	---	PS,RW	0h	EROA[7:0] EEPROM Word Address
7	---	RO	0b	RESERVED Write as 0b, ignore when read
6	---	P,RW	1b	EETYPE EEPROM Type 0: 93C46 1: 93C56/66(Default)
5	---	PS,RW	0b	REEP Reload EEPROM. User needs to clear it up after the operation completes
4	---	PS,RW	0b	WEP Write EEPROM Enable 0: EEPROM write operation is disabled 1: EEPROM write operation is enabled
3	---	PS,RW	0b	EPOS External PHY Operation Select 0: Select EEPROM 1: Select External PHY
2	---	PS,RW	0b	ERPRR EEPROM Read Command User needs to clear it up after the operation completes
1	---	PS,RW	0b	ERPRW EEPROM Write Command User needs to clear it up after the operation completes
0	---	PS,RO	0b	ERRE EEPROM or PHY Access Status 0: Idle 1: EEPROM or PHY access is in progress

7.3.38 EEPROM Data Register (31Bh)

PHY_ADR	REG_ADR	ABS_ADR
18h	1Bh	31Bh

Bit	ROM	Type	Default	Description
15:0	---	PS,RW	0h	EE_DATA[15:0] EEPROM 16bit Data

7.3.39 Strap Pin Control & Status Register (31Ch)

PHY_ADR	REG_ADR	ABS_ADR
18h	1Ch	31Ch

Bit	ROM	Type	Default	Description
15	---	PT,RO	*	H_TEST3 hard-strap TEST3 * The default value depend on the pin, TEST3
14	---	PT,RO	*	H_TEST2 hard-strap TEST2 * The default value depend on the pin, TEST2
13	---	PT,RO	*	H_TEST1 hard-strap TEST1 * The default value depend on the pin, TEST1
12	---	RW	---	RESERVED Write as 0b, ignore when read
11	---	RO	---	RESERVED Write as 0b, ignore when read
10	---	PT,RO	*	H_EECS hard-strap EECS * The default value depend on the strap pin, EECS
9	---	PT,RO	*	H_EECK hard-strap EECK * The default value depend on the strap pin, EECK
8:6	---	RO	---	RESERVED Write as 000b, ignore when read
5	---	PT,RW	*	HS_TXER2 hard-strap/soft-strap P2_TXER * The default value depend on the strap pin, P2_TXER
4	---	PT,RW	*	HS_TXE2 hard-strap/soft-strap P2_TXE * The default value depend on the strap pin, P2_TXE
3	---	PT,RW	*	HS_TXD23 hard-strap/soft-strap P2_TXD3 * The default value depend on the strap pin, P2_TXD3
2	---	PT,RW	*	HS_TXD22 hard-strap/soft-strap P2_TXD2 * The default value depend on the strap pin, P2_TXD2
1:0	---	RW	---	RESERVED Write as 0b, ignore when read

Note
1. The default value of Hard-strap in REG 18h.1Ch depends on each pins' strap setting when power-on reset, refer to the section 5.8 Strap Pins Table for more detail.
2. The Hard-strap's setting can be overridden via Soft-strap (REG 18h.1Ch.[5:0]). The updated setting will be applied until software reset is asserted (write REG 10h.11h.[0] to 1).

7.3.40 SMI Bus Error Check Register (339h)

PHY_ADR	REG_ADR	ABS_ADR
19h	19h	339h

Bit	ROM	Type	Default	Description
15:9	--	RO	0h	RESERVED Write as 0h, ignore when read
8	---	PS,RO	0b	SMI_ERR SMI Bus Error Status(Read only) 0: Checksum check correct 1: Checksum check error
7:0	---	PS,RW	0h	SMI_CSUM[7:0] SMI Bus Command Checksum Calculated checksum value by HW

7.3.41 SMI Bus Control Register (33Ah)

PHY_ADR	REG_ADR	ABS_ADR
19h	1Ah	33Ah

Bit	ROM	Type	Default	Description
15:1	---	RO	0h	RESERVED Write as 0h, ignore when read
0	---	P,RW	0b	SMI_ECE SMI Bus Error Check Enable 0: Disable 1: Enable

7.3.42 PHY Control Register (33Eh)

PHY_ADR	REG_ADR	ABS_ADR
19h	1Eh	33Eh

Bit	ROM	Type	Default	Description
15	07h.[15]	PSE,RW	0b	MDIX_DIS_P0 Port0 Auto-MDIX Control 0: Auto_MDIX Enable 1: Auto_MDIX Disable
14	07h. [14]	PSE,RW	0b	MDIX_DIS_P1 Port1 Auto-MDIX Control 0: Auto_MDIX Enable 1: Auto_MDIX Disable
13:9	---	RO	0h	RESERVED Write as 0h, ignore when read
8	07h. [8]	PSET,RW	0b	Reserved
7:4	---	RO	0h	RESERVED Write as 0h, ignore when read
3:0	---	PS,RW	3h	I_TUNE_TX[3:0] TX Operation Current To tune the TX operation current

Note:
There are two method to control Auto-MDIX ability on each port, Switch REG 19h.1Eh.[15:14] and per-port's PHY REG 02h/03h.14h.[4]. For instance, we can control port 0's Auto-MDIX ability by:

Auto-MDIX	Switch REG 19h.1Eh.[15]	Port 0's PHY REG 02h.14h.[4]
Enable	0	0
Disable	1	Don't care
Disable	Don't care	1

8. EEPROM Format

Name	Word	Description
Signature	00h	When this word is 1049h, the EEPROM data is valid and can be loaded to DM8203 / DM8203I.
RESERVED	01h~02h	Reserved Set to "0000h" in application
Load Control 0	03h	Bit [01:00] = Load enable of word 04h & 05h 01b: Enable, 00b/10b/11b: Disable Bit [03:02] = Reserved Set to "00b" or "11b" in application Bit [05:04] = Load enable of word 07h 01b: Enable, 00b/10b/11b: Disable Bit [07:06] = Load enable of word 09h & 0Ah 01b: Enable, 00b/10b/11b: Disable Bit [09:08] = Load enable of word 0Dh 01b: Enable, 00b/10b/11b: Disable Bit [11:10] = Reserved Set to "00b" or "11b" in application Bit [13:12] = Reserved Set to "00b" or "11b" in application Bit [15:14] = Reserved Set to "00b" or "11b" in application
Vendor ID	04h	2 byte vendor ID (Default: 0A46h) If bit [1:0] of word 03h is "01b", Bit [15:0] will be loaded to REG 18h.10h
Product ID	05h	2 byte product ID (Default: 8603h) If bit [1:0] of word 03h is "01b", Bit [15:0] will be loaded to REG 18h.11h
RESERVED	06h	Reserved Set to "0000h" in application
RESERVED	08h	Reserved Set to "0000h" in application
PHY Vendor ID	09h	2 byte PHY ID1 If bit [7:6] of word 03h is "01b", Bit[15:0] will be loaded to PHY Vendor ID.
PHY Device ID	0Ah	2 byte PHY ID2 If bit [7:6] of word 03h is "01b", Bit[15:0] will be loaded to PHY Device ID.
RESERVED	0Bh~0Ch	Reserved Set to "0000h" in application
Port 2 MAC Control	0Dh	Port 2 MAC Control If bit [9:8] of word 03h is "01b", Bit [15:0] will be loaded to REG 18h.15h
Load Control 1	0Eh	Bit [01:00] = Load enable of word 12h ~ 16h 01b: Enable, 00b/10b/11b: Disable Bit [03:02] = Load enable of word 17h &18h 01b: Enable, 00b/10b/11b: Disable Bit [05:04] = Load enable of word 1Ch ~ 24h 01b: Enable, 00b/10b/11b: Disable Bit [07:06] = Reserved Set to "00b" or "11b" in application

		Bit [09:08] = Load enable of word 31h ~ 52h 01b: Enable, 00b/10b/11b: Disable Bit [11:10] = Reserved Set to “00b” or “11b” in application Bit [13:12] = Reserved Set to “00b” or “11b” in application Bit [15:14] = Reserved Set to “00b” or “11b” in application
Load Control 2	0Fh	Bit [01:00] = Load enable of word 80h ~ 8Ah 01b: Enable, 00b/10b/11b: Disable Bit [03:02] = Load enable of word 90h ~ 9Ah 01b: Enable, 00b/10b/11b: Disable Bit [05:04] = Load enable of word A0h ~ AAh 01b: Enable, 00b/10b/11b: Disable Bit [07:06] = Reserved Set to “00b” or “11b” in application Bit [09:08] = Reserved Set to “00b” or “11b” in application Bit [11:10] = Reserved Set to “00b” or “11b” in application Bit [13:12] = Reserved Set to “00b” or “11b in application Bit [15:14] = Reserved Set to “00b” or “11b” in application
RESERVED	10h~11h	Reserved Set to “0000h” in application
Switch Control	12h	If bit [01:00] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 10h.12h
Mirror Control	13h	If bit [01:00] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 10h.13h
Global Learning & Aging Control	15h	If bit [01:00] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 10h.15h
MIB Counter Disable	16h	If bit [01:00] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 11h.10h
RESERVED	19h~1Bh	Reserved Set to “0000h” in application
VLAN Priority Map Register	1Ch	If bit [05:04] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 10h.17h
TOS Priority Map 0	1Dh	If bit [05:04] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 10h.18h
TOS Priority Map 1	1Eh	If bit [05:04] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 10h.19h
TOS Priority Map 2	1Fh	If bit [05:04] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 10h.1Ah
TOS Priority Map 3	20h	If bit [05:04] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 10h.1Bh
TOS Priority Map 4	21h	If bit [05:04] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 10h.1Ch
TOS Priority Map 5	22h	If bit [05:04] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 10h.1Dh
TOS Priority Map 6	23h	If bit [05:04] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 10h.1Eh
TOS Priority Map 7	24h	If bit [05:04] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 10h.1Fh

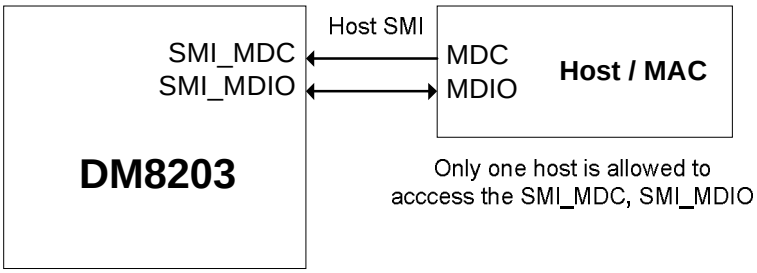
RESERVED	25h~30h	Reserved Set to “0000h” in application
VLAN Mode & Rule Control	31h	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 11h.1Eh
RESERVED	32h~42h	Reserved Set to “0000h” in application
VLAN Table - MEMBER_0H	43h	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.10h
VLAN Table - MEMBER_1H	44h	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.11h
VLAN Table - MEMBER_2H	45h	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.12h
VLAN Table - MEMBER_3H	46h	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.13h
VLAN Table - MEMBER_4H	47h	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.14h
VLAN Table - MEMBER_5H	48h	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.15h
VLAN Table - MEMBER_6H	49h	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.16h
VLAN Table - MEMBER_7H	4Ah	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.17h
VLAN Table - MEMBER_8H	4Bh	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.18h
VLAN Table - MEMBER_9H	4Ch	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.19h
VLAN Table - MEMBER_AH	4Dh	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.1Ah
VLAN Table - MEMBER_BH	4Eh	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.1Bh
VLAN Table - MEMBER_CH	4Fh	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.1Ch
VLAN Table - MEMBER_DH	50h	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.1Dh
VLAN Table - MEMBER_EH	51h	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.1Eh
VLAN Table - MEMBER_FH	52h	If bit [09:08] of word 0Eh is “01b”, Bit [15:00] will be loaded to REG 13h.1Fh
RESERVED	53h~7Fh	Reserved Set to “0000h” in application
P0 Basic Control 0	80h	If bit [01:00] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 08h.11h
P0 Basic Control 1	81h	If bit [01:00] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 08h.12h
P0 Block Control 0	82h	If bit [01:00] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 08h.13h
P0 Block Control 1	83h	If bit [01:00] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 08h.14h
P0 Bandwidth Control	84h	If bit [01:00] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 08h.15h
P0 VLAN Tag Information	85h	If bit [01:00] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 08h.16h
P0 Priority & VLAN	86h	If bit [01:00] of word 0Fh is “01b”,

Control		Bit [15:00] will be loaded to REG 08h.17h
RESERVED	87h 89h~8Ah 8Bh~8Fh	Reserved Set to “0000h” in application
P1 Basic Control 0	90h	If bit [03:02] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 09h.11h
P1 Basic Control 1	91h	If bit [03:02] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 09h.12h
P1 Block Control 0	92h	If bit [03:02] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 09h.13h
P1 Block Control 1	93h	If bit [03:02] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 09h.14h
P1 Bandwidth Control	94h	If bit [03:02] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 09h.15h
P1 VLAN Tag Information	95h	If bit [03:02] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 09h.16h
P1 Priority & VLAN Control	96h	If bit [03:02] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 09h.17h
RESERVED	97h 99h~9Ah 9Bh~9Fh	Reserved Set to “0000h” in application
P2 Basic Control 0	A0h	If bit [05:04] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 0Ah.11h
P2 Basic Control 1	A1h	If bit [05:04] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 0Ah.12h
P2 Block Control 0	A2h	If bit [05:04] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 0Ah.13h
P2 Block Control 1	A3h	If bit [05:04] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 0Ah.14h
P2 Bandwidth Control	A4h	If bit [05:04] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 0Ah.15h
P2 VLAN Tag Information	A5h	If bit [05:04] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 0Ah.16h
P2 Priority & VLAN Control	A6h	If bit [05:04] of word 0Fh is “01b”, Bit [15:00] will be loaded to REG 0Ah.17h
RESERVED	A7h	Reserved Set to “0000h” in application
RESERVED	A9h~AAh	Reserved Set to “0000h” in application
RESERVED	ABh~FFh	Reserved Set to “0000h” in application

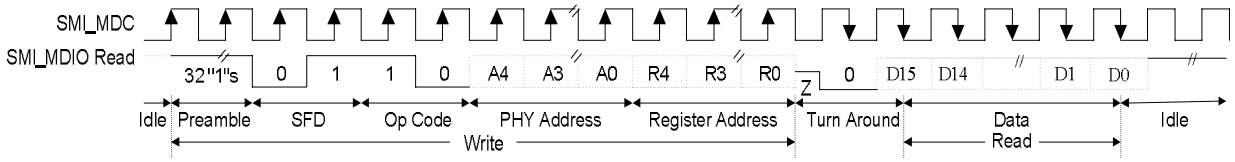
9. Functional Description

9.1 Host Serial Management Interface

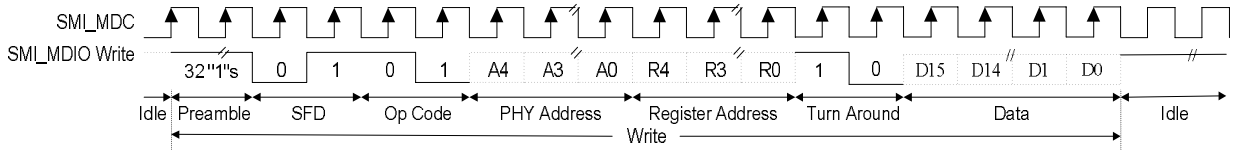
9.1.1 Host SMI Frame Structure



Host SMI - Read Frame Structure



Host SMI - Write Frame Structure



The Host SMI consists of two pins, one is SMI_MDC and another is SMI_MDIO. User can access DM8203 / DM8203I's EEPROM, PHY registers, MIB counters and Configuration registers through Host SMI. The format is following. The <PHY Address> and <Register Address> fields of the frame are mapped to address of PHY register and Switch register set of DM8203 / DM8203I.

9.1.2 Host SMI Bus Error Check Function

Because SMI bus tends to be interfered by noise on board-level. This function is used to check the command validity to suppress the mistaken command. In write procedure, the written value in register will be applied until the correct checksum is written (error proofing) and user can read status for validation (error detecting). In read procedure, user can compare hardware calculated checksum with software calculated one to validate the result.

For example:

- Write Procedure

  (1). Set REG 19h.1Ah.[0] = 1 to enable SMI Bus Error Check function

  (2). Write data to DM8203 / DM8203I's register (general write command)

  (3). CPU calculate checksum (CSUM[7:0]) and write it to REG 19h.19h.[7:0]

  (4). Check function status REG 19h.19h.[8]

- Read Procedure

  (1). Set REG 19h.1Ah.[0] = 1 to enable SMI Bus Error Check function

  (2). Read data from DM8203 / DM8203I's register (general read command)

  (3). Read hardware calculated checksum from REG 19h.19h.[7:0] and compare it with CPU calculated one (CSUM[7:0])

Checksum calculate formula:

CSUM[0] = D[0] ^ D[8] ^ R[0] ^ A[3]
CSUM[1] = D[1] ^ D[9] ^ R[1] ^ A[4]
CSUM[2] = D[2] ^ D[10] ^ R[2] ^ OP[0]
CSUM[3] = D[3] ^ D[11] ^ R[3] ^ OP[1]
CSUM[4] = D[4] ^ D[12] ^ R[4]
CSUM[5] = D[5] ^ D[13] ^ A[0]
CSUM[6] = D[6] ^ D[14] ^ A[1]
CSUM[7] = D[7] ^ D[15] ^ A[2]

Note:

D[15:0] = <Data> field of SMI frame
R[4:0] = <Register Address> field of SMI frame
A[4:0] = <PHY Address> field of SMI frame
OP[1:0] = <Op Code> field of SMI frame

9.2 Switch Functions

9.2.1 Address Learning

The DM8203 / DM8203I has a self-learning mechanism for learning the MAC addresses of incoming packets in real time. DM8203 / DM8203I stores MAC addresses, port number and time stamp information in the Hash-based Address Table. It can learn up to 1K unicast address entries.

The switch engine updates address table with new entry if incoming packet's Source Address (SA) does not exist and incoming packet is valid (non-error and legal length).

Besides, DM8203 / DM8203I has an option to disable address learning for individual port. This feature can be set by REG 08h/09h/0Ah.11h.[12].

9.2.2 Address Aging

The time stamp information of address table is used in the aging process. The switch engine updates time stamp whenever the corresponding SA receives. The switch engine would delete the entry if its time stamp is not updated for a period of time. The period can be programmed or disabled through REG 10h.15h.[1:0].

9.2.3 Packet Forwarding

The DM8203 / DM8203I forwards the incoming packet according to following decision:

- If DA is Multicast/Broadcast, the packet is forwarded to all ports, except to the port on which the packet was received.
- Switch engine would look up address table based on DA when incoming packets is UNICAST. If the DA was not found in address table, the packet is treated as a multicast packet and forward to other ports. If the DA was found and its destination port number is different to source port number, the packet is forward to destination port.
- Switch engine also look up VLAN, Port Monitor setting and other forwarding constraints for the forwarding decision, more detail will discuss in later sections.

The DM8203 / DM8203I will filter incoming packets under following conditions:

- Error packets, including CRC errors, alignment errors, illegal size errors.
- PAUSE packets.
- If incoming packet is UNICAST and its destination port number is equal to source port number.

9.2.4 Inter-Packet Gap (IPG)

IPG is the idle time between any two valid packets at the same port. The typical number is 96 bits time. In other word, the value is 9.6u sec for 10Mbps and 960n sec for 100Mbps.

9.2.5 Back-off Algorithm

The DM8203 / DM8203I implements the binary exponential back-off algorithm in half-duplex mode compliant to IEEE standard 802.3.

9.2.6 Late Collision

Late Collision is a type of collision. If a collision error occurs after the first 512 bit times of data are transmitted, the packet is dropped.

9.2.7 Full Duplex Flow Control

The DM8203 / DM8203I supports IEEE standard 802.3x flow control frames on both transmit and receive sides. On the receive side, The DM8203 / DM8203I will defer transmitting next normal frames, if it receives a pause frame from link partner. On the transmit side, The DM8203 / DM8203I issues pause frame with maximum pause time when internal resources such as received buffers, transmit queue and transmit descriptor ring are unavailable. Once resources are available, The DM8203 / DM8203I sends out a pause frame with zero pause time allows traffic to resume immediately.

9.2.8 Half Duplex Flow Control

The DM8203 / DM8203I supports half-duplex backpressure. The inducement is the same as full duplex mode. When flow control is required, the DM8203 / DM8203I sends jam pattern and results in a collision. The flow control ability can be set in REG 08h/09h/0Ah.11h.[5].

9.2.9 Partition Mode

The DM8203 / DM8203I provides a partition mode for each port, see REG 08h/09h/0Ah.11h.[6]. The port enters partition mode when more than 64 consecutive collisions are occurred. In partition mode the port continuous to transmit but it will not receive. The port returned to normal operation mode when a good packet is seen on the wire. The detail description of partition mode represent following:

(1). Entering Partition State

A port will enter the Partition State when either of the following conditions occurs:

- The port detects a collision on every one of 64 consecutive re-transmit attempts to the same packet.
- The port detects a single collision which occurs for more than 512 bit times.
- Transmit defer timer time out, which indicates the transmitting packet is deferred to long.

(2). While in Partition State:

The port will continue to transmit its pending packet, regardless of the collision detection, and will not allow the usual Back-off Algorithm. Additional packets pending for transmission will be transmitted, while ignoring the internal collision indication. This frees up the ports transmit buffers which would otherwise be filled up at the expense of other ports buffers. The assumption is that the partition is signifying a system failure situation (bad connection/cable/station), thus dropping packets is a small price to pay vs. the cost of halting the switch due to a buffer full condition.

(3). Exiting from Partition State

The Port exits from Partition State, following the end of a successful packet transmission. A successful packet transmission is defined as no collisions were detected on the first 512 bits of the transmission.

9.2.10 Broadcast Storm Filtering

The DM8203 / DM8203I has an option to limit the traffic of broadcast or multicast packets, to protect the switch from lower bandwidth availability.

There are two types of broadcast storm control, one is throttling broadcast packet only, the other includes multicast. This feature can be set through REG 08h/09h/0Ah.12h.

The broadcast storm threshold can be programmed by EEPROM or REG 08h/09h/0Ah.15h, the default setting is no broadcast storm protecting.

9.2.11 Bandwidth Control

The DM8203 / DM8203I supports two types of bandwidth control for each port. One is the ingress and egress bandwidth rate can be controlled separately, the other is combined together, this function can be set through REG 08h/09h/0Ah.12h.[14]. The bandwidth control is disabled by default.

To separate and combined bandwidth control mode, the threshold rate is defined in REG 08h/09h/0Ah.15h.

The behavior of bandwidth control as below:

(1). For the ingress control, if flow control function is enabled, Pause or Jam packet will be transmitted. The ingress packets will be dropped if flow control is disabled.

(2). For the egress control, the egress port will not transmit any packets. On the other hand, the ingress bandwidth of source port will be throttled that prevent packets from forwarding.

(3). In combined mode, if the sum of ingress and egress bandwidth over threshold, the bandwidth will be throttled.

9.2.12 Port Monitoring Support

The DM8203 / DM8203I supports “Port Monitoring” function on per port base, detail as below:

(1). Sniffer Port and Monitor Port

There is only one port can be selected as “sniffer port” by REG 10h.13h, multiple ports can be set as “receive monitor port” or “transmit monitor port” in REG 08h/09h/0Ah.12h.

(2). Receive monitor

All packets received on the “receive monitor port” are send a copy to “sniffer port”. For example, port 0 is set as “receive monitor port” and port 2 is selected as a “sniffer port”. If a packet is received form port 0 and predestined to port 1 after forwarding decision, the DM8203 / DM8203I will forward it to port 1 and port 2 in the end.

(3). Transmit monitor

All packets transmitted on the “transmit monitor port” are send a copy to “sniffer port”. For example, port 1 is set as “transmit monitor port” and port 2 is selected as “sniffer port”. If a packet is received from port 0 and predestined to port 1 after forwarding decision, the DM8203 / DM8203I will forward it to port 1 and port 2 in the end.

(4). Exception

The DM8203 / DM8203I has an optional setting that broadcast/multicast packets are not monitored (see REG 08h/09h/0Ah.12h.[11]). It’s useful to avoid unnecessary bandwidth.

9.2.13 VLAN Support

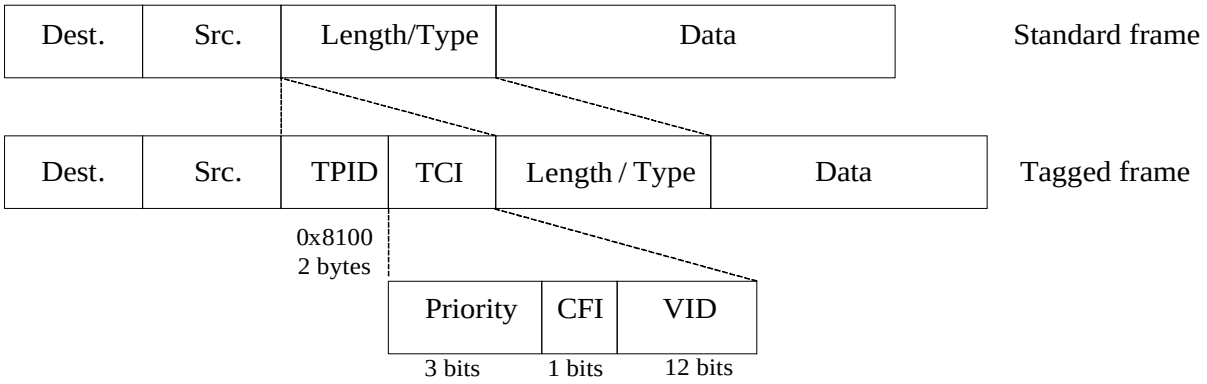
9.2.13.1 Port-Based VLAN

The DM8203 / DM8203I supports port-based VLAN as default, and up to 16 groups. Each port has a default VID called PVID (Port VID, see REG 08h/09h/0Ah.16h). For VLAN setting, the DM8203 / DM8203I used LSB 4-bytes of PVID as index and mapped to the VLAN Group Mapping Registers (REG 13h.10h~1Fh) to decide the destination port(s).

9.2.13.2 802.1Q-Based VLAN

Regarding IEEE 802.1Q standard, Tag-based VLAN uses an extra tag to identify the VLAN membership of a frame across VLAN-aware switch/router. A tagged frame is four bytes longer than an untagged frame and contains two bytes of TPID (Tag Protocol Identifier) and two bytes of TCI (Tag Control Information).

The DM8203 / DM8203I also supports 16 802.1Q-based VLAN groups, as specified in REG 11h.1Eh.[0]. It's obvious that the tagged packets can be assigned to several different VLANs which are determined according to the VID inside the VLAN Tag. Therefore, the operation is similar to port-based VLAN. The DM8203 / DM8203I used LSB 4-bytes VID of received packet with VLAN tag and VLAN Group Mapping Register (REG 13h.10h~1Fh) to configure the VLAN partition. If the destination port of received packet is not same VLAN group with received port, it will be discarded.



9.2.13.3 Tag/Untag

User can define each port as Tag port or Un-tag port by REG 08h/09h/0Ah.17h.[14] in 802.1Q-based VLAN mode. The operation of Tag and Un-tag can explain as below conditions:

(1). Receive untagged packet and forward to Un-tag port. Received packet will forward to destination port without modification.

(2). Receive tagged packet and forward to Un-tag port. The DM8203 / DM8203I will remove the tag from the packet and recalculate CRC before sending it out.

(3). Receive untagged packet and forward to Tag port. The DM8203 / DM8203I will insert the PVID tag when an untagged packet enters the port, and recalculate CRC before delivering it.

(4). Receive tagged packet and forward to Tag port. Received packet will forward to destination port without modification.

9.2.14 Priority Support

The DM8203 / DM8203I supports Quality of Service (QoS) mechanism for multimedia communication such as VoIP and video conferencing.

The DM8203 / DM8203I provides three priority classifications: Port-based, 802.1p-based and DiffServ-based priority. See next section for more detail. The DM8203 / DM8203I offers four level queues for transmit on each port.

The DM8203 / DM8203I provides two packet scheduling algorithms: Weighted Round Robin (WRR) and Strict Priority Queuing (SPQ). WRR based on their priority and queue weight, the priority weight 8, 4, 2 and 1 for queue 3, 2, 1, and 0 respectively by default. Queues with larger weights get more service than smaller. This mechanism can get highly efficient bandwidth and smooth the traffic. Strict Priority Queuing (SPQ) based on priority only. The packets on the highest priority queue is transmitted first. The next highest-priority queue is work until last queue empties, and so on. This feature can be set in REG 08h/09h/0Ah.17h.[5].

9.2.14.1 Port-Based Priority

Port based priority is the simplest scheme and as default. Each port has a 2-bit priority value as index for splitting ingress packets to the corresponding transmit queue. This value can be set in REG 08h/09h/0Ah.17h.[1:0].

9.2.14.2 802.1p-Based Priority

The DM8203 / DM8203I extracts 3-bit priority field from received packet with 802.1p VLAN tag, and maps this field against VLAN Priority Map Registers (REG 10h.17h) to determine which transmit queue is designated. The VLAN Priority Map is programmable.

9.2.14.3 DiffServ-Based Priority

DiffServ based priority uses the most significant 6-bit of the ToS field in standard IPv4 header, and maps this field against ToS Priority Map Registers (REG 10h.18h~1Fh) to determine which transmit queue is designated. The ToS Priority Map is programmable too. In addition, User can only refer to most significant 3-bit of the ToS field optionally, see REG 11h.1Eh.[7].

9.3 MII Interface

9.3.1 MII Data Interface

The DM8203 / DM8203I port 2 provides a Media Independent Interface (MII) as defined in the IEEE 802.3u standard (Clause 22).

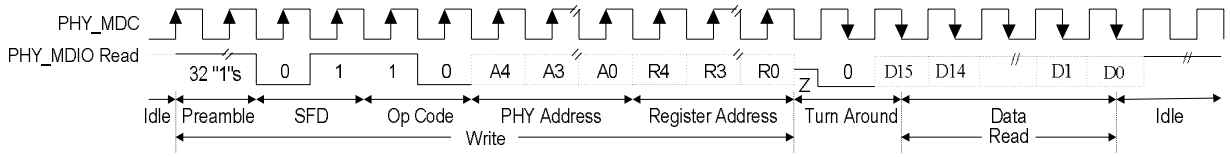
The MII consists of a nibble wide receive data bus, a nibble wide transmit data bus, and control signals to facilitate data transfers between the DM8203 / DM8203I port 2 and external device (a PHY or a MAC in reverse MII).

- P2_TXD3~0 (transmit data) is a nibble (4 bits) of data that are driven by the DM8203 / DM8203I synchronously with respect to P2_TXC. For each P2_TXC period, which P2_TXE is asserted, P2_TXD3~0 are accepted for transmission by the external device.
- P2_TXC (transmit clock) from the external device is a continuous clock that provides the timing reference for the transfer of the P2_TXE, P2_TXD3~0. The DM8203 / DM8203I can drive 25MHz clock if it is configured to reversed MII mode.
- P2_TXE (transmit enable) from the DM8203 / DM8203I port 2 MAC indicates that nibbles are being presented on the MII for transmission to the external device.
- P2_RXD3~0 (receive data) is a nibble (4 bits) of data that are sampled by the DM8203 / DM8203I port 2 MAC synchronously with respect to P2_RXC. For each P2_RXC period which P2_RXDV is asserted, P2_RXD3~0 are transferred from the external device to the DM8203 / DM8203I port 2 MAC reconciliation sub layer.
- P2_RXC3~0 (receive clock) from external device to the DM8203 / DM8203I port 2 MAC reconciliation sub layer is a continuous clock that provides the timing reference for the transfer of the P2_RXDV, P2_RXD3~0, and P2_RXER signals.
- P2_RXDV (receive data valid) input from the external device to indicates that the external device is presenting recovered and decoded nibbles to the DM8203 / DM8203I port 2 MAC reconciliation sub layer. To interpret a receive frame correctly by the reconciliation sub layer, P2_RXDV must encompass the frame, starting no later than the Start-of-Frame delimiter and excluding any End-Stream delimiter.
- P2_RXER (receive error) input from the external device is synchronously with respect to P2_RXC. P2_RXER will be asserted for 1 or more clock periods to indicate to the reconciliation sub layer that an error was detected somewhere in the frame being transmitted from the external device to the DM8203 / DM8203I port 2 MAC.
- P2_CRS (carrier sense) is asserted by the external device when either the transmit or receive medium is non-idle, and de-asserted by the external device when the transmit and receive medium are idle. The P2_CRS can also in output mode when the DM8203 / DM8203I port 2 is configured to reversed MII mode.
- P2_COL (collision detection) is asserted by the external device, when both the transmit and receive medium is non-idle, and de-asserted by the external device when the either transmit or receive medium are idle. The P2_COL can also in output mode when the DM8203 / DM8203I port 2 is configured to reversed MII mode.

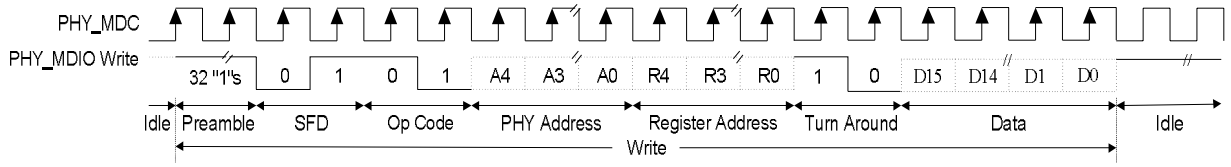
9.3.2 MII Serial Management Interface

The serial control interface uses a simple two-wired serial interface to obtain and control the status of the physical layer through the MII interface. The serial control interface consists of PHY_MDC (Management Data Clock to PHY), and PHY_MDIO (Management Data Input/Output to PHY) signals.

In read/write operation, the management data frame is 64-bits long and starts with 32 contiguous logic one bits (preamble) synchronization clock cycles on PHY_MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by the operation code (OP) :< 10> indicates Read operation and <01> indicates Write operation. For read operation, a 2-bit turnaround (TA) filing between Register Address field and Data field is provided for PHY_MDIO to avoid contention. Following the turnaround time, 16-bit data is read from or written onto management registers.



Management Interface - Read Frame Structure



Management Interface - Write Frame Structure

9.4 Internal PHY Functions

9.4.1 100Base-TX Operation

The transmitter section contains the following functional blocks:

- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Converter
- NRZI to MLT-3
- MLT-3 Driver

9.4.1.1 4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission, see reference Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the desertions of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code-group pair (01101 00111) indicating the end of frame. After the T/R code-group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

9.4.1.2 Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to the repeated 5B sequences, like the continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code-group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

9.4.1.3 Parallel to Serial Converter

The Parallel to Serial Converter receives parallel 5B scrambled data from the scrambler, and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI encoder block

9.4.1.4 NRZ to NRZI Encoder

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard, for 100Base -TX transmission over Category-5 unshielded twisted pair cable.

9.4.1.5 MLT-3 Converter

The MLT-3 conversion is accomplished by converting The data stream output, from the NRZI encoder

into two binary data streams, with alternately phased logic One event.

9.4.1.6 MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver, which converts these streams to current sources and alternately drives either side of the transmit transformer's primary winding, resulting in a minimal current MLT-3 signal.

9.4.1.7 4B5B Code Group

Symbol	Meaning	4B code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	undefined	01101
R	ESD (2)	undefined	00111
H	Error	undefined	00100
V	Invalid	undefined	00000
V	Invalid	undefined	00001
V	Invalid	undefined	00010
V	Invalid	undefined	00011
V	Invalid	undefined	00101
V	Invalid	undefined	00110
V	Invalid	undefined	01000
V	Invalid	undefined	01100
V	Invalid	undefined	10000
V	Invalid	undefined	11001

Table 1

9.4.2 100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data.

The receive section contains the following functional blocks:

- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

9.4.2.1 Signal Detect

The signal detects function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX standards for both voltage thresholds and timing parameters.

9.4.2.2 Adaptive Equalization

When transmitting data over copper twisted pair cable at high speed, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation, caused by frequency variations, must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation requires significant compensation, which will be over-killed in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

9.4.2.3 MLT-3 to NRZI Decoder

The DM8203 / DM8203I decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data.

9.4.2.4 Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125 MHz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ decoder.

9.4.2.5 NRZI to NRZ

The transmit data stream is required to be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

9.4.2.6 Serial to Parallel

The Serial to Parallel Converter receives a serial data stream from the NRZI to NRZ converter. It converts the data stream to parallel data to be presented to the descrambler.

9.4.2.7 Descrambler

Because of the scrambling process requires to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, and it descrambles the data streams, and presents the data streams to the Code Group alignment block.

9.4.2.8 Code Group Alignment

The Code Group Alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected and subsequent data is aligned on a fixed boundary.

9.4.2.9 4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups receive the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R Symbols).

The T/R symbol pair is also stripped from the nibble, presented to the Reconciliation layer.

9.4.3 10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM8203 / DM8203I is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented in nibble format, converted to a serial bit stream, then the Manchester encoded. When receiving, the bit stream, encoded by the Manchester, is decoded and converted into nibble format.

9.4.4 Collision Detection

For half-duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. Collision detection is disabled in full duplex operation.

9.4.5 Carrier Sense

Carrier Sense (CRS) is asserted in half-duplex operation during transmission or reception of data. During full-duplex mode, CRS is asserted only during Receive operations.

9.4.6 Auto-Negotiation

The objective of Auto-negotiation is to provide a means to exchange information between linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-negotiation does not test the characteristics of the linked segment. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

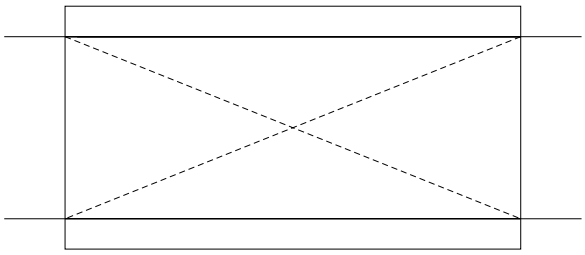
Auto-negotiation also provides a parallel detection function for devices that do not support the Auto-negotiation feature. During Parallel detection there is no exchange of information of configuration. Instead, the receive signal is examined. If it is discovered that the signal matches a technology, which the receiving device supports, a connection will be automatically established using that technology. This allows devices not to support Auto-negotiation but support a common mode of operation to establish a link.

9.5 HP Auto-MDIX Function

The DM8203 / DM8203I supports the automatic detect cable connection type, MDI/MDIX (straight through/cross over). A manual configuration by register bit for MDI or MDIX is still accepted.

When set to automatic, the polarity of MDI/MDIX controlled timing is generated by 16-bits LFSR. The switching cycle time is located from 200ms to 420ms. The polarity control is always switch until detect received signal. After selected MDI or MDIX, this feature is able to detect the required cable connection type. (Straight through or crossed over) and make correction automatically

RX + /- from DM8203 / DM8203I RX+/- to RJ45



TX + /- from DM8203 / DM8203I TX+/- to RJ45

* MDI: _____

* MDIX: - - - - - - - - -

10. DC and AC Electrical Characteristics

10.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVDD33	Digital 3.3V Power	-0.3	3.6	V	
DVDD18	Digital 1.8V Power	-0.3	1.95	V	
AVDD33	Analog 3.3V Power	-0.3	3.6	V	
AVDD18	Analog 1.8V Power	-0.3	1.95	V	
IOV	Input/Output Voltage	-0.5	5.5	V	
T_{STG}	Storage Temperature Range	-65	+150	°C	
T_A	Ambient Temperature	0	+70	°C	
T_A	Ambient Temperature	-40	+85	°C	For DM8203I
L_T	Lead Temperature (TL, soldering, 10 sec.).	-	+260	°C	

10.2 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DVDD33	Digital 3.3V Power	3.135	-	3.465	V	-
DVDD18	Digital 1.8V Power	1.71	-	1.89	V	-
AVDD33	Analog 3.3V Power	3.135	-	3.465	V	-
AVDD18	Analog 1.8V Power	1.71	-	1.89	V	-
P_D (Power Dissipation)	100BASE-TX	-	107	-	mA	1.8V only
		-	54	-	mA	3.3V only
	10BASE-TX	-	57	-	mA	TX idle, 1.8V only
		-	64	-	mA	100% utilization, 1.8V only
		-	11	-	mA	3.3V only

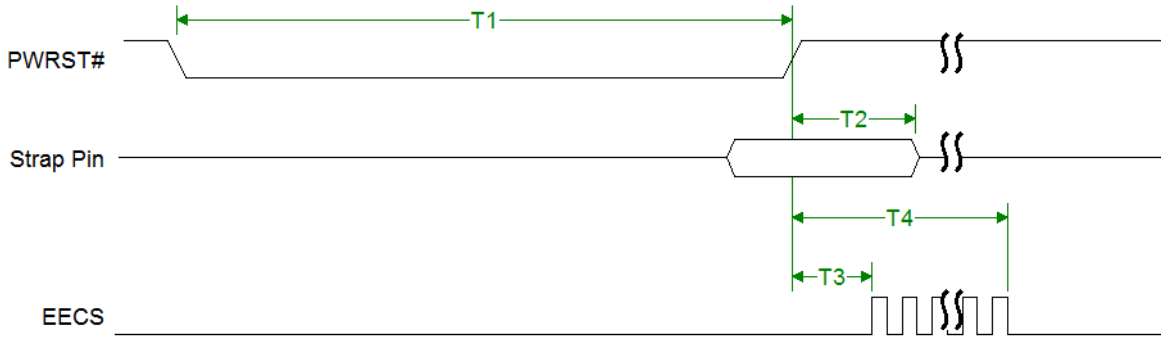
10.3 DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
VIL	Input Low Voltage	-	-	0.8	V	Vcond1*
VIH	Input High Voltage	2.0	-	-	V	Vcond1
IIL	Input Low Leakage Current	-1	-	-	uA	VIN = 0.0V, Vcond1
IIH	Input High Leakage Current	-	-	1	uA	VIN = 3.3V, Vcond1
Outputs						
VOL	Output Low Voltage	-	-	0.4	V	IOL = 4mA
VOH	Output High Voltage	2.4	-	-	V	IOH = -4mA
Receiver						
VICM	RX+/RX- Common Mode Input Voltage	-	1.8	-	V	100 Ω Termination Across
Transmitter						
VTD100	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
VTD10	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
ITD100	100TX+/- Differential Output Current	|19|	|20|	|21|	mA	Absolute Value
ITD10	10TX+/- Differential Output Current	|44|	|50|	|56|	mA	Absolute Value

Note:
1. Vcond1: DVDD33 = 3.3V, DVDD18 = 1.8V, AVDD33 = 3.3V, AVDD18 = 1.8V.

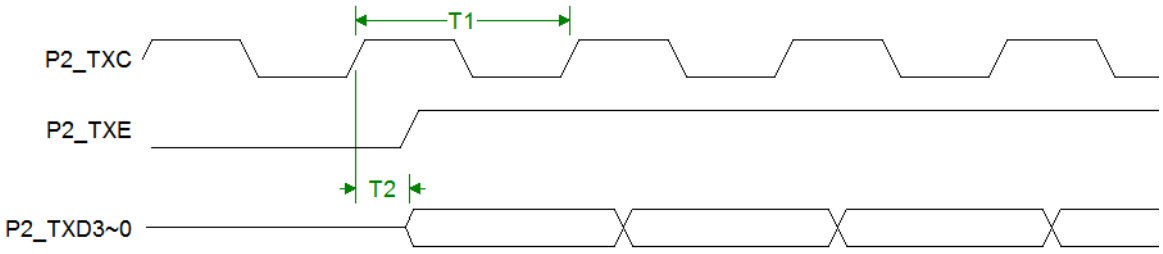
10.4 AC Characteristics

10.4.1 Power On Reset Timing



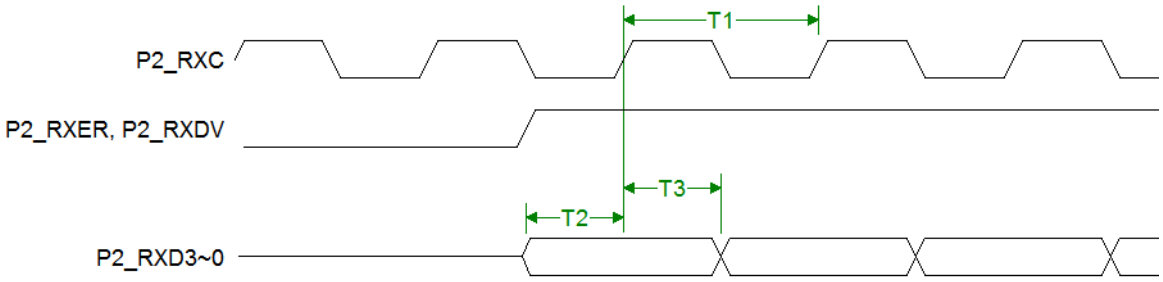
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	PWRST# Low Period	1	-	-	ms	-
T2	Strap pin hold time with PWRST#	40	-	-	ns	-
T3	PWRST# high to EECS high	-	5	-	us	
T4	PWRST# high to EECS burst end	-	--	4	ms	

10.4.2 Port 2 MII Interface Transmit Timing



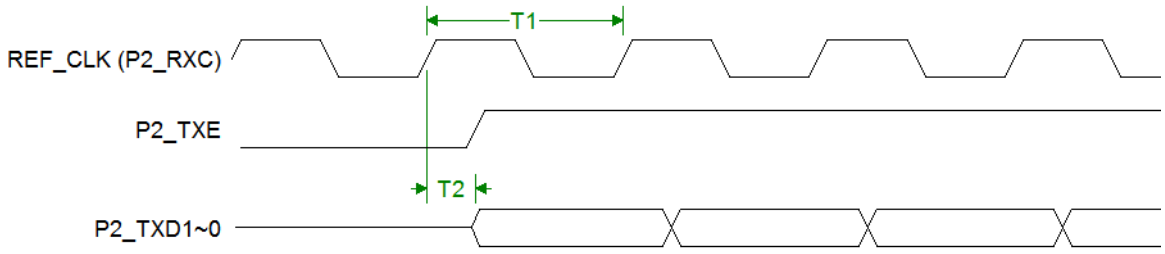
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	100M MII Transmit Clock Period	-	40	-	ns
T1	10M MII Transmit Clock Period	-	400	-	ns
T2	P2_TXE,P2_TXD3~0 to P2_TXC Rising Output Delay		8		ns

10.4.3 Port 2 MII Interface Receive Timing



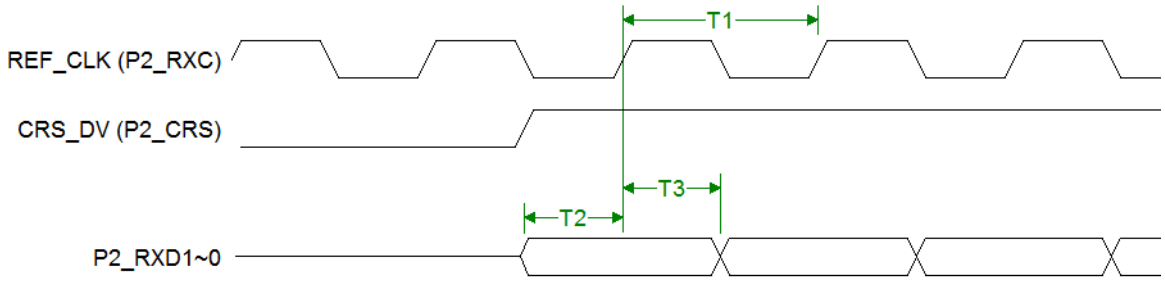
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	100M MII Receive Clock Period	-	40	-	ns
T1	10M MII Receive Clock Period	-	400	-	ns
T2	P2_RXER, P2_RXDV and P2_RXD3~0 to P2_RXC Setup Time	5	-	-	ns
T3	P2_RXER, P2_RXDV and P2_RXD3~0 to P2_RXC Hold Time	5	-	-	ns

10.4.4 Port 2 RMII Interface Transmit Timing



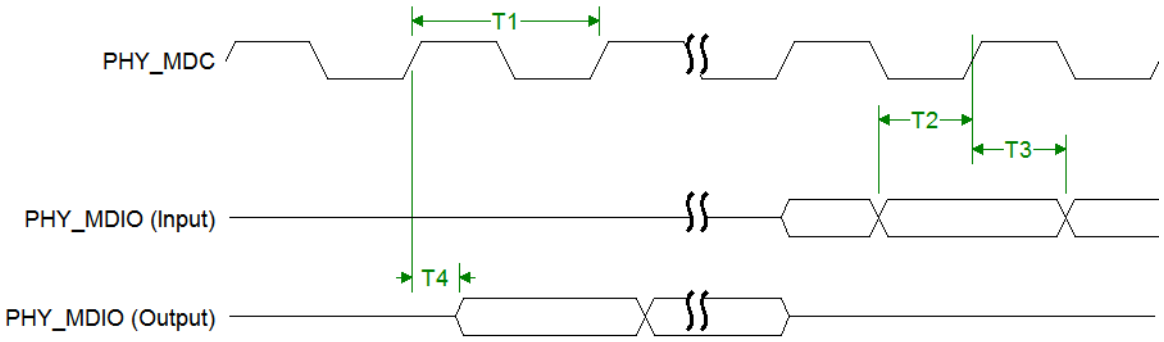
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	RMII REF_CLK Period	-	20	-	ns
T2	P2_TXE,P2_TXD1~0 to REF_CLK Rising Output Delay		8		ns

10.4.5 Port 2 RMII Interface Receive Timing



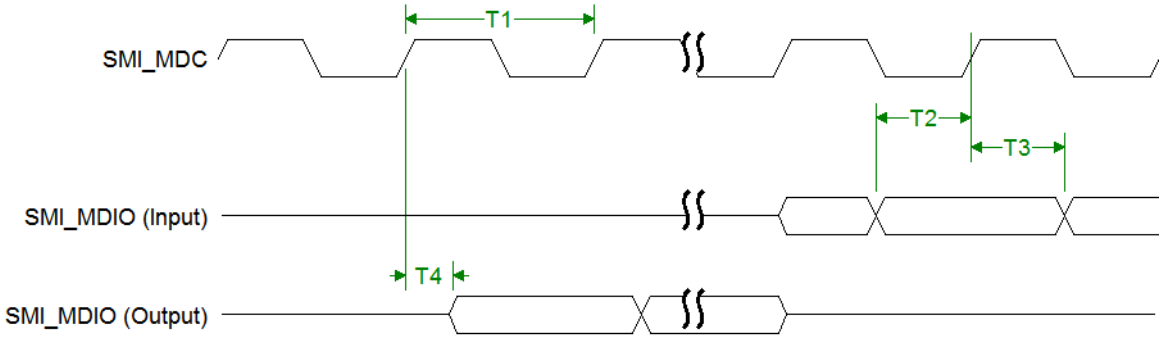
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	RMII REF_CLK Period	-	20	-	ns
T2	CRS_DV, P2_RXD to REF_CLK Setup Time	4	-	-	ns
T3	CRS_DV, P2_RXD1~0 to REF_CLK Hold Time	2	-	-	ns

10.4.6 MII Management Interface Timing



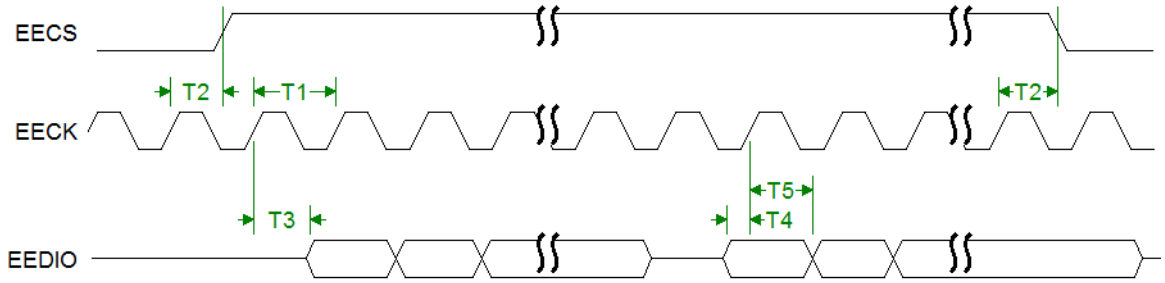
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	PHY_MDC Period	-	1920	-	ns
T2	PHY_MDIO to PHY_MDC Setup Time on Input State	40	-	-	ns
T3	PHY_MDIO to PHY_MDC Hold Time on Input State	40	-	-	ns
T4	PHY_MDIO to PHY_MDC Rising Output Delay on Output State	-	960	-	ns

10.4.7 Host SMI Interface Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	SMI_MDC Period	80	-	-	ns
T2	SMI_MDIO to SMI_MDC Setup Time on Input State	40	-	-	ns
T3	SMI_MDIO to SMI_MDC Hold Time on Input State	40	-	-	ns
T4	SMI_MDIO to SMI_MDC Rising Output Delay on Output State	-	5	-	ns

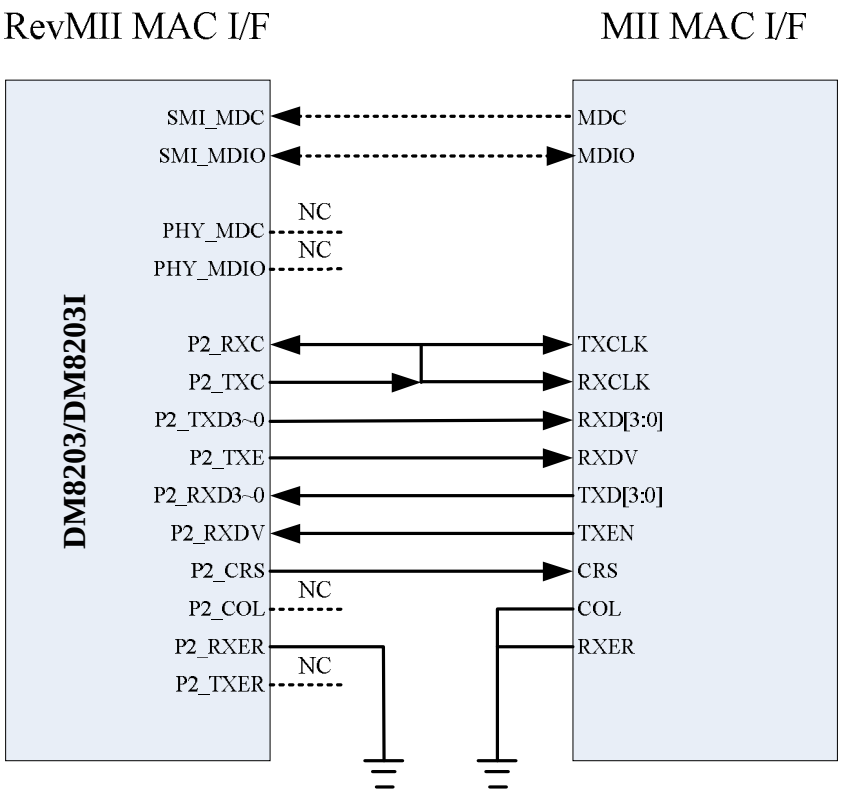
10.4.8 EEPROM Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	EECK Period	-	5120	-	ns
T2	EECS to EECK Rising Output Delay	-	4160	-	ns
T3	EEDIO to EECK Rising Output Delay on Output State	-	4160	-	ns
T4	EEDIO to EECK Rising Setup Time on Input State	8	-	-	ns
T5	EEDIO to EECK Rising Hold Time on Input State	8	-	-	ns

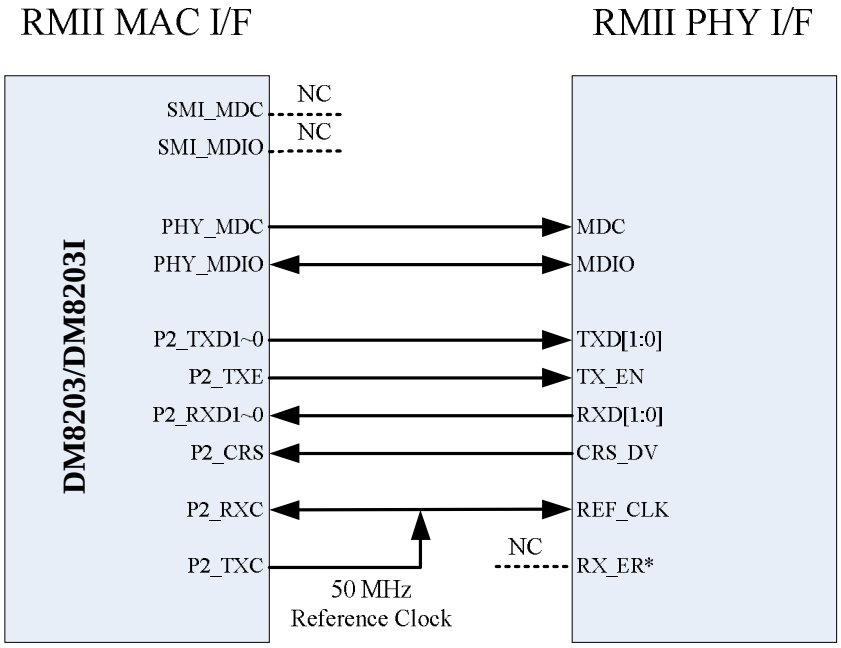
11. Application Information

11.1 Application of Reverse MII



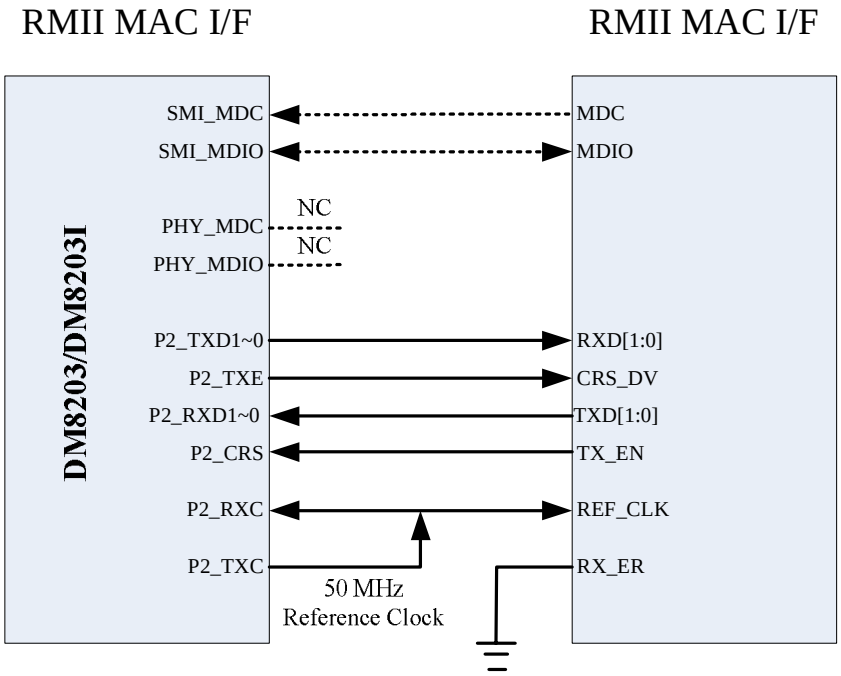
Note: The P2_TXE and P2_TXD2 pins of DM8203 / DM8203I must be pull-up resistor with 4.7K ohm to DVDD33 in this application.

11.2 Application of Reduce MII to PHY



Note: The P2_TXD3 pin of DM8203 / DM8203I must be pull-up resistor with 4.7K ohm to DVDD33 in this application.

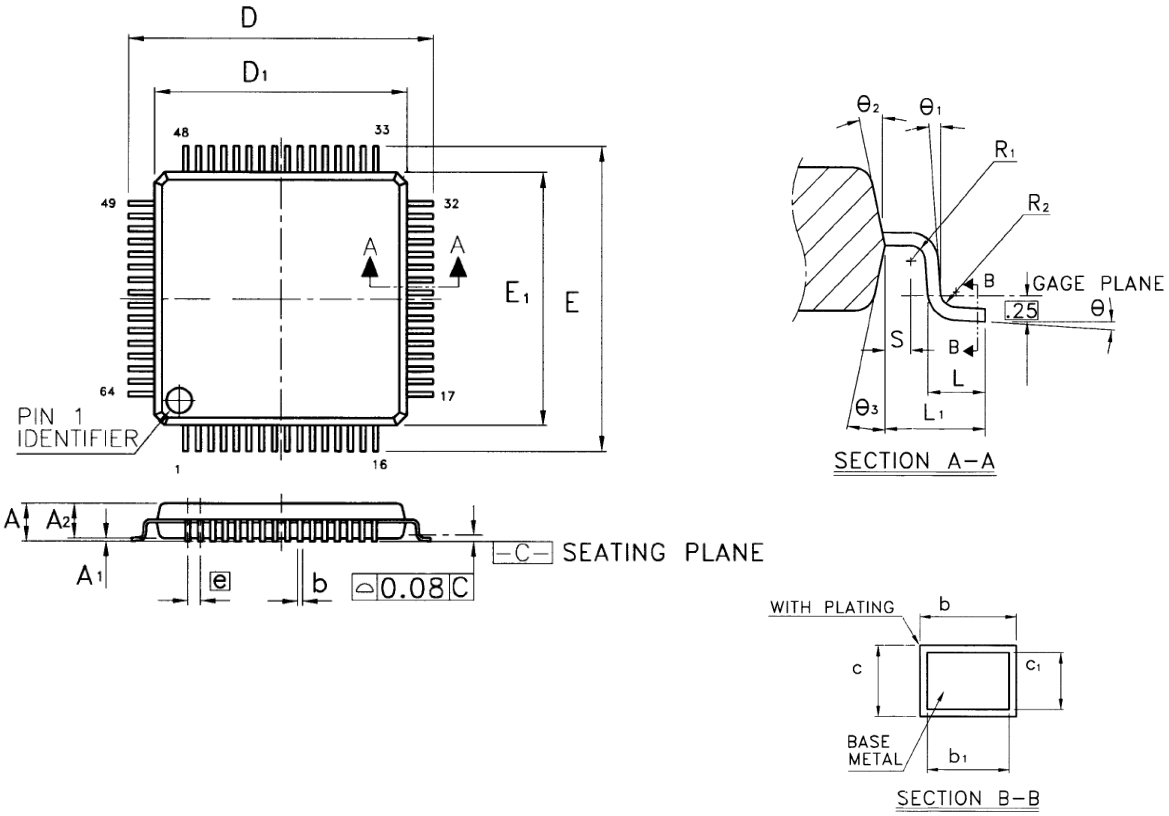
11.3 Application of Reduce MII to MAC



Note: The P2_TXE and P2_TXD3 pins of DM8203 / DM8203I must be pull-up resistor with 4.7K ohm to DVDD33 in this application.

12. Package Information

64 Pins LQFP Package Outline Information:



Symbol	Dimension in mm				Dimension in inch		
	Min	Nom	Max		Min	Nom	Max
A	-	-	1.60		-	-	0.063
A_1	0.05	-	0.15		0.002	-	0.006
A_2	1.35	1.40	1.45		0.053	0.055	0.057
b	0.17	0.22	0.27		0.007	0.009	0.011
b_1	0.17	0.20	0.23		0.007	0.008	0.009
c	0.09	-	0.20		0.004	-	0.008
c_1	0.09	-	0.16		0.004	-	0.006
D	12.00 BSC				0.472 BSC		
D_1	10.00 BSC				0.394 BSC		
E	12.00 BSC				0.472 BSC		
E_1	10.00 BSC				0.394 BSC		
e	0.50 BSC				0.020 BSC		
L	0.45	0.60	0.75		0.018	0.024	0.030
L_1	1.00 REF				0.039 REF		
R_1	0.08	-	-		0.003	-	-
R_2	0.08	-	0.20		0.003	-	0.008
S	0.20	-	-		0.008	-	-
θ	0^o	3.5^o	7^o		0^o	3.5^o	7^o
θ_1	0^o	-	-		0^o	-	-
θ_2	12^o TYP				12^o TYP		
θ_3	12^o TYP				12^o TYP		

1. Dimension D_1 and E_1 do not include resin fin.
2. All dimensions are base on metric system.
3. General appearance spec should base on its final visual inspection spec.

13. Ordering Information

Part Number	Pin Count	Package
DM8203EP	64	LQFP (Pb-free)
DM8203IEP	64	LQFP (Pb-free)

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For additional information about DAVICOM products, contact the Sales department at:

Headquarters

Hsin-chu Office:
No.6, Li-Hsin 6th Rd.,
Hsinchu Science Park,
Hsinchu City 300, Taiwan, R.O.C.
TEL: +886-3-5798797
FAX: +886-3-5646929
MAIL: sales@davicom.com.tw
HTTP: http://www.davicom.com.tw

WARNING

Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.