

# HHW Corp. Flash Media Products



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## Revision History

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1.0	Initial Release	June 30, 2017	Preliminary

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# Datasheet

## Secure Digital Card

### PRODUCT DESCRIPTION

SD Memory card (Secure Digital Memory Card) is a memory card that is specifically designed to meet the security, capacity, performance and environment requirements. The SD Memory Card will include a copyright protection mechanism that complies with the security of the SDMI standard and will be faster and capable for higher memory capacity. The SD Memory Card communication is based on an advanced 9-pin interface (Clock, Command, 4x Data and 3x Power lines) designed to operate in at maximum operating frequency of 50 MHz and low voltage range.

HHW's SD33 SD memory card is designed with industry leading edge micro controllers and SLC/MLC flash to achieve high level performance, reliability and endurance. SD33 SD memory card is optimized for OEM applications where device life is the top priority.

### FEATURES

- Compliance:
  - SD specification version 2.0 and 3.0 (UHS-I), and eSD 2.1
- Operating voltage range
  - 2.7-3.6 V
- Variable clock Frequency
  - 0-25MHz - Default Speed Timing
  - 0-50MHz - High Speed Timing
- Support
  - CPRM and ASSD 2.0 or Mc-EX can be supported
  - SD (x1 and x4) and SPI mode
  - Write protection using mechanical switch
- Support SD command class:
  - All SD Speed Classes Possible
- Performance:
  - Read (max): 95MB/s
  - Write (max): 90MB/s
- Available Storage Capacities:
  - 128MB~256GB
- High reliability and long life
  - Internal ECC (Error Correcting Code) results in high data reliability
    - Advanced wear leveling algorithm
    - AES encryption engine 128 and 256-Bit, ECB, CBC, and XTS modes supported
- Temperature Range: -40 °C to +85 °C (W-Temp) ; 0 °C to 70 °C (Temp)
- RoHS Compliant

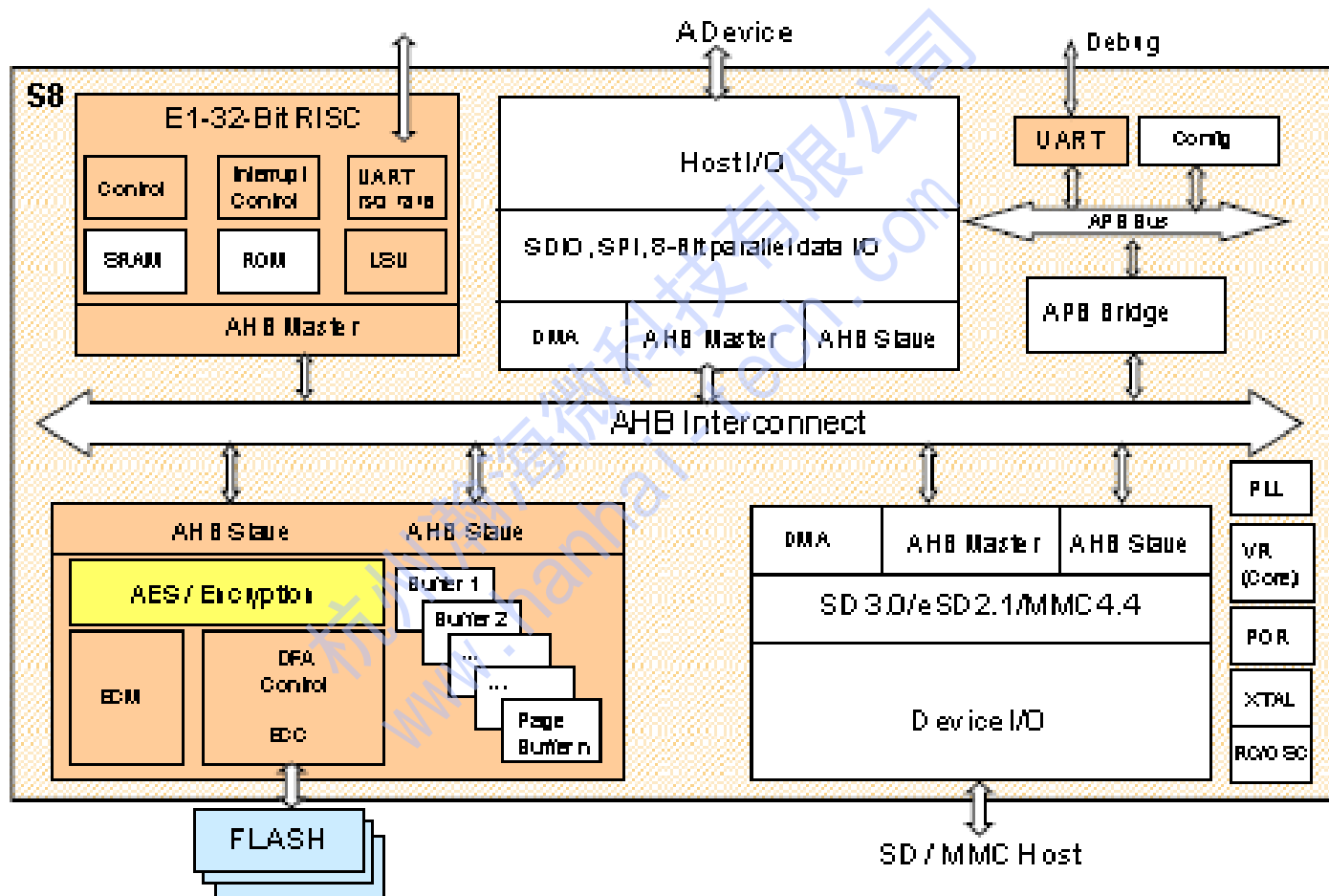
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# 1 General Description

The HHW Corporation SD memory card contains a Hyperstone designed Flash controller, programmable firmware and flash memory module(s). The proprietary space manager architecture in the controller maximizes read/write data rate performance to and from the host and flash memory, eliminating firmware delays during sector read and write operations. The Hyperstone Flash controller, combined with tailored firmware, which ensures complete compatibility with a wide range of operating systems.

Figure 1-1: Block Diagram



## 2 PRODUCT SPECIFICATION

### 2.1 Electrical Interface

**Table 2-1a: SD mode pin assignment and description**

Pin No.	Signal	Signal Types	Description
1	CD/DAT3	Signal	Card Detect/ Data Line [bit 3]
2	CMD	Signal	Command/Response
3	VSS1	Ground	Ground
4	VDD	Power	Supply voltage
5	CLK	Signal	Clock
6	VSS2	Ground	Ground
7	DAT0	Signal	Data Line [bit 0]
8	DAT1	Signal	Data Line [bit 1]
9	DAT2	Signal	Data Line [bit 2]

**Table 2-1b: SPI mode pin assignment and description**

Pin No.	Signal	Signal Types	Description
1	CS	Signal	Chip Select (neg. true)
2	DI	Signal	Data in
3	VSS1	Ground	Ground
4	VDD	Power	Supply voltage
5	SCLK	Signal	Clock
6	VSS2	Ground	Ground
7	D0	Signal	I/O
8	Reserved		
9	Reserved		

**Note:**

- 1) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET\_BUS\_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
- 2) At power up this line has a 50Kohm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET\_CLR\_CARD\_DETECT (ACMD42) command

## 2.2 Environmental and Reliability Characteristics

**Table 2-2: Environmental and Reliability Characteristics**

Shock	1,500 G max. (operating/non-operating)
Vibration	20 G peak to peak max. (operating/non-operating)
Acoustic Noise	0 dB
Humidity	95%
Altitude	80,000 ft max.
Data Retention	10 years
Endurance	>2,000,000 Program Erase Cycles
MTBF	3,000,000 power-on hours
Data Reliability	1 in $10^{14}$ bits, read

## 2.3 Data Transfer Rate

**Table 2-3: Data Transfer Rate**

Speed Rate	Sequential Read Speed (Max)
650X	95 MB/S
Speed Rate	Sequential Write Speed (Max)
615X	90 MB/s

Note: where X denotes a write performance of 150Kbytes per second.

## 2.4 POWER CYCLING TEST

HHW's power cycling test simulates device stability against data loss/corruption under unstable power supply conditions. The Power Cycling Test contains (3) main test items (In Order):

- **Dynamic Read/Write Test**
  - Write sector-by-sector to Sec X (randomly picked)
  - Power off in the middle of writing
  - 10s later, power on device
  - Verify 1024 sectors prior to (Sec X – 128) sectors
  
- **Protection for Static Area Test**
  - Write 100 sectors to (5) pre-defined locations
  - Power off in the middle of writing after completed
  - 10s later, power on device
  - Verify data sectors are maintained
  
- **Pattern Test**
  - Combination of Dynamic and Protection Test
  - Tested with additional test patterns

Each test is performed for 3,500 cycles.



## 3 ELECTRICAL SPECIFICATION

### 3.1 Absolute Maximum Ratings

**Table 3-1: Absolute Max. Ratings**

Parameters	Symbol	Min	Max	Unit
Storage Temperature	Tstg	-55	+95	°C
Input Power	Vdd	3.0	3.6	V
Voltage on any pin except Vcc with respect to GND	V	0.5	Vcc+0.5	V
Input Current	I	2	80	mA

**NOTE:** Stress above those listed under Absolute Maximum Ratings may cause permanent DAMAGE to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 3.2 Recommended Operating Conditions

**Table 3-2: Operating Conditions**

Parameters	Symbol	Min	Max	Unit	Test Condition
Operating Temperature	Ta	-40	+85	°C	<b>Industrial Temp</b>
Supply Voltage	Vdd	2.7	3.6	V	

### 3.3 DC Characteristics

**Table 3-3: DC Characteristics**

Parameters	Symbol	Min	Max	Unit	Test Condition
Supply Voltage	Vdd	2.7	3.6	V	
Operating Current	Icc		80	mA	
Suspend Current	Isc	100	1000	uA	
Input LOW Voltage	VIL	Vss-0.3	0.25*Vdd	V	
Input HIGH Voltage	VIH	0.625*Vdd	Vdd+0.3	V	
Output LOW Voltage	VoL		0.125*Vdd	V	IOL=100uA Vdd min
Output HIGH Voltage	VoH	0.75*Vdd		V	IOH=-100uA Vdd min

### 3.4 AC Characteristics

Figure 3-4a: Timing diagram (default mode)

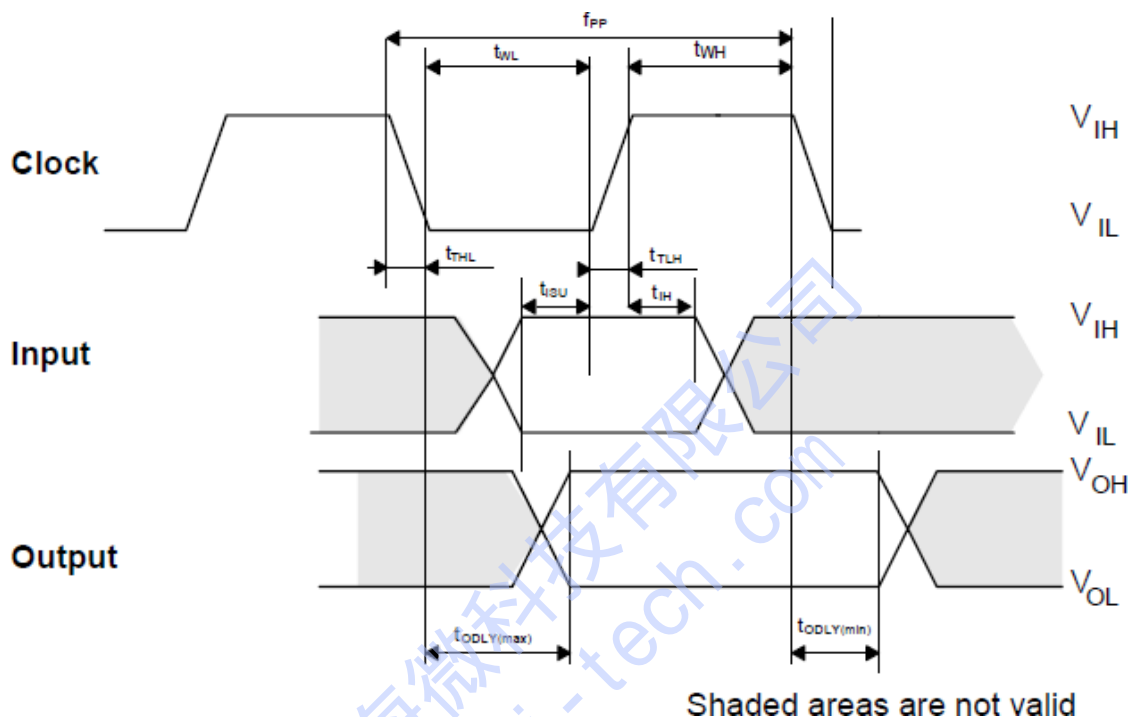
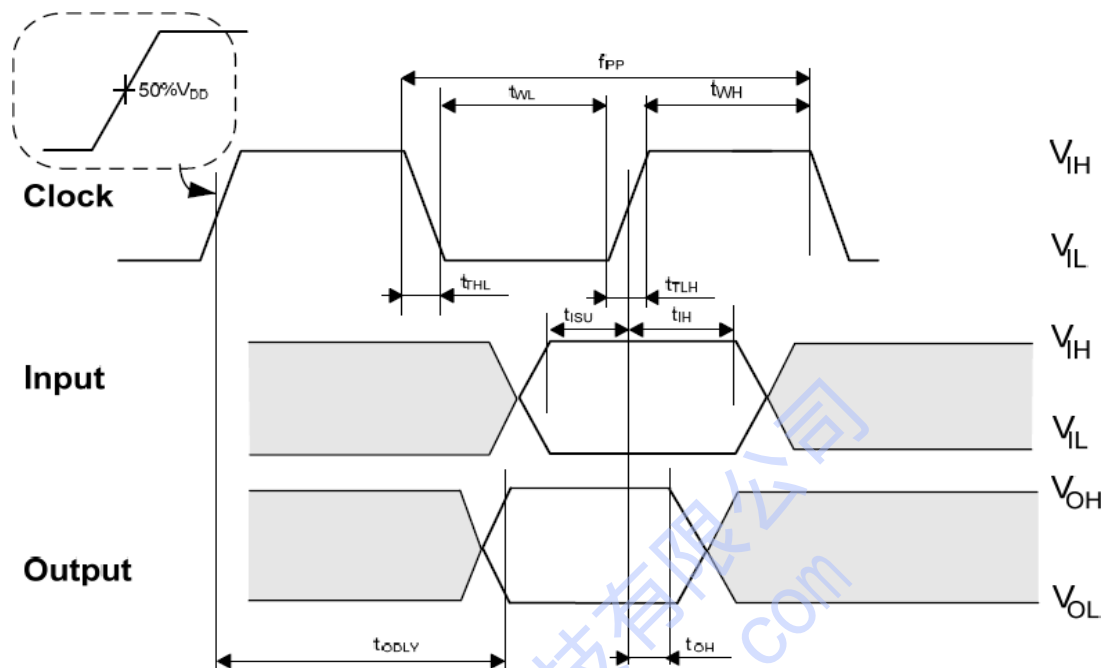


Table 3-4a: AC Characteristics (Default mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min (VIH) and max (VIL))					
Clock frequency data transfer mode	f <sub>PP</sub>	0	25	MHz	C <sub>card</sub> ≤ 10pf (1 card)
Clock frequency identification mode	f <sub>OD</sub>	0 <sub>i</sub> /100	400	kHz	C <sub>card</sub> ≤ 10pf (1 card)
Clock low time	t <sub>WL</sub>	10		ns	C <sub>card</sub> ≤ 10pf (1 card)
Clock high time	t <sub>WH</sub>	10		ns	C <sub>card</sub> ≤ 10pf (1 card)
Clock rise time	t <sub>TLH</sub>		10	ns	C <sub>card</sub> ≤ 10pf (1 card)
Clock fall time	t <sub>THL</sub>		10	ns	C <sub>card</sub> ≤ 10pf (1 card)
Inputs CMD,DAT (referenced to CLK)					
Input set-up time	t <sub>ISU</sub>	5		ns	C <sub>card</sub> ≤ 10pf (1 card)
Input hold time	t <sub>IH</sub>	5		ns	C <sub>card</sub> ≤ 10pf (1 card)
Outputs CMD,DAT (referenced to CLK)					
Output delay time during data transfer mode	t <sub>ODLY</sub>	0	14	ns	C <sub>L</sub> ≤ 40pf (1 card)
Output delay time during identification mode	t <sub>ODLY</sub>	0	50	ns	C <sub>L</sub> ≤ 40pf (1 card)

Note: 1) 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required

**Figure 3-4b: Timing diagram (high-speed mode)**


Shaded areas are not valid

**Table 3-4b: AC Characteristics (high-speed mode)**

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min (V <sub>IH</sub> ) and max (V <sub>IL</sub> ))					
Clock frequency data transfer mode	f <sub>PP</sub>	0	50	MHz	C <sub>card</sub> ≤ 10pf (1 card)
Clock low time	t <sub>WL</sub>	7		ns	C <sub>card</sub> ≤ 10pf (1 card)
Clock high time	t <sub>WH</sub>	7		ns	C <sub>card</sub> ≤ 10pf (1 card)
Clock rise time	t <sub>TLH</sub>		3	ns	C <sub>card</sub> ≤ 10pf (1 card)
Clock fall time	t <sub>THL</sub>		3	ns	C <sub>card</sub> ≤ 10pf (1 card)
Inputs CMD,DAT (referenced to CLK)					
Input set-up time	t <sub>ISU</sub>	6		ns	C <sub>card</sub> ≤ 10pf (1 card)
Input hold time	t <sub>IH</sub>	2		ns	C <sub>card</sub> ≤ 10pf (1 card)
Outputs CMD,DAT (referenced to CLK)					
Output delay time during data transfer mode	t <sub>ODLY</sub>		14	ns	C <sub>L</sub> ≤ 40pf (1 card)
Output hold time	t <sub>OH</sub>	2.5	50	ns	C <sub>L</sub> ≥ 15pf (1 card)
Total system capacitance for each line <sup>1</sup>	C <sub>L</sub>		40	pf	1 card

Note: 1) In order to satisfy severe timing, host shall drive only one card

## 4 PHYSICAL DIMENSIONS

Table 4-1: Physical Dimensions

Length	32.0mm (+/- 0.1mm)
Width	24.0mm (+/- 0.1mm)
Thickness	2.1mm (+/- 0.15mm)

### 4.1 Package Dimensions

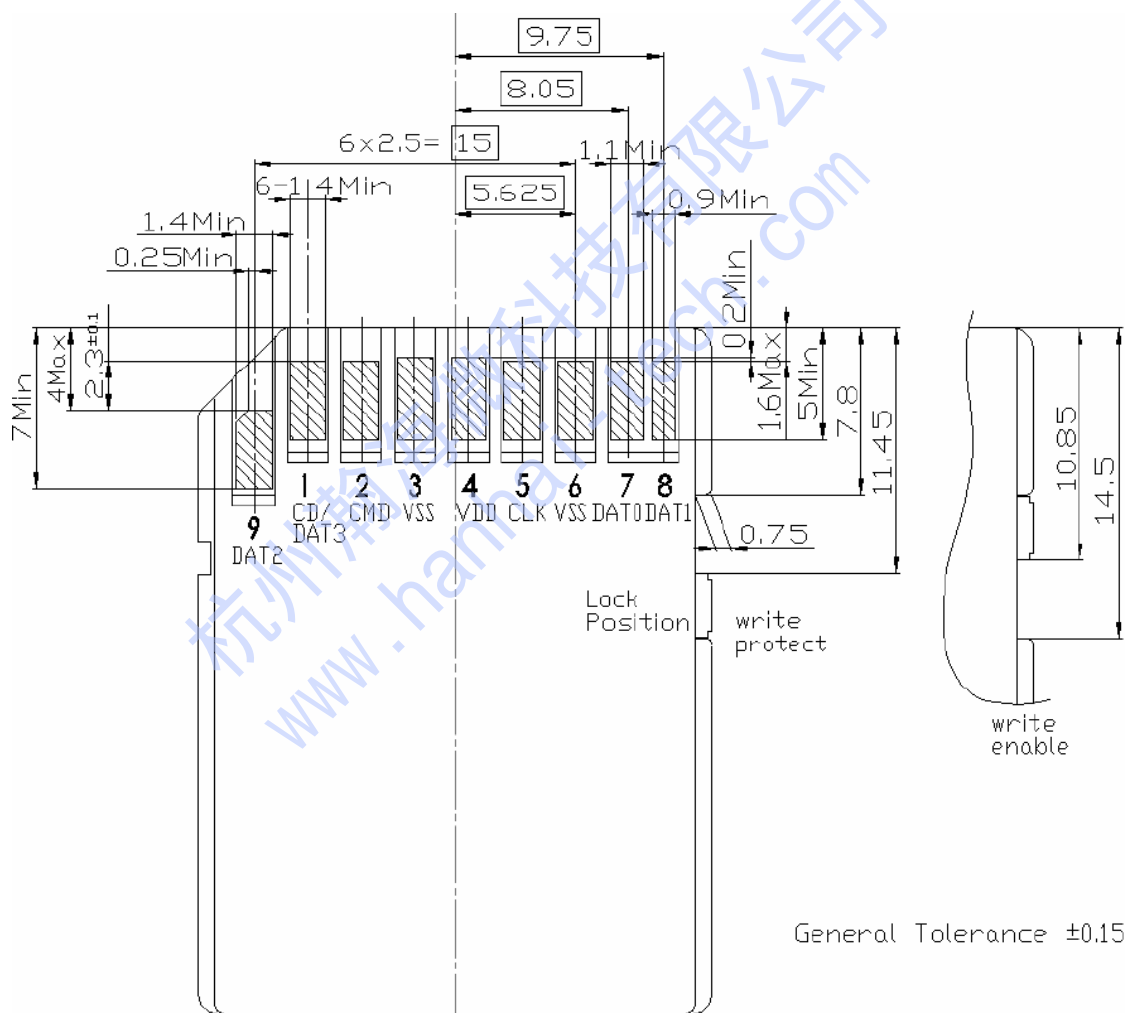


Figure 4-1a: SD card dimension



## 5 Part Number and Ordering Information

### 1. Part Number List

SD Card( SLC)		
Capacity	Normal-Temperature	Wide-temperature
128MB		HHW128MSDS-33
256MB		HHW256MSDS-33
512MB		HHW512MSDS-33
1GB		HHW1GSDS-33
2GB		HHW2GSDS-33
4GB		HHW4GSDS-33
8GB		HHW8GSDS-33
16GB		HHW16GSDS-33
32GB		
64GB		

SD Card( MLC)		
Capacity	Normal-Temperature	Wide-temperature
4GB		HHW4GSDM-33
8GB		HHW8GSDM-33
16GB		HHW16GSDM-33
32GB		HHW32GSDM-33
64GB		HHW64GSDM-33
128GB		HHW128GSDM-33
256GB		HHW256GSDM-33

SD Card( aSLC)		
Capacity	Normal-Temperature	Wide-temperature
2GB		HHW2GSDA-33
4GB		HHW4GSDA-33
8GB		HHW8GSDA-33
16GB		HHW16GSDA-33
32GB		HHW32GSDA-33
64GB		HHW64GSDA-33
128GB		HHW128GSDA-33