MPQ4262

36V, 100W Buck-Boost Converter with Integrated Low-Side MOSFETS and an I²C Interface for Automotive, AEC-Q100

DESCRIPTION

The MPQ4262 is a buck-boost converter with two integrated low-side power MOSFETs (LS-FETs). The device can deliver up to 100W of peak output power at certain input voltage (V_{IN}) supply ranges with excellent efficiency.

The MPQ4262 is suitable for USB power delivery (USB PD) applications. It can work with an external USB PD controller through the I²C interface. The I²C interface and one-time programmable (OTP) memory provide flexible, configurable parameters.

Fault condition protections includes CC current limiting, output over-voltage protection (OVP), and thermal shutdown (TSD).

The MPQ4262 requires a minimal number of readily available, standard external components. It is available in a QFN-20 (3mmx5mm) package.

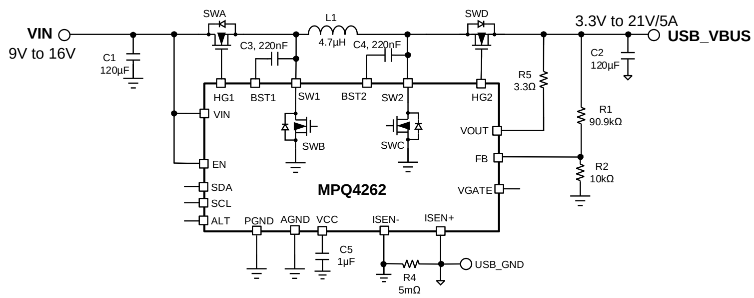
FEATURES

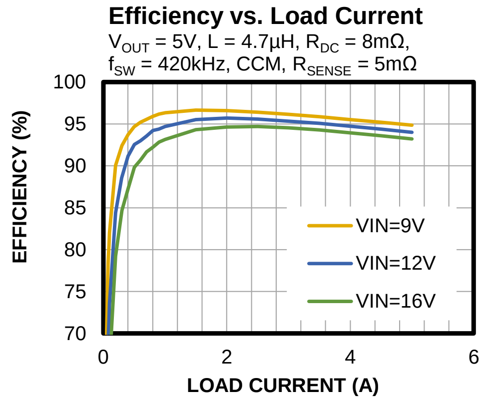
- 100W Buck-Boost Converter with Integrated Low-Side MOSFETs (LS-FETs)
- Integrated Gate Driver for High-Side Power MOSFETs (HS-FETs)
- 3.6V to 36V Start-Up Input Voltage (V_{IN}) Range
- Supports 2.8V Falling V_{IN} when the Output Voltage (V_{OUT}) > 3.5V
- 1V to 36V V_{OUT} Range
- Up to 5A Output Current (I_{OUT})
- Up to 98% Peak Efficiency
- I²C-Configurable Reference Voltage (V_{REF}) Range: 0.1V to 2.147V with 1mV Resolution
- Accurate Output CC Current Limit: ±5%
- Meets USB PD 3.0 with PPS Specification
- Selectable 280kHz, 420kHz, or 580kHz Switching Frequency (f_{SW})
- Selectable Forced PWM Mode or Automatic PFM/PWM Mode
- Output Bias VCC LDO for Higher Efficiency
- Ground Short to Battery Protection
- Line Drop Compensation via R_{SENS}
- I²C, Alert, and One-Time Programmable (OTP) Memory
- EN Shutdown Passive Discharge
- Output OCP, OVP, and Thermal Shutdown Protection
- Available in a QFN-20 (3mmx5mm) Package with Wettable Flank
- Available in AEC-Q100 in Grade 1

APPLICATIONS

- USB Power Delivery Hubs
- USB Power Delivery Charging Ports
- Wireless Charging

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ4262GQVE-0000-AEC1	QFN-20 (3mmx5mm)	*See Below*	1
MPQ4262GQVE-0001-AEC1			
MPQ4262GQVE-0002-AEC1			
MPQ4262GQVE-xxxx-AEC1**			

* For Tape & Reel, add suffix -Z (e.g. MPQ4262GQVE-xxxx-AEC1-Z).

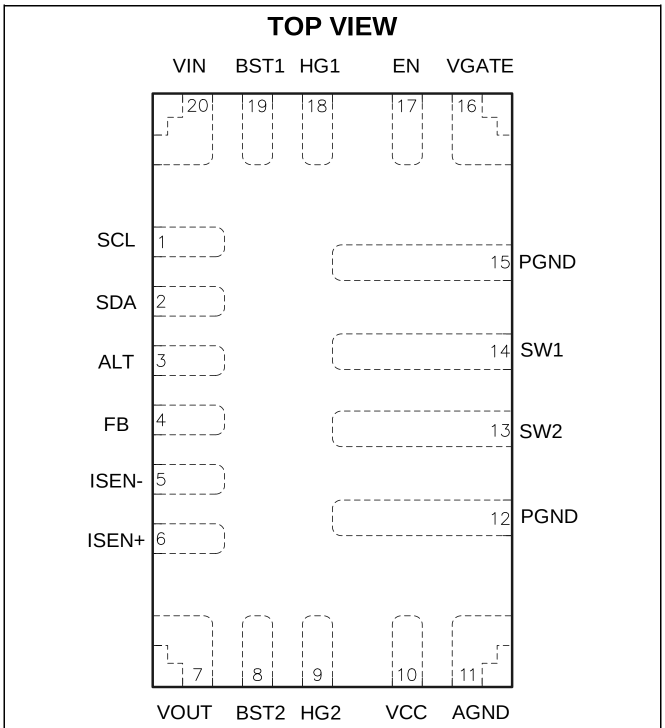
** “xxxx” is the configuration code identifier for the register setting stored in the MTP. The default number is “0000”. Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0000” code.

TOP MARKING

MPYW
4262
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
4262: Part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-20 (3mmx5mm) with Wettable Flank

PIN FUNCTIONS

Pin #	Name	Description
1	SCL	**I²C clock signal input.**
2	SDA	**I²C data line.**
3	ALT	**I²C alert pin.** Open-drain output, active low.
4	FB	**Feedback pin.** To set the output voltage, connect FB to the tap of an external resistor divider from the output to AGND.
5	ISEN-	**Negative node of the current-sense signal input.** Place a current-sense resistor between PGND and the output capacitor (C_{OUT}) at ground. Then connect the ISEN- pin to the PGND side.
6	ISEN+	**Positive node of current-sense signal input.** Place a current-sense resistor between PGND and the output capacitor (C_{OUT}) at ground. Then connect the ISEN+ pin to the C_{OUT} side.
7	VOUT	**Output voltage sense input.** The VOUT pin provides the VCC supply under certain V_{OUT} conditions.
8	BST2	**Bootstrap.** A 0.22μF capacitor should be Kelvin connected from the SW2 pin to the BST2 pin to form a floating supply across the high-side switch driver.
9	HG2	**High-side gate driver 2 output for the boost high-side switch (SWD).**
10	VCC	**Internal 5V LDO regulator output.** Decouple VCC with a 1μF to 4.7μF capacitor.
11	AGND	**Analog ground.** Connect AGND to PGND, then connect AGND to the VCC capacitor's ground node.
12, 15	PGND	**Power ground.** PGND requires additional consideration during PCB layout. Connect PGND to ground with copper traces and vias.
13	SW2	**Switch 2 node of the buck-boost.** Connect SW1 to SW2 with a power inductor. Use a wide PCB trace to make this connection.
14	SW1	**Switch 1 node of the buck-boost.** Connect SW1 to SW2 with a power inductor. Use a wide PCB trace to make this connection.
16	VGATE	**Gate driver pin to drive the external MOSFET.** The external MOSFET provides ground short to battery protection.
17	EN	**EN input.** Apply logic high to enable the chip.
18	HG1	**High-side gate driver 1 output for the buck high-side switch (SWA).**
19	BST1	**Bootstrap.** A 0.22μF capacitor should be Kelvin connected from the SW1 pin to the BST1 pin to form a floating supply across the high-side switch driver.
20	VIN	**Supply voltage for internal logic circuitry, but not for the power MOSFETs.** Kelvin connect the VIN pin to the SWA MOSFET's drain with a wide PCB trace. The VIN trace cannot supply power to other DC/DC converters.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage (V_{IN})..................... -0.4V to +40V
V_{SW1}.............................-0.3V (-8V for <10ns)
.....................to V_{IN} + 0.3V (+43V for <10ns)
V_{SW2} ....-0.3V (-8V for <10ns)
.... to V_{OUT} + 0.3V (+43V for <10ns)
$V_{BST1/2}$ .... $V_{SW1/2}$ + 6V
V_{OUT} .... -0.3V to +40V
V_{EN} .... -0.3V to +40V
V_{VCC} ....-0.3V to +6V (+7.5V for 500µs)
All other pins................................. -0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2) (5)
QFN-20 (3mmx5mm)...................................6W
Junction temperature .... 150°C
Lead temperature .... 260°C

ESD Ratings (3)

Human body model (HBM) ....±1.8kV
Charged device model (CDM)..................±750V

Recommended Operating Conditions (4)

Operating input voltage (V_{IN})........... 3.6V to 36V
Operating output voltage (V_{OUT}) .... 1V to 36V
Output current and power .... 5A or 100W
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance

Thermal Resistance	θ_{JA}	θ_{JC}	
EVQ4262-QVE-00A (5)	20.7	2.4	°C/W
QFN-20 (3mmx5mm) (6)	39.1	2.5	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (TJ (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
4) The device is not guaranteed to function outside of its operating conditions. A 26V V_{OUT} is the default absolute OVP threshold for MPQ4262-0000. If customer needs >23V output voltage, Vout absolute OVP must be changed to 37V or disabled in related suffix code part.
5) Measured on MPQ4262 test board, four layer PCB.
6) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{Q_STD}	V_{EN} = 0V		1	30	μA
Supply current (quiescent)	I_{Q1}	No switching, I²C set OPERATION on, EN on, PFM mode		775	1250	μA
	I_{Q2}	I²C set OPERATION = off, EN on		130	250	μA
EN rising threshold	V_{EN_RISING}	EN to enable switching	-5%	1.22	+5%	V
EN hysteresis	V_{EN_HYS}			200		mV
EN pull-down resistor	R_{EN}	EN = 2V		2	3	MΩ
Thermal shutdown (7)	T_{STD}			160		°C
Thermal hysteresis (7)	T_{STD_HYS}			20		°C
VCC regulator	V_{CC}	Steady state	4.85	5.15	5.45	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 50mA		2	5	%
VCC power source change threshold	V_{CC_VTH}	V_{IN} = 12V, ramp V_{OUT} from 5V to 10V	6.4	6.8	7.2	V
V_{CC} under-voltage lockout (UVLO) rising threshold	$V_{CC\_UVLO\_R}$		3.15	3.35	3.55	V
V_{CC} UVLO threshold hysteresis	$V_{CC\_UVLO\_HYS}$			200		mV
V_{IN} UVLO falling threshold	V_{UVLO_VIN}		2.35	2.55	2.75	V
Buck-Boost Converter						
Switch B on resistance	$R_{DS\_ON\_B}$			20	40	mΩ
Switch C on resistance	$R_{DS\_ON\_C}$			14	30	mΩ
Feedback voltage	V_{FB1}		-3%	330	+3%	mV
	V_{FB2}		-2%	500	+2%	mV
	V_{FB3}		-1.5%	2	+1.5%	V
Output over-voltage protection (OVP) rising threshold	$VOUT_{OVP\_R}$		114%	120%	126%	V_{FB}
Output OVP falling threshold	$VOUT_{OVP\_F}$		105%	110%	115%	V_{FB}
Output absolute OVP rising	$VOUT_{OVP\_ABS}$	The OTP can set this value up to 37V	24	26	28	V
Output absolute OVP hysteresis	$VOUT_{OVP\_ABS\_HYS}$			0.65		V
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW1} = 36V, V_{SW2} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW1} = 36V, V_{SW2} = 36V, T_J = -40°C to+125°C			30	
Hiccup off timer	t_{HICCUP}	V_{OUT} = 5V		400		ms
Oscillator frequency	f_{SW1}	T_J = 25°C	220	280	340	kHz

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Oscillator frequency	f_{SW2}	T_J = 25°C	340	420	500	kHz
	f_{SW3}	T_J = 25°C	480	580	680	kHz
Frequency dithering span	f_{SRANGE}			±7.5		%
Soft-start time	t_{SS}	Output from 10% to 90%, V_{OUT} = 5V, constant slew rate for other V_{REF}		1		ms
Minimum on time (7)	$t_{ON\_MIN\_BT}$	Boost SWC		180		ns
Minimum off time (7)	t_{OFF_MIN}	Buck SWB		180		ns
ISENS OC threshold	I_{OC1}	OC threshold = 1A, R_{SENS} = 5mΩ	4.25	5	5.75	mV
	I_{OC2}	OC threshold = 3.6A, R_{SENS} = 5mΩ	-5%	18	+5%	mV
Low-side B valley limit	I_{LIMIT2}	Switch B, 0XD3, bits D[7:6] = 10b		13		A
Low-side C peak current limit	I_{LIMIT3}	Switch C, 0XD3, bits D[7:6] = 10b		15	20	A
Line drop compensation	V_{DROP}	I_{OUT} = 1A		100		mV
Output discharge resistor	R_{DISCHG}			75	150	Ω
Mode Transition Threshold						
Buck-boost to buck transition threshold (7)	V_{MODE_TH2}	V_{IN} / V_{OUT}		120		%
Buck-boost to boost transition hysteresis (7)	V_{MODE_HYS2}	V_{IN} / V_{OUT}		82		%
High-side Gate Driver						
Gate source current capability (7)	$I_{HS1\_HS3\_SRC}$	V_{BST-SW} = 5.2V, 4.7nF load		0.8		A
	$I_{HS2\_HS4\_SRC}$	V_{BST-SW} = 5.2V, 4.7nF load		1.2		A
Gate source resistance	$R_{HS1\_HS3\_SRC}$	V_{BST-SW} = 5.2V		3	5	Ω
	$R_{HS2\_HS4\_SRC}$	V_{BST-SW} = 5.2V		2	3	Ω
Gate sink current capability (7)	$I_{HS1\_HS3\_SIN}$	V_{BST-SW} = 5.2V, 4.7nF load		1.8		A
	$I_{HS2\_HS4\_SIN}$	V_{BST-SW} = 5.2V, 4.7nF load		3.3		A
Gate sink resistance	$R_{HS1\_HS3\_SIN}$	V_{BST-SW} = 5.2V		1	2	Ω
	$R_{HS2\_HS4\_SIN}$	V_{BST-SW} = 5.2V		1	2	Ω
ALT pin leakage	I_{ALT_LKG}	V_{ALT} = 5V		0.1		μA
ALT pin pull low resistance	R_{ALT}				15	Ω

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I²C Interface Specifications (7)						
Input logic high	V_{IH}		1.25			V
Input logic low	V_{IL}				0.6	V
Output voltage logic low	V_{OUT_L}				0.4	V
SCL clock frequency	f_{SCL}			400	1000	kHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}		0	60		ns
Set-up time for (repeated) start command	t_{SU_STA}		160			ns
Hold time for (repeated) start command	t_{HD_STA}		160			ns
Bus free time between a start and a stop command	t_{BUF}		160			ns
Set-up time for stop command	t_{SU_STO}		160			ns
Rising time of SCL and SDA	t_R		10		300	ns
Falling time of SCL and SDA	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance for each bus line	C_B				400	pF
Power Good (PG) Indication						
PG lower rising threshold	$V_{PG\_R\_L}$	PG switches high	88.5%	93%	98.5%	V_{FB}
PG lower falling threshold	$V_{PG\_F\_L}$	PG switches low	77%	82.5%	88%	V_{FB}
PG upper rising threshold	$V_{PG\_R\_H}$	PG switches low	115%	120.5%	126%	V_{FB}
PG upper falling threshold	$V_{PG\_F\_H}$	PG switches high	105%	110%	115%	V_{FB}
Short to Battery Protection						
GND short to battery ISENS threshold	I_{SC}	OC threshold = 20A, R_{SENS} = 5mΩ		100		mV
Short to battery retry delay	t_{SC_RTY}			70		ms
Gate pull-down resistance	R_{SC_PD}			7		Ω

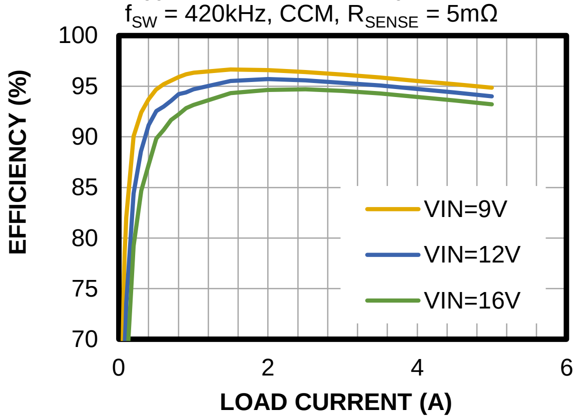
Note:

7) Guaranteed by characterization.

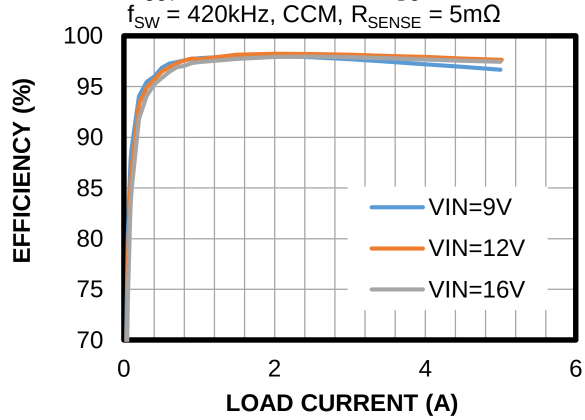
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

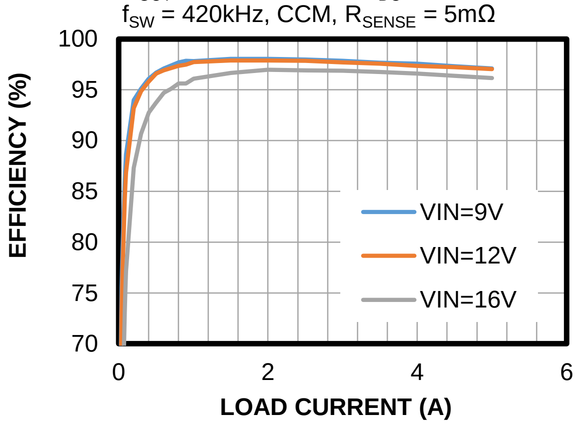
Efficiency vs. Load Current
V_{OUT} = 5V, L = 4.7µH, R_{DC} = 8mΩ,
f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



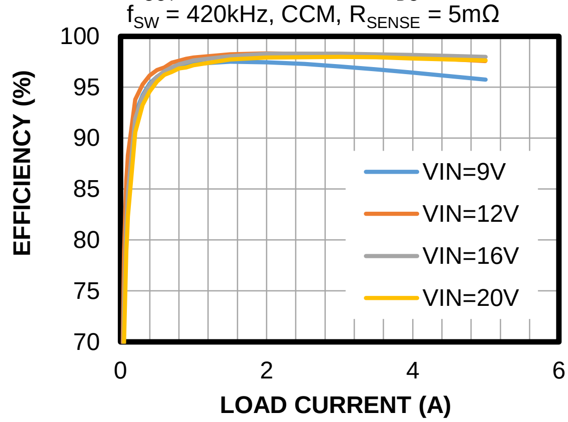
Efficiency vs. Load Current
V_{OUT} = 12V, L = 4.7µH, R_{DC} = 8mΩ,
f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



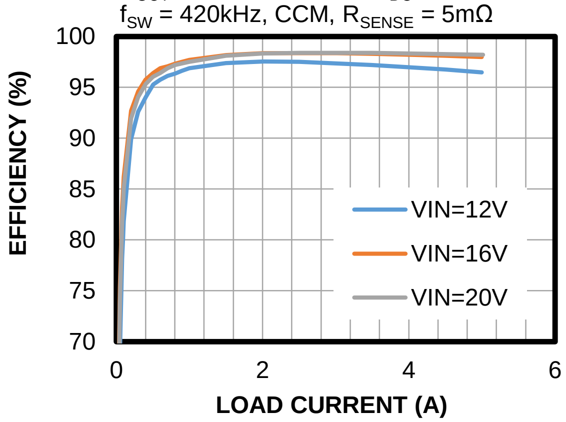
Efficiency vs. Load Current
V_{OUT} = 9V, L = 4.7µH, R_{DC} = 8mΩ,
f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



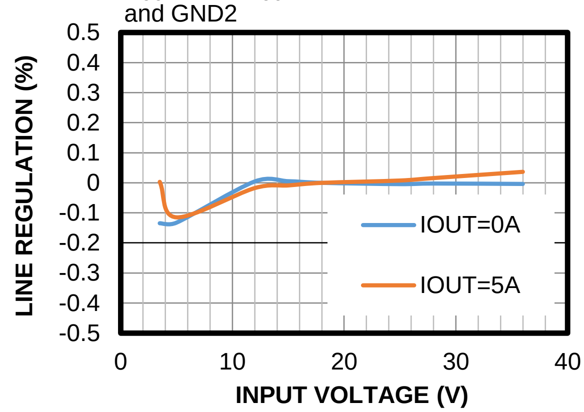
Efficiency vs. Load Current
V_{OUT} = 15V, L = 4.7µH, R_{DC} = 8mΩ,
f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



Efficiency vs. Load Current
V_{OUT} = 20V, L = 4.7µH, R_{DC} = 8mΩ,
f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



Line Regulation
V_{OUT} = 5V, V_{OUT} measured between VOUT and GND2

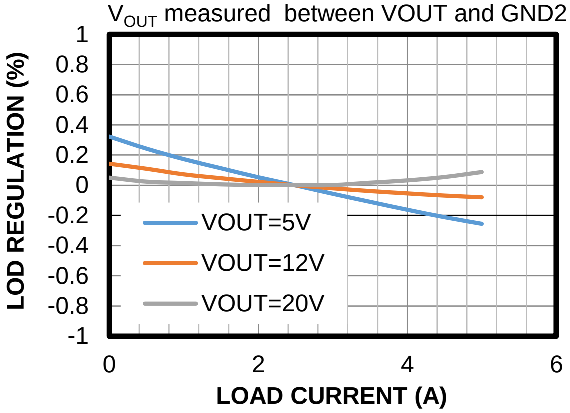


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

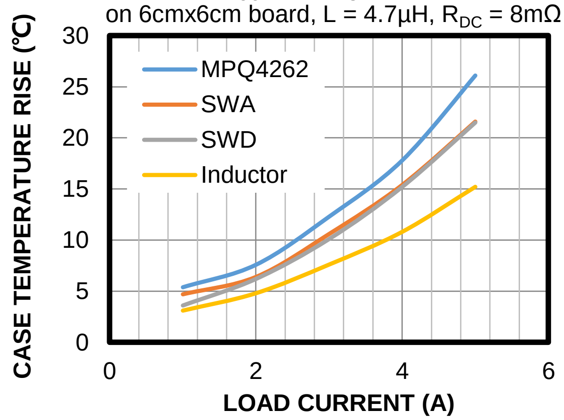
Load Regulation

R_{SENSE} = 5mΩ, no line drop compensation, V_{OUT} measured between VOUT and GND2



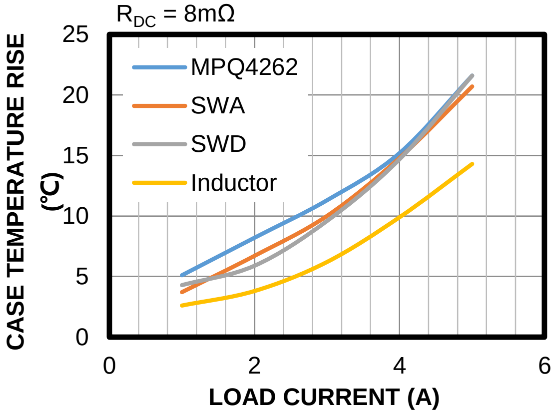
Case Temperature Rise

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 420kHz, based on 6cmx6cm board, L = 4.7µH, R_{DC} = 8mΩ



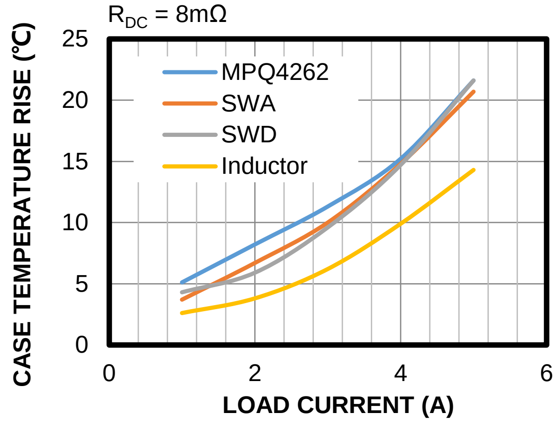
Case Temperature Rise

V_{IN} = 12V, V_{OUT} = 12V, f_{SW} = 420kHz, based on 6cmx6cm board, L = 4.7µH, R_{DC} = 8mΩ

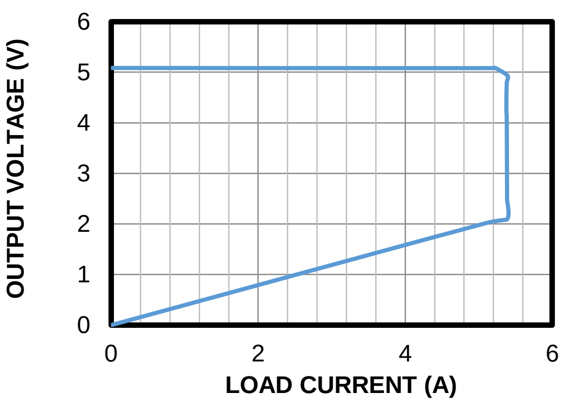


Case Temperature Rise

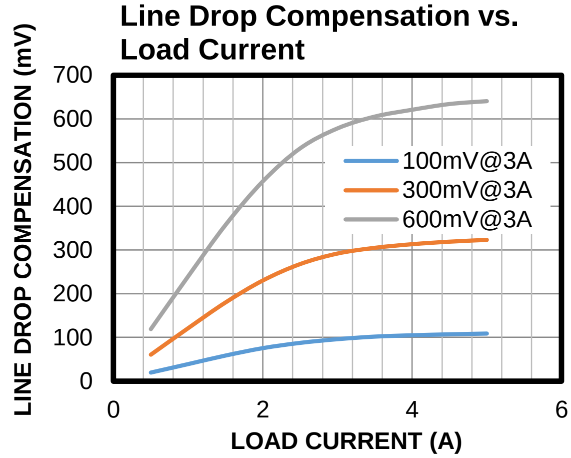
V_{IN} = 12V, V_{OUT} = 12V, f_{SW} = 420kHz, based on 6cmx6cm board, L = 4.7µH, R_{DC} = 8mΩ



CC/CV Curve

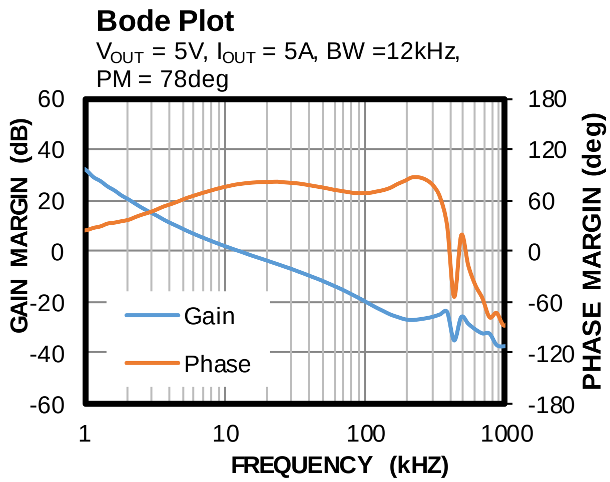


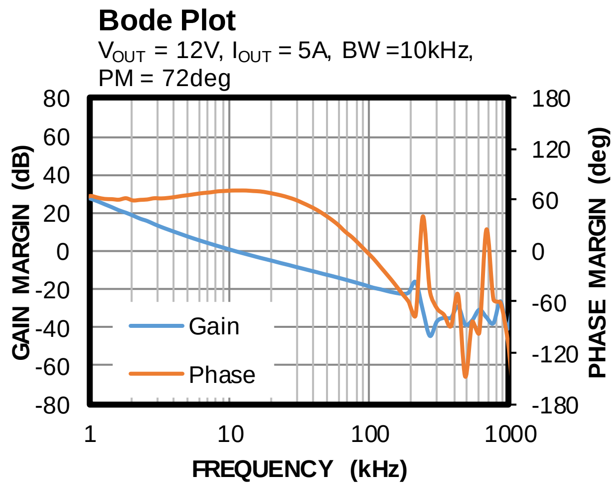
Line Drop Compensation vs. Load Current

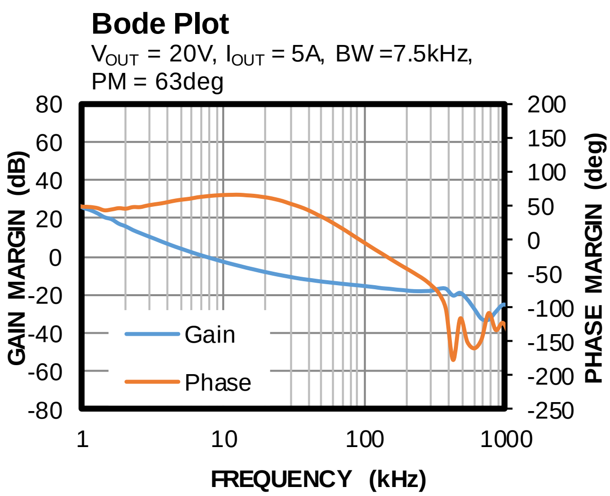


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.





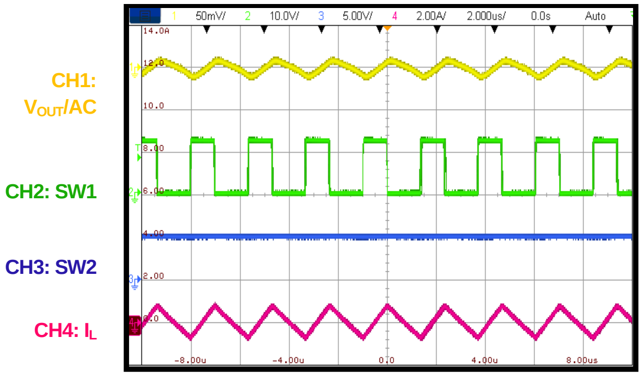


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

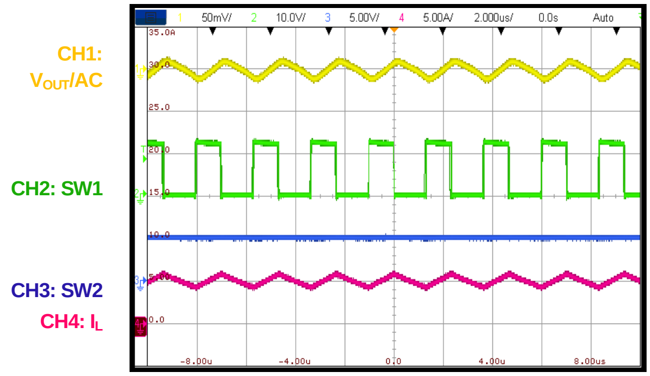
Output Voltage Ripple

V_{OUT} = 5V, load = 0A



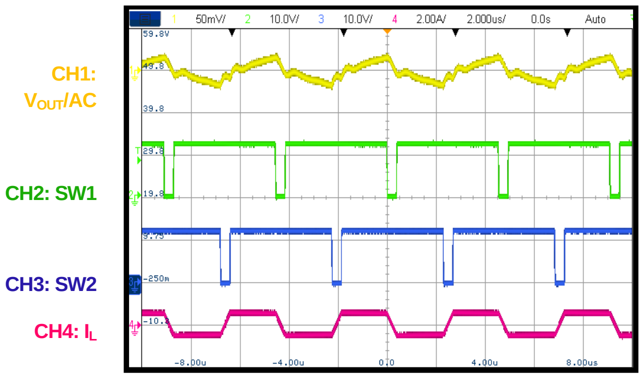
Output Voltage Ripple

V_{OUT} = 5V, load = 5A



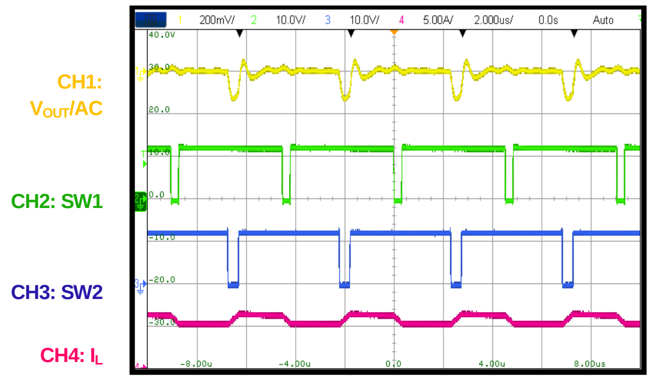
Output Voltage Ripple

V_{OUT} = 12V, load = 0A, f_{SW} decreased to half its value in buck-boost mode



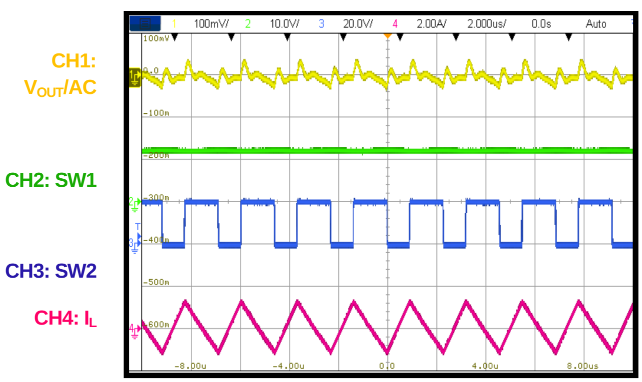
Output Voltage Ripple

V_{OUT} = 12V, load = 5A, f_{SW} decreased to half its value in buck-boost mode



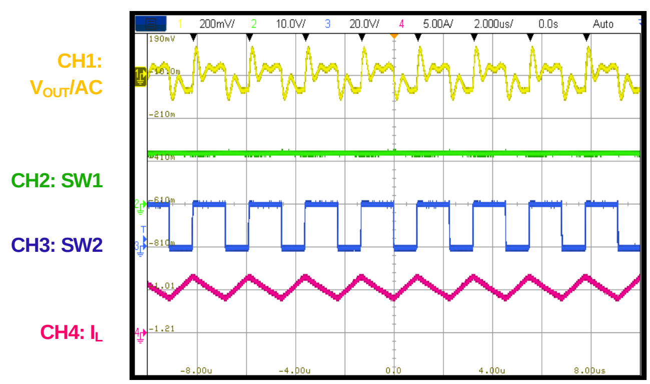
Output Voltage Ripple

V_{OUT} = 20V, load = 0A



Output Voltage Ripple

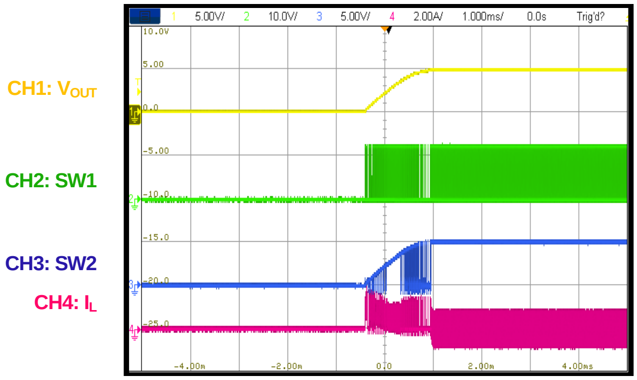
V_{OUT} = 20V, load = 3A



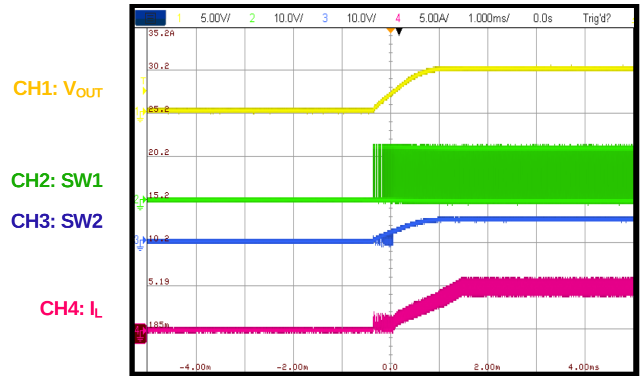
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

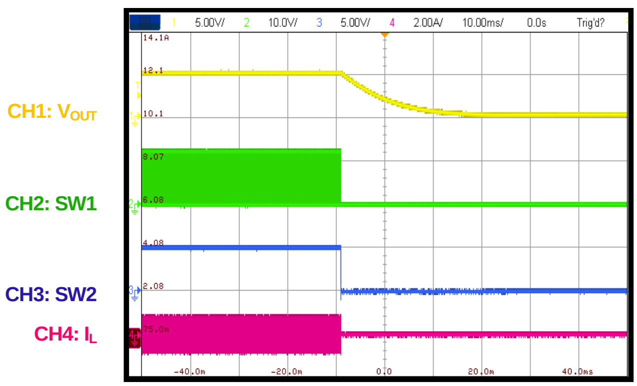
I^{2}C Operation On
Load = 0A



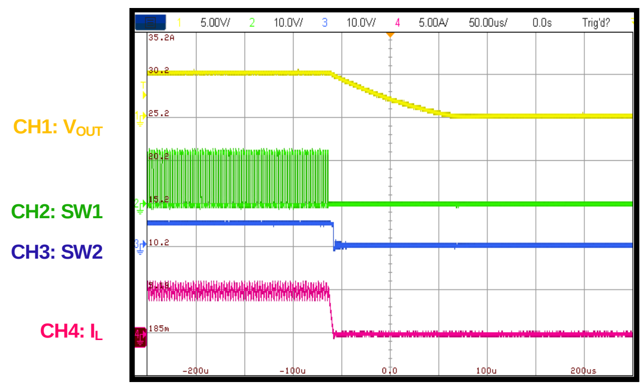
I^{2}C Operation On
Load = 5A



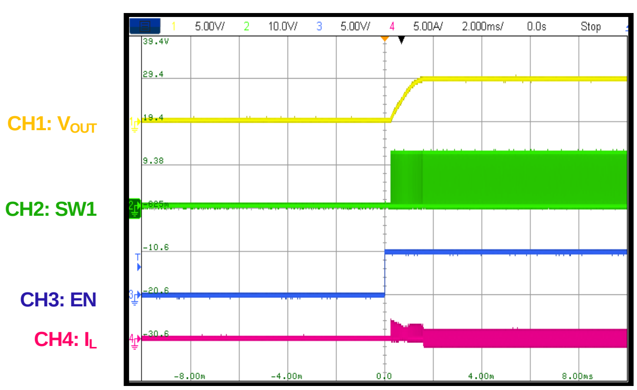
I^{2}C Operation Off
Load = 0A



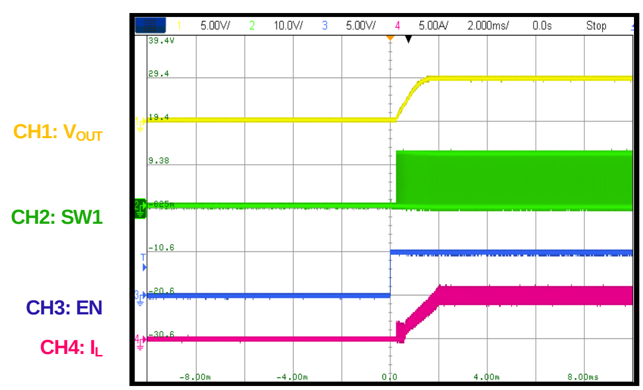
I^{2}C Operation Off
Load = 5A



EN Pin Enabled
Load = 0A



EN Pin Enabled
Load = 5A

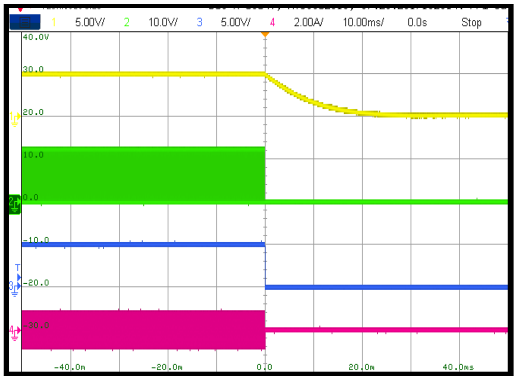


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

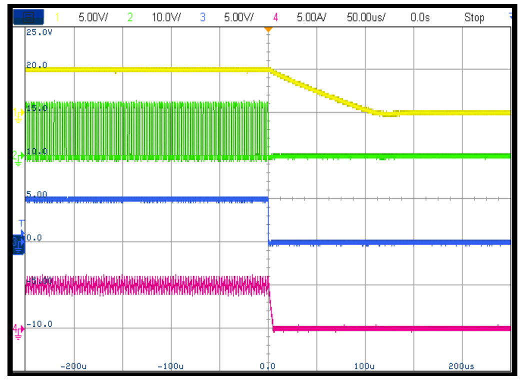
EN Pin Disabled
Load = 0A

CH1: V_{OUT}
CH2: SW1
CH3: EN
CH4: I_L



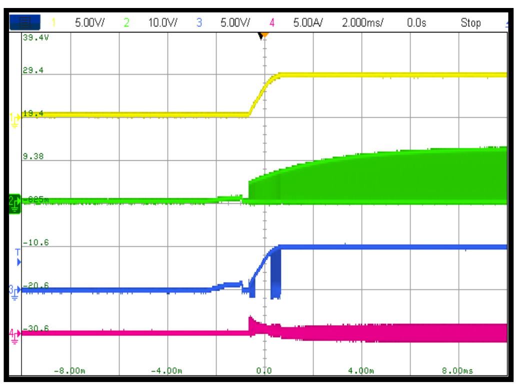
EN Pin Disabled
Load = 5A

CH1: V_{OUT}
CH2: SW1
CH3: EN
CH4: I_L



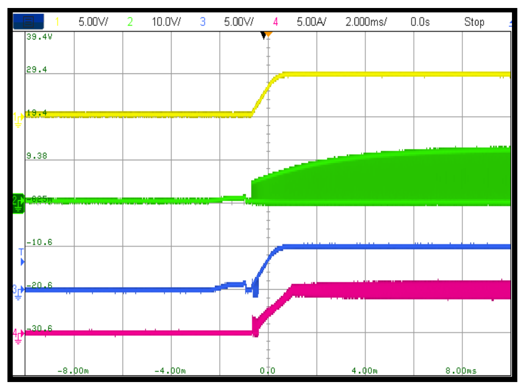
Input Start-Up
Load = 0A

CH1: V_{OUT}
CH2: SW1
CH3: SW2
CH4: I_L



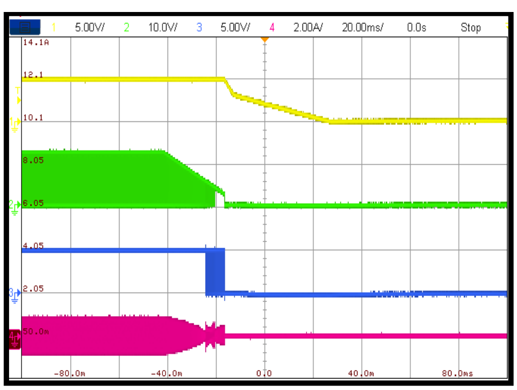
Input Start-Up
Load = 5A

CH1: V_{OUT}
CH2: SW1
CH3: SW2
CH4: I_L



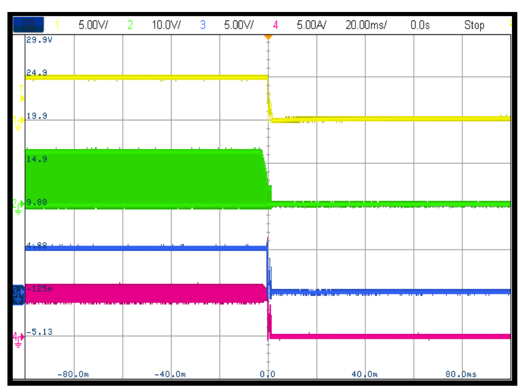
Input Shutdown
Load = 10mA

CH1: V_{OUT}
CH2: SW1
CH3: SW2
CH4: I_L



Input Shutdown
Load = 5A

CH1: V_{OUT}
CH2: SW1
CH3: SW2
CH4: I_L

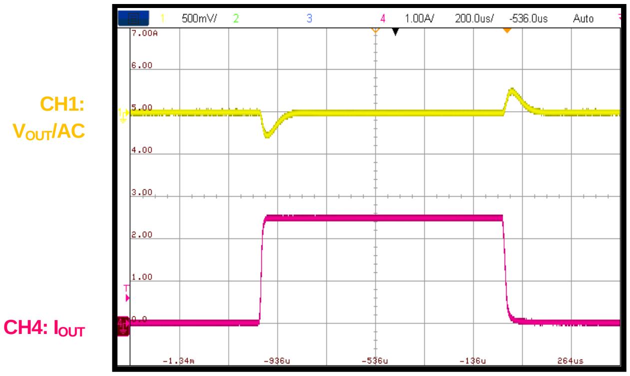


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

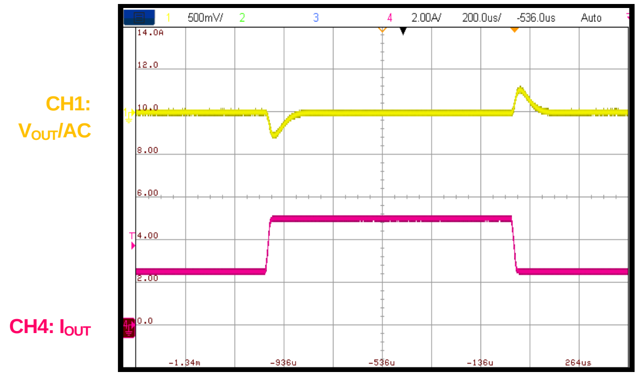
Load Transient Response

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A to 2.5A, 150mA/µs



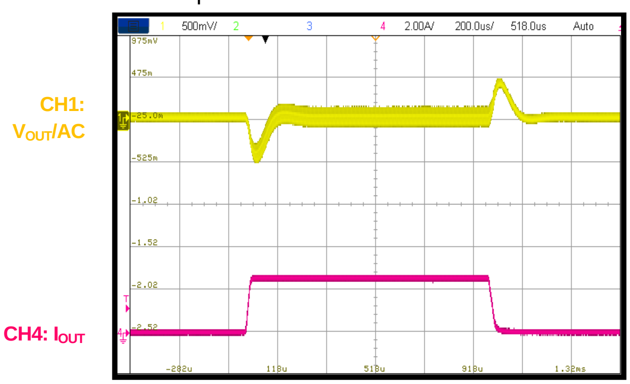
Load Transient Response

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2.5A to 5A, 150mA/µs



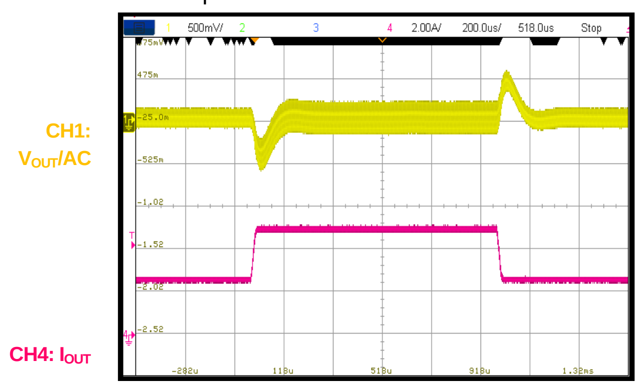
Load Transient Response

V_{IN} = 12V, V_{OUT} = 20V, I_{OUT} = 0A to 2.5A, 150mA/µs



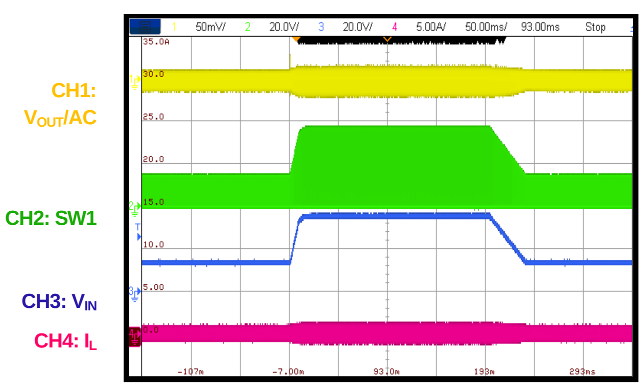
Load Transient Response

V_{IN} = 12V, V_{OUT} = 20V, I_{OUT} = 2.5A to 5A, 150mA/µs



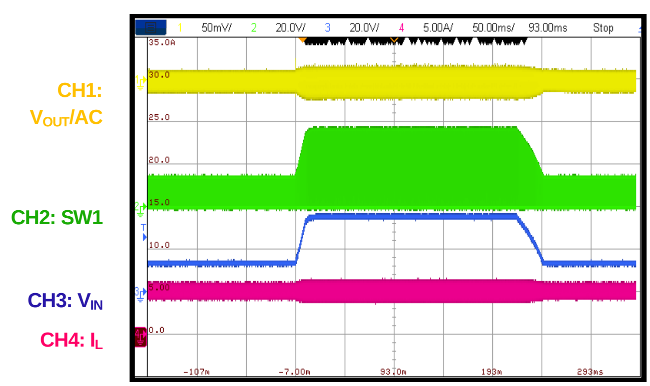
Input Voltage Transient Response

V_{IN} = 14V to 35V, V_{OUT} = 5V, load = 0A



Input Voltage Transient Response

V_{IN} = 14V to 35V, V_{OUT} = 5V, load = 5A

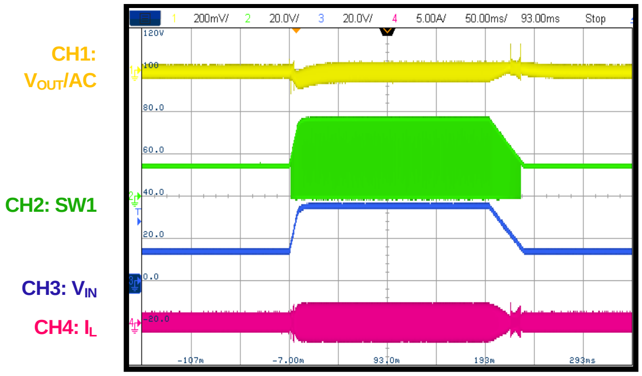


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

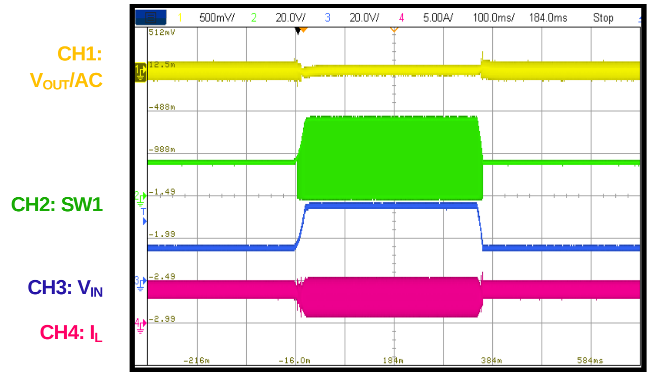
Input Voltage Transient

V_{IN} = 14V to 35V, V_{OUT} = 20V, load = 0A



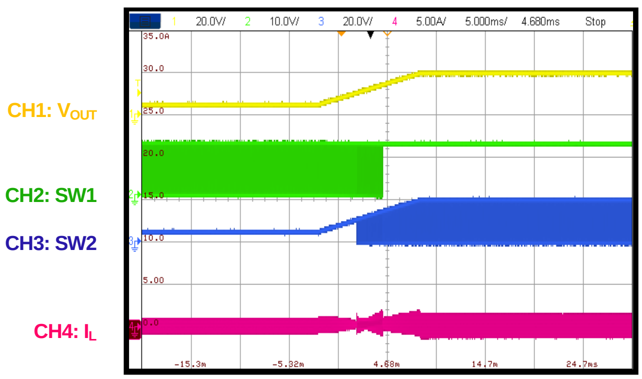
Input Voltage Transient

V_{IN} = 14V to 35V, V_{OUT} = 20V, load = 3A



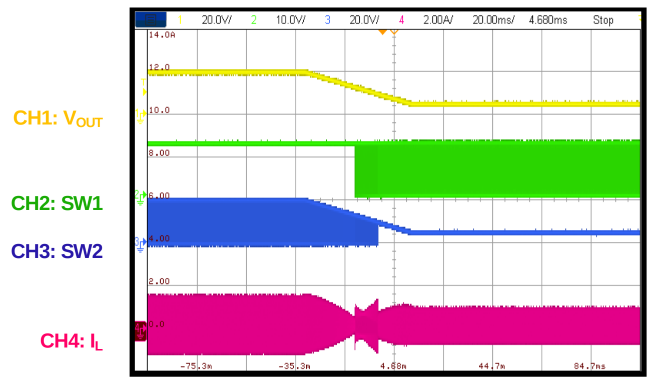
Output Voltage Transition

V_{OUT} = 5V to 20V, I_{OUT} = 0A



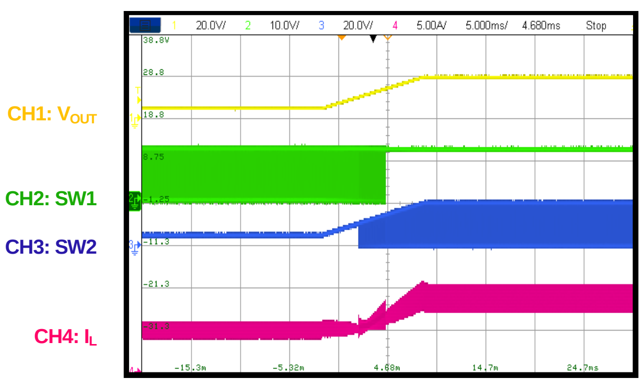
Output Voltage Transition

V_{OUT} = 20V to 5V, I_{OUT} = 0A



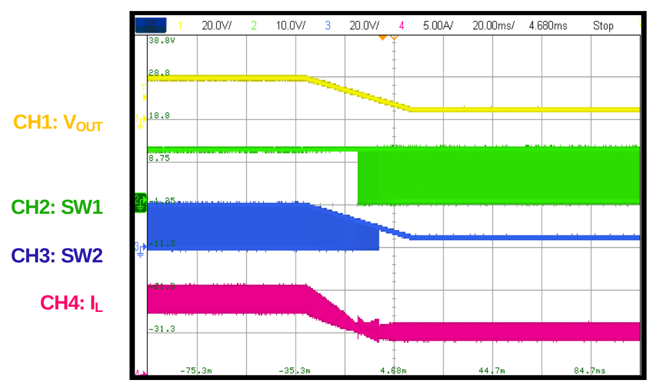
Output Voltage Transition

V_{OUT} = 5V to 20V, I_{OUT} = 3A



Output Voltage Transition

V_{OUT} = 20V to 5V, I_{OUT} = 3A

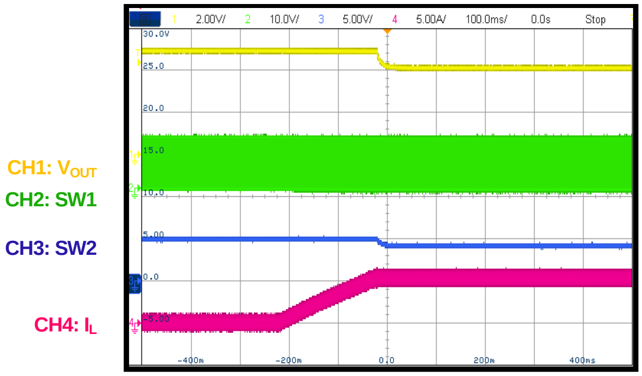


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

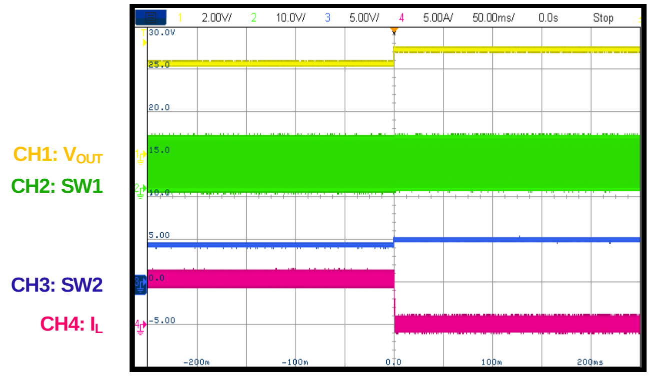
CC Entry

CV load = 4V, CC limit = 5.4A

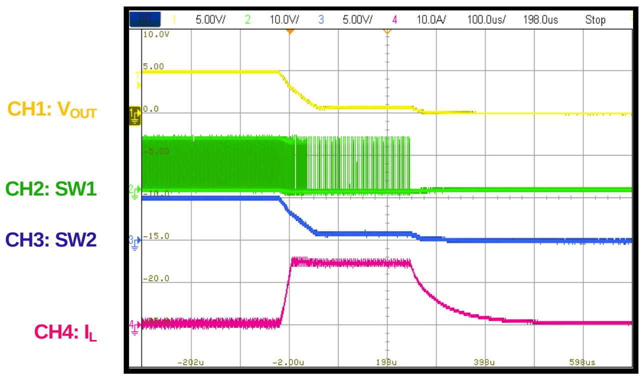


CC Recovery

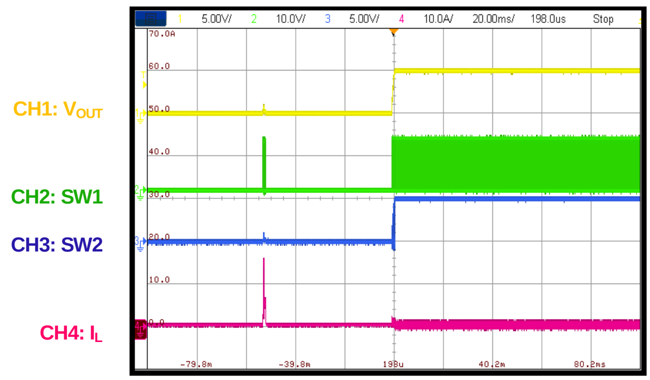
CV load = 4V, CC limit = 5.4A



Short-Circuit Protection Entry



Short-Circuit Protection Recovery



FUNCTIONAL BLOCK DIAGRAM

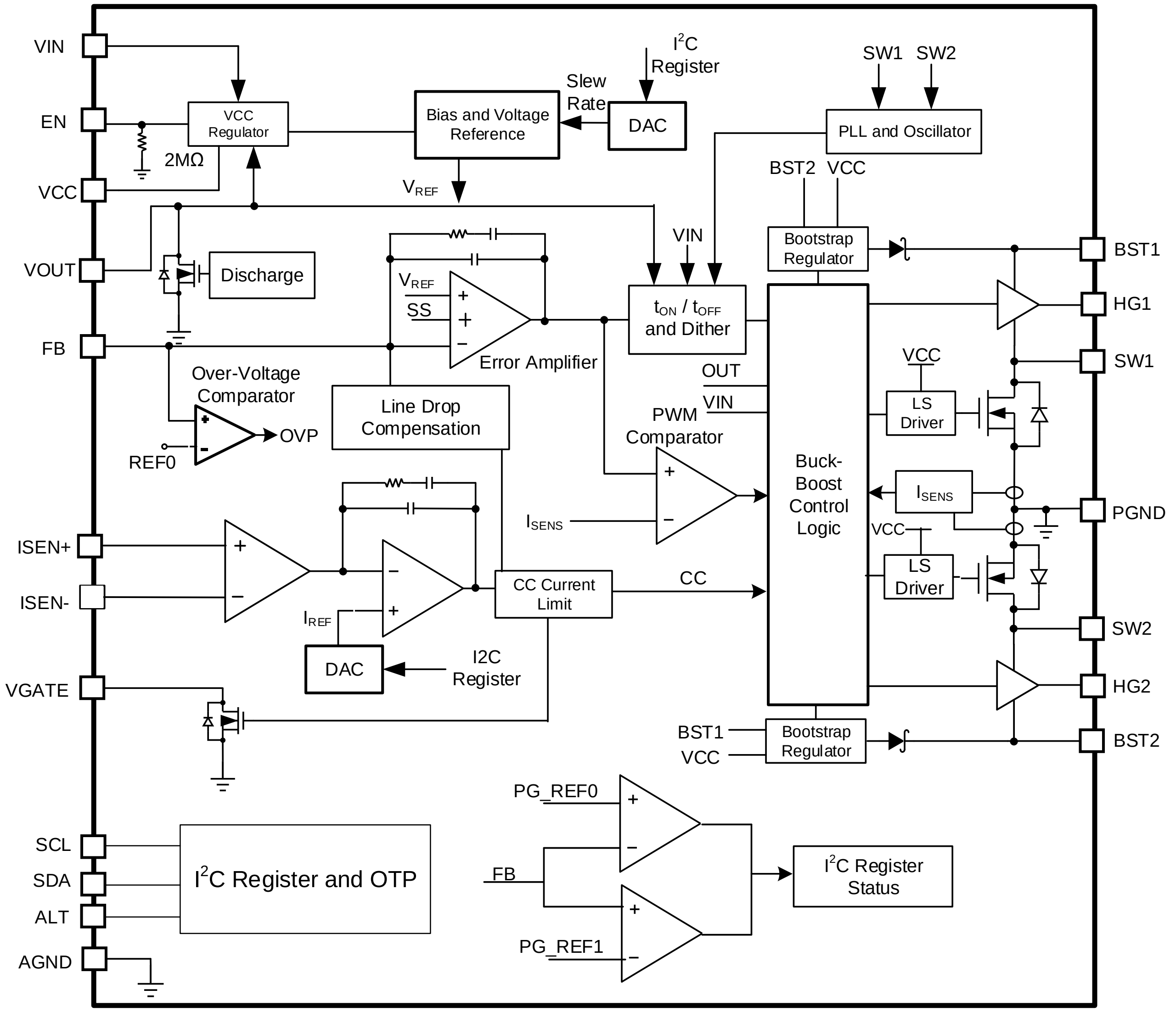


Figure 1: Functional Block Diagram

OPERATION

The MPQ4262 is a buck-boost converter with integrated low-side MOSFETs (LS-FETs). The device works with a fixed frequency for buck, boost, and buck-boost mode. A special buck-boost control strategy provides high efficiency across the full input range and smooths the transient response between different modes. Figure 1 on page 18 shows the internal block diagram.

Buck-Boost Operation

The MPQ4262 can regulate the output voltage (V_{OUT}) to be above, below, or equal to the input voltage (V_{IN}). Figure 2 shows a buck-boost power structure with one inductor and four switches (SWA, SWB, SWC, and SWD).

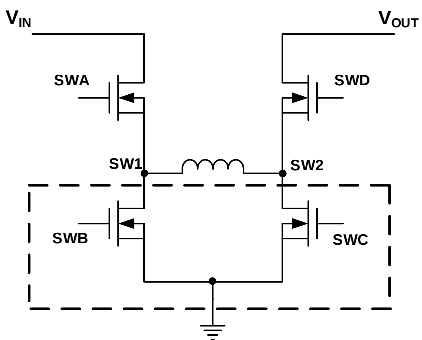


Figure 2: Buck-Boost Topology

Buck mode, boost mode, and buck-boost mode can have different V_{IN} inputs (see Figure 3).

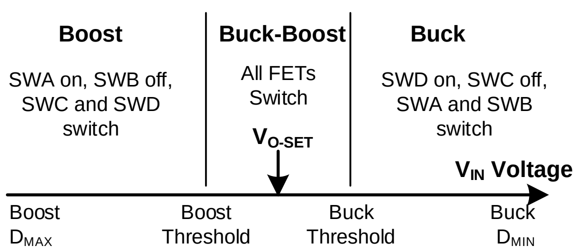


Figure 3: Buck-Boost Operation Range

Buck Mode ($V_{IN} > V_{OUT}$)

When V_{IN} exceeds V_{OUT}, the MPQ4262 works in buck mode. In buck mode, switch A (SWA) and switch B (SWB) switch for buck regulation. Meanwhile, switch C (SWC) is off, and switch D (SWD) stays on to conduct the inductor current (I_L).

In each buck mode cycle, SWA turns on first when the FB voltage (V_{FB}) drops below the reference voltage (V_{REF}). After SWA turns off, SWB turns on to conduct I_L until it triggers the COMP control signal. By repeating this operation, the converter regulates V_{OUT}.

Boost Mode ($V_{IN} < V_{OUT}$)

When V_{IN} is below V_{OUT}, the MPQ4262 works in boost mode. In boost mode, SWC and SWD switch for boost regulation. Meanwhile, SWB is off and SWA stays on to conduct the inductor current.

In each boost mode cycle, SWC turns on to conduct I_L. When I_L rises and triggers the control signal on the COMP pin, SWC turns off and SWD turns on for the current freewheeling period. Then SWC turns on and off repeatedly to regulate V_{OUT} in boost mode.

Buck-Boost Mode ($V_{IN} \approx V_{OUT}$)

When V_{IN} is almost equal to V_{OUT}, the converter cannot provide enough energy to the load in buck mode due to SWA's minimum off time. In boost mode, the converter supplies too much power to the load due to SWC's minimum on time. Under these conditions, the MPQ4231C adopts buck-boost control to regulate the output (see Figure 4).

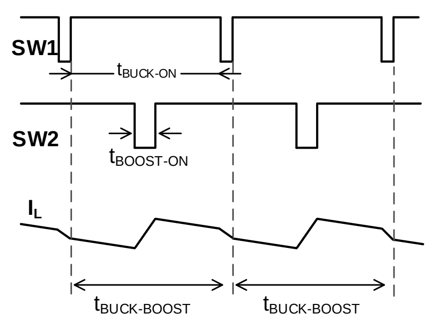


Figure 4: Buck-Boost Waveform

If V_{IN} is almost equal to V_{OUT}, buck-boost mode activates. One boost switching period is inserted into each buck switching period. The MOSFET turn-on sequence is as follows:

1. SWA and SWD
2. SWA and SWC
3. SWA and SWD
4. SWB and SWD

Throughout this process, I_L can reach the COMP voltage requirement, and supply enough current to the output.

Mode Selection

The MPQ4262 works with a fixed frequency under heavy-load conditions. When the load current decreases, the MPQ4262 can work in forced continuous conduction mode (FCCM) or pulse-skip mode (PSM) based on the MODE register setting.

Forced Continuous Conduction Mode (FCCM) or Forced Pulse-Width Modulation (PWM) Mode

In forced continuous condition mode (FCCM), the buck on time and boost off time are determined by the internal circuit to achieve a fixed frequency based on the V_{IN} / V_{OUT} ratio. When the load decreases, the average input current drops, and I_L may go negative from V_{OUT} to V_{IN} during the off time (SWD on). This forces the inductor current to work in continuous mode with a fixed frequency, producing a lower output voltage ripple than in PSM mode.

PSM and Automatic PFM/PWM Mode

In power-save mode (PSM), once I_L drops to 0A, SWD turns off to prevent the current from flowing from the output to GND, forcing I_L to work in discontinuous conduction mode (DCM). Simultaneously, the internal off time clock becomes longer once the MPQ4262 enters DCM. The frequency drops when the inductor current conduction period decreases, which reduces power loss and the output voltage ripple.

If V_{COMP} drops to the PSM threshold, the MPQ4262 stops switching to reduce switching power loss. The MPQ4262 starts switching once V_{COMP} rises above the PSM threshold. The switching pulse skips are based on V_{COMP} under light-load conditions. PSM has a much higher efficiency than FCCM with light loads, but the output voltage ripple may be higher due to the group switching pulse.

Power Supply

The MPQ4262's internal circuit is powered by VCC, including the driver gates. When V_{IN} is supplied power and EN is high, the MPQ4262 tries to regulate V_{CC} at 5V. V_{CC} and BST have separate under-voltage lockout (UVLO) thresholds that keep the gate signal off.

If V_{IN} and V_{OUT} both exceed 8V, the MPQ4262 powers VCC from the lower voltage source to reduce power loss. Otherwise, the MPQ4262 powers VCC from the higher voltage power source between V_{IN} and V_{OUT}. Both VCC and BST should have sufficient voltages to enable MPQ4262 switching.

EN Control

The MPQ4262 has an enable control pin (EN). Pull EN high to enable the IC. Pull EN low or float EN to disable the IC.

The EN pin is a high-voltage pin that can be connected to VIN directly or through a resistor. An EN resistor divider can determine V_{IN}'s on and off thresholds. It is recommended to use a resistor when using an external analog signal to control EN (see Figure 5).

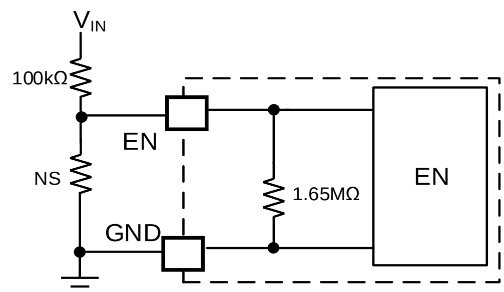


Figure 5: EN Connection

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input and VCC voltage. The MPQ4262 is enabled when V_{CC} exceeds its rising UVLO threshold; the MPQ4262 stops working when either V_{IN} or V_{CC} fall below their UVLO falling thresholds.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates an SS voltage (V_{SS}) that ramps up from 0V to 5V. When V_{SS} is below V_{REF}, the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference.

If the output of the MPQ4262 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

CC Mode Over-Current-Protection

The MPQ4262 senses the ground current by the ISEN+ and ISEN- pins. If the output current (I_{OUT}) exceeds the set current limit threshold, the MPQ4262 enters constant current limit mode (CC mode). In CC mode, the current amplitude is limited. After the load resistance is reduced, V_{OUT} drops, and V_{FB} falls below the under-voltage (UV) threshold (about 40% below V_{REF}).

If a UV condition is triggered and V_{OUT} is below 3V, the MPQ4262 enters hiccup mode to periodically restart the part. This protection is useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4262 exits hiccup mode once the over-current (OC) condition is removed.

Switching Current Limit

The MPQ4262 senses the LS-FET current in loop control, then provides the valley current limit in buck mode, as well as the peak current limit in boost mode for each cycle-by-cycle switch. In buck mode, the next period does not start before I_L drops to the valley current limit. This folds back the frequency when the valley current limit is triggered.

Based on the cycle-by-cycle switching current limit, the MPQ4262's maximum input current in buck mode can be calculated with Equation (1):

$$I_{INMAX}(A) = \frac{V_{OUT}}{V_{IN}} \times \eta \times (\text{ValleyCurrentLimit}(A) + \frac{V_{IN} - V_{OUT}}{2 \times L(\mu H) \times f(kHz)} \times \frac{V_{OUT}}{V_{IN}} \times 10^3) \quad (1)$$

Where η is the efficiency. The maximum input current in boost mode can be estimated with Equation (2):

$$I_{INMAX}(A) = \text{PeakCurrentLimit}(A) - \frac{V_{IN}}{2 \times L(\mu H) \times f(kHz)} \times \frac{V_{OUT} - V_{IN}}{V_{OUT}} \times 10^3 \quad (2)$$

Typically, the buck valley current limit is 13A, while the boost peak current limit is 15A. These limits can be configured by the I²C register (0xD3, bits D[7:6]).

Output Over-Voltage Protection (OVP)

The MPQ4262 has output over-voltage protection (OVP). If V_{OUT} exceeds 120% of V_{REF}, the switches (SWA, SWB, SWC, and SWD) turn off. A resistor discharge path from the VOUT pin to ground turns on. When the feedback output voltage drops to 110% of V_{REF}, the chip returns to normal operation.

The absolute output OVP threshold can be configured from 26V or 37V, and the default is 26V. Absolute OVP can be disabled by setting OUTPUT_OVP_EN to 0. A discharge resistor turns on when the absolute OVP threshold is triggered. If the output is biased by an external power supply, the output reverse current should be below 1.5A.

Gate Driver and BST Power

The MPQ4262 provides two N-channel MOSFET gate drivers for the H-bridge MOSFETs. Each driver can source and sink current. In buck mode, HG1 switches while HG2 stays on. In boost mode, HG2 switches while HG1 stays on. HG1 and HG2 are powered by the BST1 and BST2 pins.

Capacitors between BST1 and SW1, then BST2 and SW2, are required to supply power to HG1 and HG2. These capacitors can be powered by the internal diode connected at VCC, or they can charge one another.

The BST power has its own UVLO control. Its UVLO rising threshold is about 2.7V with a 200mV hysteresis.

Switching Frequency and Frequency Spread Spectrum Function

The MPQ4262 configures the switching frequency (f_{SW}) with a 2-bit FREQ register. The frequency can be 280kHz, 420kHz, or 580kHz. Typically, a 420kHz switching frequency is recommended.

The MPQ4262 has a frequency spread spectrum function. Set the DITHER bit to 1 (0xD0, bit D[7]) to enable this function. Set DITHER to 0 to disable the function. Spread spectrum minimizes the peak emissions at certain frequencies.

The MPQ4262 uses a 4kHz triangle wave to modulate the internal oscillator. The frequency span for the spread spectrum operation is ±7.5% (see Figure 6 on page 22).

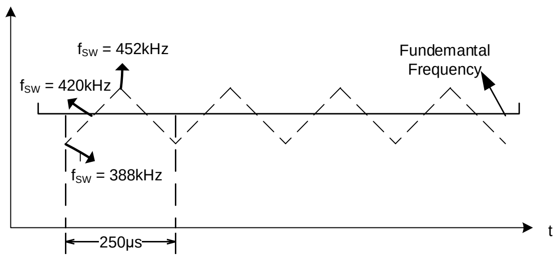


Figure 6: Frequency Spread Spectrum

The MPQ4262 frequency spread frequency can be set to 280kHz, 420kHz or 580kHz.

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then the COMP voltage and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Slew Rate Control and Output Discharge

The MPQ4262 sets the V_{OUT} slew rate via the SR bits (0xD3, bits D[4:3] set the rising slew rate, while bits D[2:1] set the falling slew rate). Four V_{REF} slew rates (rising and falling) can be selected under different application requirements.

During the voltage transient response, the discharge function operates. The discharge function is disabled automatically after V_{REF} finishes changing. A larger-value capacitor means that V_{OUT} may not discharge to the target voltage when V_{REF} finishes changing. Under this scenario, the OVP discharge function can be used to discharge C_{OUT}.

The output discharge function is enabled under the following conditions:

1. The output OVP threshold (120% of V_{FB}) or absolute OVP threshold is triggered.
2. The I²C OPERATION bit is off, or the EN pin is off. Discharge works until the 200ms delay passes.
3. If V_{IN} UVLO is triggered, but VCC has residual voltage, the MPQ4262 discharges for a limited time. This discharge function is disabled after V_{CC} drops below 1.8V.

Output Line Drop Compensation

The MPQ4262 can compensate for an output voltage drop (e.g. high impedance caused by a long trace) to keep a fairly constant load-side voltage.

See the MFR_CTRL2 section on page 29 for the detailed line drop compensation amplitude.

Battery Short to Ground Protection Driver

The MPQ4262 integrates a battery short to ground protection driver, the VGATE pin. When the output ground (USB_GND) shorts to the battery, VGATE pulls low and Q2 turns off (see Figure 7).

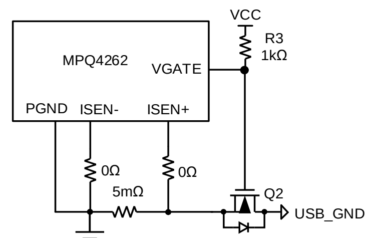


Figure 7: Battery Short to Ground Driver

Table 1 shows the VGATE logic table.

Table 1: VGATE Logic Table

Condition	VGATE Status
VIN < UVLO threshold	Open drain
EN < UVLO threshold	Open drain
Operation = off	Open drain
ISENS > 20A	0

Once V_{IN} and EN are ready (even if OPERATION is set to off), GND short to battery detection forces the device to operate with a low I_Q. The second current limit through the current-sense resistor is about 20A.

System Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold, (about 140°C), the chip is enabled.

PMBus INTERFACE

PMBus Serial Interface Description

The power management bus (PMBus) is an open-standard power management protocol that defines a means of communication with power conversion and other devices.

The PMBus is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. When connecting to the lines, a master device generates an SCL signal and device address, then arranges the communication sequence. This is based on I^2C operation principles.

Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and end of the PMBus transfer. The start command is defined as the SDA signal transitioning from high to low while the SCL is high. The stop command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 8).

The master then generates the SCL clocks and transmits the device address and the read/write direction bit (R/W) on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data is followed by an acknowledge (ACK) bit (see Figure 8).

PMBus Update Sequence

The MPQ4262 requires a start command, a valid PMBus address, a register address byte, and a data byte for a single data update. The device acknowledges the receipt of each byte by pulling the SDA low during the high period of a single clock pulse. A valid PMBus address selects the MPQ4262. The device performs an update on the falling edge of the LSB byte.

PMBus Bus Message Format

Figure 9 on page 24 shows the PMBus message format. In Figure 9, unshaded cells indicate that the bus host is driving the bus actively, and shaded cells indicate that the MPQ4262 is driving the bus.

- S = Start condition
- Sr = Repeated start condition
- P = Stop condition
- R = Read bit
- $\overline{W}$ = Write bit
- A = Acknowledge bit (0)
- $\overline{A}$ = Acknowledge bit (1)

Where “A” represents the acknowledge (ACK) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is received successfully by a device.

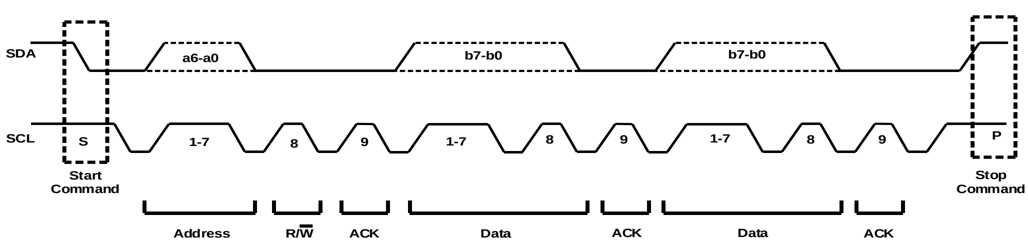


Figure 8: Data Transfer across the PMBus

a) Send Byte

1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	P

b) Write Byte

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	P

c) Write Word

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

d) Read Byte

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	$\overline{A}$	P

e) Read Word

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte Low	A

8	1	1
Data Byte High	$\overline{A}$	P

Figure 9: PMBus Message Format

REGISTER DESCRIPTION

I²C/PMBus Register

The I²C is active once V_{IN} and EN exceed their under-voltage lockout (UVLO) thresholds.

CMD Name	Command Code	Description	Type	Data Format	Unit	OTP	Default
OPERATION	0x01	On/off control	R/W Byte	Reg		Y	On
CLEAR_FAULTS	0x03		Send/ Write Byte	Reg		N	
VOUT_COMMAND	0x21		R/W Word	Linear L16	V	Y	5V
STATUS_WORD	0x79		R Word	Reg		N	
STATUS_ TEMPERATURE	0x7D		R Byte	Reg		N	
MFR_CTRL1	0xD0		R/W Byte	Reg		Y	
MFR_CURRENT_ LIMIT	0xD1	Sets the constant current (CC) limit continuously	R/W Byte	Reg		Y	5.4A
MFR_CTRL2	0xD2	Sets line drop compensation	R/W Byte	Reg		Y	
MFR_CTRL3	0xD3		R/W Byte	Reg		Y	
MFR_CTRL4	0xD4		R/W Byte	Reg		Y	
MFR_STATUS_ MASK	0xD8	Masks the ALT pin indication	R/W Byte	Reg		Y	
MFR_OTP_ CONFIGURATION_ CODE	0xD9	OTP configuration code	R/W Byte	Reg		Y	
MFR_OTP_ REVISION_ NUMBER	0xDA	OTP software revision	R/W Byte	Reg		Y	

The I²C register defaults are based on the MPQ4262-0000.

Data Format

The Linear16 (L16) format is used for the V_{OUT} command (see Figure 10).

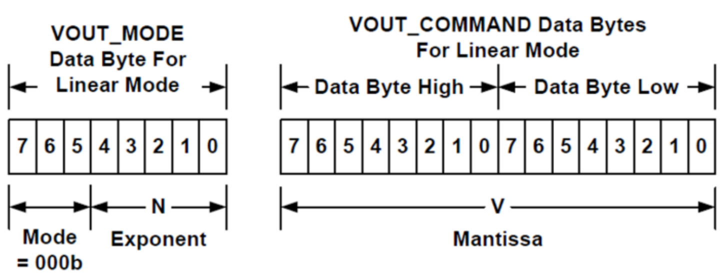


Figure 10: V_{OUT} Command

To read V_{OUT}, follow the description below:

The MODE bits are set to 000b. The voltage (in V) can be calculated with Equation (3):

$$\text{Voltage} = V \times 2^N \quad (3)$$

Where Voltage is the parameter of interest (in V), V is a 16-bit unsigned binary integer, and N is a 5-bit, two's complement, binary integer.

PMBUS COMMANDS

OPERATION

The OPERATION command configures the converter's operational state.

Bit Number	Description	Hex	Meaning
[7:0]	Sets the converter on or off. Note that the EN pin has a higher control priority than this bit.	00h	The output is off.
		01h or 80h	The output is on (default).

CLEAR_FAULTS

The CLEAR_FAULTS command clears any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device clears its ALT signal output if the device is asserting the ALT signal.

If the fault is still present when the bit is cleared, the fault bit is immediately set again, and the host is notified. This command is write-only (see Figure 9 on page 24).

VOUT_COMMAND

The VOUT_COMMAND sets the output voltage. It follows the Linear16 (L16) linear data format.

Command	VOUT_COMMAND															
Format	Linear16															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Data byte high								Data byte low							
Default value (5V)	5120 decimal															

V_{OUT} (in V) can be calculated from the Equation (4):

$$V_{OUT} = V \times 2^{-10} \quad (4)$$

Where V is a 16-bit unsigned binary integer of VOUT_COMMAND, bits[15:0]. The valid V_{OUT} range is between 1V and 21.47V. If V_{OUT} is out of its range, an abnormal V_{OUT} is detected.

The feedback resistor ratio is V_{OUT} / V_{FB} = 10. The VOUT_COMMAND resolution is 10mV.

The internal reference voltage is equal to V_{OUT} / 10. The internal reference voltage ranges between 0.1V and 2.147V with 1mV steps. There is a total of 2047 steps. There is an 11-bit DAC. When the DAC input bit is set to 0, the DAC output is 0.1V.

STATUS_WORD

The STATUS_WORD command returns 2 bytes of information with a summary of the unit's fault conditions. Based on the information in these bytes, the host can obtain more information by reading the appropriate status registers.

Byte	Bits	Status Bit Name	Description
Low	7	RESERVED	Reserved. The default value is 0b.
	6	RESERVED	Reserved. The default value is 0b.
	5	VOUT_OV_FAULT	Indicates if an output over-voltage fault has occurred.
	4	IOUT_OC_FAULT	Indicates if an output over-current fault has occurred. The bit is set if the device reaches the CC current limit or the peak current limit, or if it enters hiccup mode.
	3	GND_SHORT_VBATT	Indicates if a GND short to battery fault has occurred.
	2	TEMPERATURE	Indicates if a temperature fault or warning has occurred.
	1	RESERVED	Reserved. The default value is 0b.
	0	RESERVED	Reserved. The default value is 0b.
High	7	VOUT	Indicates if an output voltage fault or warning has occurred.
	6	IOUT/POUT	Indicates if an output current fault has occurred. The bit is set if the device reaches the CC current limit or the peak current limit, or if it enters hiccup mode.
	5	RESERVED	Reserved. The default value is 0b.
	4	OC_EXIT	Indicates if the output current exits the CC current limit. This bit is only set high when I_{OUT} changes from CC mode (before enter hiccup) to a different mode. The bit is not set after the device recovers from hiccup mode.
	3	PG_STATUS#	The POWER_GOOD signal, if present, is negated. 1: The output voltage is not good 0: The output voltage is power good
	2	RESERVED	Reserved. The default value is 0b.
	1	RESERVED	Reserved. The default value is 0b.
	0	RESERVED	Reserved. The default value is 0b.

The PG_STATUS# bit is an exception, as it always reflects the current state of the POWER_GOOD signal.

STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns 1 data byte with information on temperature faults.

Bits	Bit Name	Description
7	OT_FAULT	Indicates if an over-temperature (OT) fault occurs. The OTP entry threshold 160°C.
6	OT_WARNING	Indicates if an over-temperature (OT) warning occurs. The entry threshold is 135°C, with a 20°C hysteresis.
5	RESERVED	Reserved.
4	RESERVED	Reserved.
3	OT_WARNING_EXIT	An over-temperature (OT) warning falling edge sets this bit high
2	RESERVED	Reserved.
1	RESERVED	Reserved.

I²C REGISTER MAP

Name	REG (0x)	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MFR_CTRL1	D0	R/W	DITHER_ENABLE	FREQ		SWA_FET_RON		OUTPUT_OVP_EN	OUTPUT_DISCHARGE_EN	PFM/PWM_MODE
MFR_CURRENT_LIMIT	D1	R/W	LDC_DISABLE	Constant current limit (1A to 5.4A/50mA step)						
MFR_CTRL2	D2	R/W							LINE_DROP_COMPENSATION	
MFR_CTRL3	D3	R/W	SWITCHING_CURRENT_LIMIT		RSENS	SLEW_RATE_RISE		SLEW_RATE_FALL		FREQ_MODE
MFR_CTRL4	D4	R/W		CC_BLANK_TIMER	SW2_EDGE	I²C Address (A5~A1)				
MFR_STATUS_MASK	D8	R/W	Masks the ALT pin indication if a fault or event occurs							
MFR_OTP_CONFIGURATION_CODE	D9	R/W	OTP configuration code, defined by MPS							
MFR_OTP_REVISION_NUMBER	DA	R/W	OTP software revision number, defined by MPS							

I²C Slave Address

The I²C slave address is set to 67h by default.

I²C Address A7~A1	
Binary	**Hex**
1100 111 (default)	**67h**
I²C/OTP-adjustable for A5~A1	Set by MFR_CTRL4_D[4:0]

MFR_CTRL1

Address: 0xD0
Reset value: Set by OTP
Type: Read and Write

Bit	Bit Name	Description
D[7]	DITHER_ENABLE	0: No dither 1: Enables the frequency spread spectrum function (default)
D[6:5]	FREQ	Sets the MPQ4262 switching frequency. The default value is 01. 00: 280kHz 01: 420kHz 10: 580kHz 11: Reserved
D[4:3]	SWA_FET_RON	Sets SWA's on resistance under $5V_{GS}$ conditions. This value will affects the zero-current detection (ZCD) and negative current limit in boost mode. It should match the real MOSFET value. The default value is 01. 00: 5mΩ 01: 10mΩ 10: 15mΩ 11: 20mΩ
D[2]	OUTPUT_OVP_EN	Enables output over-voltage protection (OVP). The default value is 1. 1: Enabled 0: Disabled

D[1]	OUTPUT_ DISCHARGE_ EN	Enables the output discharge function. The default value is 1. There is a passive discharge resistor from the VOUT pin to ground. This discharge function works until the 200ms timer runs out. 1: The MPQ4262 turns on the output discharge function during the EN, V_{IN}, or I²C off period until V_{OUT} is fully discharged 0: Disable the output discharge function during the EN, V_{IN}, or I²C off period
D[0]	PFM/PWM_MODE	Sets the buck-boost mode to auto-PFM/PWM mode, or forced PWM mode. The default value is 1. 0: Auto-PFM/PWM mode 1: Forced PWM mode

MFR_CURRENT_LIMIT

Address: 0xD1
Reset value: Set by MTP
Type: Read and Write

Sets the output constant current (CC) limit threshold

Name	LDC_DISABLE	CONSTANT_CURRENT_LIMIT						
Format	Direct, unsigned binary integer							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default value (5.4A)	0	108 integer						

The real-world I_{OUT} over-current threshold (in A) can be calculated with Equation (5):

$$IOUT\_OC\ (A) = IOUT\_LIM \times 0.05 \tag{5}$$

Where IOUT_LIM is a 7-bit, unsigned binary integer of IOUT_LIM, bits D[6:0].

The IOUT_OC resolution (or minimum step) is 50mA. The maximum value is 5.4A. Beyond this range, the current limit is clamped at 5.4A.

D[7] is the bit that enables line drop compensation. When D[7] is set to 0, line drop compensation is controlled by register 0xD2. When D[1] is set to 1, line drop compensation is disabled.

MFR_CTRL2

Address: 0xD2
Reset value: Set by OTP
Type: Read and Write

Bits	Bit Name	Description
D[7:2]	RESERVED	Reserved.
D[1:0]	LINE_DROP_ COMPENSATION	Sets the output voltage compensation value vs. the load current. The compensation amplitude is fixed for any output voltage. Line drop compensation is only enabled for applications where the output voltage exceeds 5V. This value is clamped when I_{OUT} > 3.6A. The default value is 00. 00: No compensation 01: V_{OUT} compensates 100mV at a 3A I_{OUT} 10: V_{OUT} compensates 300mV at a 3A I_{OUT} 11: V_{OUT} compensates 600mV at a 3A I_{OUT}

MFR_CTRL3

Address: 0xD3
Reset value: Set by OTP
Type: Read and Write

Bits	Bit Name	Description
D[7:6]	SWITCHING_ CURRENT_LIMIT	Set the current limit for switch B (SWB) and switch C (SWC). The default value is 10. D[7:6] / SWC Peak Current Limit / SWB Valley Current Limit: 00 / 8A / 6A 01 / 12A / 9A 10 / 15A / 13A 11 / 20A / 17A
D[5]	RSENS	Select the R_{SENS} resistor value. The default value is 0. 0: 5mΩ 1: 10mΩ
D[4:3]	SLEW_RATE_ RISE	Sets the V_{OUT} rising slew rate. The default value is 01. The slew rate can be calculated with the following equation: V_{OUT} Slew Rate = V_{REF} Slew Rate x Feedback Ratio Where Feedback Ratio = 10. 00: 0.08mV/µs; V_{REF} rising slew rate 01: 0.16mV/µs; V_{REF} rising slew rate 10: 0.4mV/µs; V_{REF} rising slew rate 11: 0.8mV/µs; V_{REF} rising slew rate
D[2:1]	SLEW_RATE_ FALL	Sets the V_{OUT} falling slew rate. The default value is 01. The slew rate can be calculated with the following equation: V_{OUT} Slew Rate = V_{REF} Slew Rate x Feedback Ratio Where Feedback Ratio = 10. 00: 0.02mv/µs; V_{REF} falling slew rate 01: 0.04mv/µs; V_{REF} falling slew rate 10: 0.1mv/µs; V_{REF} falling slew rate 11: 0.2mv/µs; V_{REF} falling slew rate
D[0]	FREQ_MODE	Sets the frequency in buck-boost mode. The default value is 1. 0: Reduce the frequency by half in buck-boost mode 1: Maintain the same frequency in buck-boost mode

MFR_CTRL4

Address: 0xD4
Reset value: Set by OTP
Type: Read and Write

Bits	Bit Name	Description
D[7]	RESERVED	Reserved.
D[6]	CC_BLANK_ TIMER	Sets the blanking time before the device enters CC mode. The default value is 1. 0: 5ms 1: 400µs
D[5]	SW2_EDGE	Selects the SW2 rising and falling speed. The default value is 1. 0: Normal 1: Faster than normal

D[4:0]	I2C_ADDRESS	Sets the I²C slave address A5~A1 bit. The default value is 00111b (67h).

MFR_STATUS_MASK

Address: 0xD8
Reset value: Set by OTP
Type: Read and Write

This register only can mask the ALT pin's behavior, which means that the STATUS register still indicates each event.

Bits	Bit Name	Description
7	VOUT_MSK	0: Not masked 1: Masked (default)
6	IOUT/POUT_MSK	This bit masks IOUT_OC_FAULT, IOUT/POUT and OC_EXIT. The default value is 0. 0: Not masked 1: Masked
5	RESERVED_MSK	0: Not masked 1: Masked (default)
4	TEMP_MSK	Masks temperature-related events. The default value is 1. 0: Not masked 1: Masked
3	PG_STATUS#_ MSK	Masks the higher level PG off control. The default value is 1. 0: Not masked 1: Masked
2	PG_ALT_ EDGE_MSK	0: Not masked. The ALT pin indicates both PG_STATUS# rising and falling edges 1: Mask enabled (default). The ALT pin only indicates the PG_STATUS# falling edge, which is when the output voltage transitions from a not good voltage to a good voltage
1	GND_SHORT_ VBATT_MSK	0: Not masked 1: Masked (default)
0	UNKNOWN_MSK	0: Not masked 1: Masked (default)

MFR_OTP_CONFIGURATION_CODE

Address: 0xD9
Reset value: Set by OTP
Type: Read and Write

Bits	Bit Name	Description
D[7:0]	OTP_ CONFIGURATION_ CODE	Returns the OTP configuration code, defined by MPS.

MFR_OTP_REVISION_NUMBER

Address: 0xDA
Reset value: Set by OTP
Type: Read and Write

Bits	Bit Name	Description
D[7:0]	OTP_ REVISION_ NUMBER	Returns the OTP software revision number, defined by MPS.

MPQ4262GQVE-0000 CONFIGURATION TABLE

OTP Items	Description	Value
OPERATION	Sets the device on or off	1: On
VOUT_COMMAND	Sets the output voltage	5V
DITHER_ENABLE	Enables frequency spread spectrum	1: Enabled
FREQ	Sets the switching frequency	01: 420kHz
SWA_FET_RON	Sets SWA's on resistance	01: 10mΩ
OUTPUT_OVP_EN	Enables output OVP	1: Enabled
OUTPUT_DISCHARGE_EN	Enables the output discharge function during the V_{IN}, I²C, or EN off period	1:Enabled
PFM/PWM_MODE	Selects auto-PFM/PWM mode or forced PWM mode	1: Forced PWM mode
CONSTANT_ CURRENT_LIMIT	Sets the output current limit	5.4A
LINE_DROP_ COMPENSATION	Sets the output voltage compensation value vs. load current	00: No compensation
SWITCHING_ CURRENT_LIMIT	Sets the SWB valley current limit and SWC peak current limit	10: SWC peak: 15A; SWB valley: 13A
RSENS	Selects the R_{SENS} resistor value	0:5mΩ
SLEW_RATE_RISE	Sets the V_{OUT} rising slew rate	01: 0.16mV/µs
SLEW_RATE_FALL	Sets the V_{OUT} falling slew rate	01: 0.04mV/µs
FREQ_MODE	Sets the frequency for buck-boost mode	1: Maintain the same frequency in buck-boost mode
CC_BLANK_TIMER	Sets the blanking time before entering CC mode	1: 400µs
SW2_EDGE	Selects the SW2 rising and falling speed	1: Faster than normal
ABSOLUTE OUTPUT OVP	Selects the absolute OVP threshold	0: 26V
OT WARNING FUNCTION	Enables the OT warning function	0: Enabled
I2C_ADDRESS	Sets the I²C slave address	67h
VOUT_MSK	Masks ALT pin indication	1: Masked
IOUT/POUT_MSK		0: Not masked
RESERVED_MSK		1: Masked
TEMP_MSK		1: Masked
PG_STATUS#_MSK		1: Masked
PG_ALT_EDGE MSK		1: Masked
GND_SHORT_ VBATT_MSK		1: Masked
UNKNOWN_MSK		1: Masked

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Inductor

Inductor selection is based on the operating mode. The inductance for buck mode can be estimated with Equation (6):

$$L_{BUCK} = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Where ΔI_L is the peak-to-peak inductor ripple current, which is 30% to 50% of the maximum load current.

For boost mode, inductor selection is based on limiting the peak-to-peak current ripple (ΔI_L) to be about 30% to 50% of the maximum input current. The target inductance for boost mode can be calculated with Equation (7):

$$L_{BOOST} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (7)$$

Where ΔI_L is the peak-to-peak ripple current. $I_{IN(MAX)}$ can be estimated with Equation (8):

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{LOAD(MAX)}}{V_{IN} \times \eta} \quad (8)$$

Where $I_{LOAD(MAX)}$ is the maximum load current, and η is the efficiency.

Choosing a larger-value inductor reduces the ripple current but increases the physical size of the inductor. A larger-value inductor also reduces the achievable bandwidth of the converter by moving the right half-plane zero to lower frequencies. Select the inductor for the specific application requirements.

Selecting the Input Capacitor

In buck mode, the input current is discontinuous, while it is continuous in boost mode. A capacitor must supply the AC current in buck mode while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance, and these capacitors should be placed as close to the VIN pin as possible. Ceramic capacitors with X5R or X7R dielectrics are recommended because they are fairly stable across temperature fluctuations. The capacitors must also have a ripple current rating greater than the converter's maximum input ripple current. The input ripple current in buck mode can be estimated with Equation (9):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (9)$$

The worst-case condition in buck mode occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (10):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (10)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple in buck mode can be estimated with Equation (11):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

The worst-case condition occurs where V_{IN} = 2 x V_{OUT}, calculated with Equation (12):

$$\Delta V_{IN} = \frac{1}{4} \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (12)$$

Selecting the Output Capacitor

In boost mode, the output current (I_{OUT}) is discontinuous, so an output capacitor (C_{OUT}) must be able to reduce the output voltage ripple.

A larger-value capacitor may be required to lower the output voltage ripple and transient response. Ceramic, low-ESR capacitors with X5R or X7R dielectrics are recommended. If using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, so the output voltage ripple is independent of the ESR. The output voltage ripple can be estimated with Equation (13):

$$\Delta V_{OUT} = \frac{(1-\frac{V_{IN}}{V_{OUT}}) \times I_{LOAD}}{C_{OUT} \times f_{SW}} \quad (13)$$

Where V_{RIPPLE} is the output ripple voltage, and C_{OUT} is the capacitance of the output capacitor.

If using polymer, hybrid, or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The output voltage ripple can be estimated with Equation (14):

$$\Delta V_{OUT} = \frac{(1-\frac{V_{IN}}{V_{OUT}}) \times I_{LOAD}}{C_{OUT} \times f_{SW}} + \frac{I_{LOAD} \times R_{ESR} \times V_{OUT}}{V_{IN}} \quad (14)$$

Where R_{ESR} is the equivalent series resistance of the output capacitors.

Choose output capacitors that satisfy the design's output voltage ripple and load transient response requirements. Consider capacitance derating when designing applications with high output voltages.

Selecting the External MOSFETs (SWA and SWD)

The MPQ4262 requires two external N-channel power MOSFETs (see Figure 11). In buck mode, SWA and SWB switch while SWD stays on. In boost mode, SWC and SWD switch while SWA stays on.

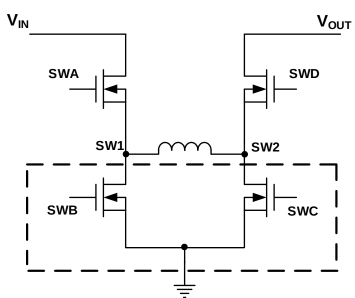


Figure 11: Buck-Boost Topology

The critical parameters to select a MOSFET are described below.

1. Maximum drain-to-source voltage ($V_{DS(MAX)}$): SWA must withstand the maximum input voltage and the transient spikes at SW1 during switching. Select SWA and SWB to have a $V_{DS(MAX)}$ that is 1.5 times the input voltage.

   SWD withstands the output voltage and additional transient spikes at SW2 during switching. Select SWD to have a $V_{DS(MAX)}$ that is at least 1.5 times the output voltage.
2. Maximum current ($I_{D(MAX)}$)
3. V_{TH}: The driver voltages of the MPQ4262 are supplied by VCC. The gate plateau voltages should be below the converter's minimum V_{CC}. Otherwise, the MOSFETs may not fully turn on during start-up or under overload conditions.
4. On resistance ($R_{DS(ON)}$)
5. Total gate charge (Q_G): For the MPQ4262, the Q_G value for all switches should be below 30nC (at a 5V GATE condition). The SW1 rising time and SW2 falling time are shorter than 15ns.

SWA

When the MPQ4262 works in boost mode, SWA is always on. SWA's conduction power loss can be calculated with Equation (15):

$$P_{C\_LOSS(SWA)} = (I_{OUT} \times \frac{V_{OUT}}{V_{IN}})^2 \times R_{DSON(SWA)} \quad (15)$$

Assume that the MOSFET's thermal resistance from the junction to ambient is 50°C/W (determined by the board's power dissipation), and that the maximum acceptable temperature rise is 50°C. The maximum power loss can be estimated with Equation (16):

$$P_{C\_LOSS(SWA)} < 1W \quad (16)$$

Use the above calculations to select a MOSFET with an appropriate on resistance.

When the MPQ4262 works in buck mode, the conduction and switching loss of SWA can be calculated with Equation (17) and Equation (18), respectively:

$$P_{C\_LOSS(SWA)} = \frac{V_{OUT}}{V_{IN}} \times I_{OUT}^{\ 2} \times R_{DSON(SWA)} \quad (17)$$

$$P_{SW\_LOSS(SWA)} = \frac{1}{2} V_{IN} \times I_{OUT} \times (t_{ON} + t_{OFF}) \times f_{sw} \quad (18)$$

Figure 12 on page 34 shows the switch on/off state. The switch on time (t_{ON}) and the switch off time (t_{OFF}) are based on the MOSFET datasheet.

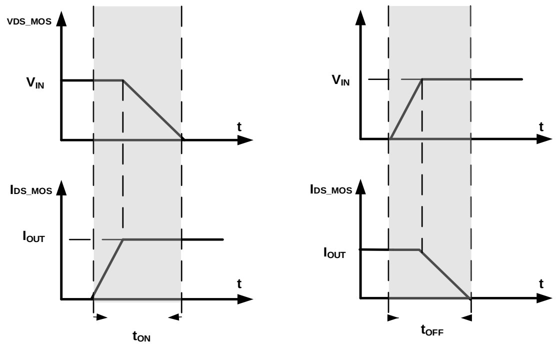


Figure 12: Switch On/Off State

SWD

When the MPQ4262 works in buck mode, SWD is always on. The SWD power loss can be calculated with Equation (19):

$$P_{C\_LOSS(SWD)} = I_{OUT}^2 \times R_{DSON(SWD)} \quad (19)$$

$P_{C\_LOSS(SWD)}$ should be less than the maximum power loss. When the MPQ4262 works in boost mode, the conduction loss can be estimated with Equation (20):

$$P_{C\_LOSS(SWD)} = \frac{V_{OUT}}{V_{IN}} \times I_{OUT}^2 \times R_{DSON(SWD)} \quad (20)$$

When determining the total power loss, the dead time and low-side MOSFET switching loss can be ignored.

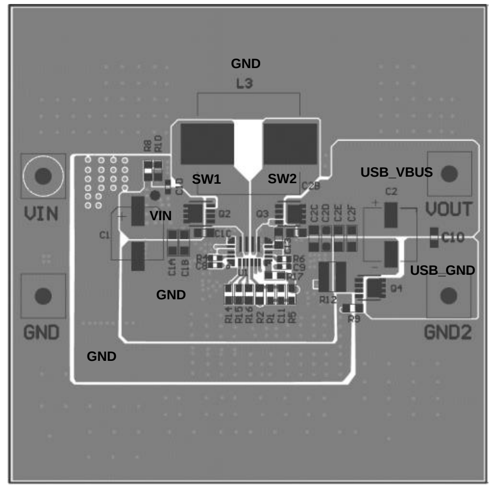
PCB Layout Guidelines (8)

Efficient PCB layout is critical for standard operation and thermal dissipation. For the best results, refer to Figure 13 and follow the guidelines below:

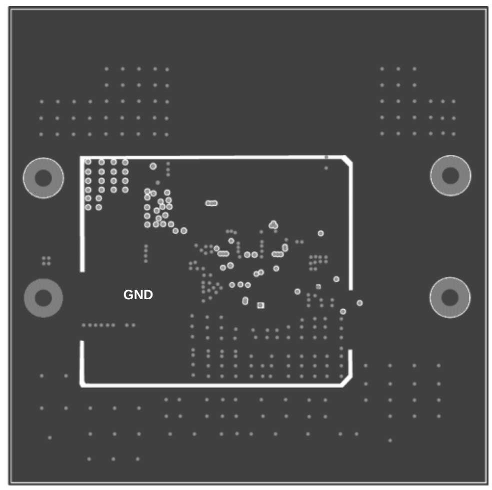
1. In buck mode, place the input power loop — including the input filter capacitor (C_{IN}), the power MOSFET (SWA), and SW1 node — as close together as possible.
2. In boost mode, place the output power loop —including the output filter capacitor (C_{OUT}), the power MOSFET (SWD), and SW2 node — as close together as possible.
3. Use short, direct, and wide traces to connect VOUT.
4. Add vias to GND after the output filter if required.
5. Use a large copper plane for PGND, and add multiple vias to improve thermal dissipation.
6. Connect AGND to PGND.
7. To improve EMI performance, place two ceramic input decoupling capacitors as close as possible to the SWA and SWD drains, and PGND.
8. Place the input filter at the bottom layer to improve EMI performance.
9. Place the VCC decoupling capacitor as close as possible to VCC.
10. The output current-sense traces (ISEN+ and ISEN-) must have a Kelvin connection.
11. The switching nodes of the BST1/2 capacitors must be Kelvin connected to the SW1 and SW2 pins with a wide PCB trace.
12. Kelvin connect the VIN pin to the SWA drain with a wide PCB trace.

Note:

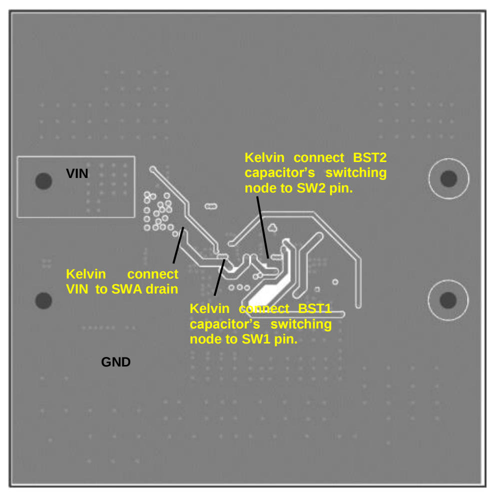
8) The recommended layout is based on the typical application circuit (see Figure 14 on page 38).



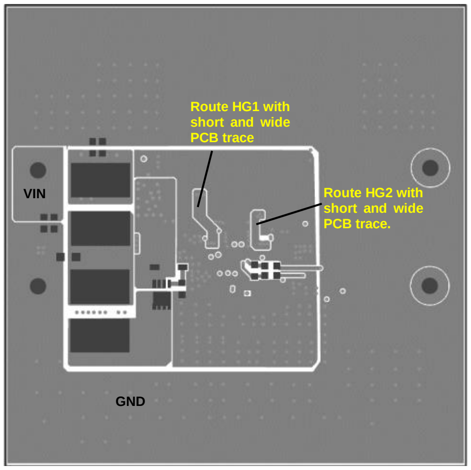
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 13: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

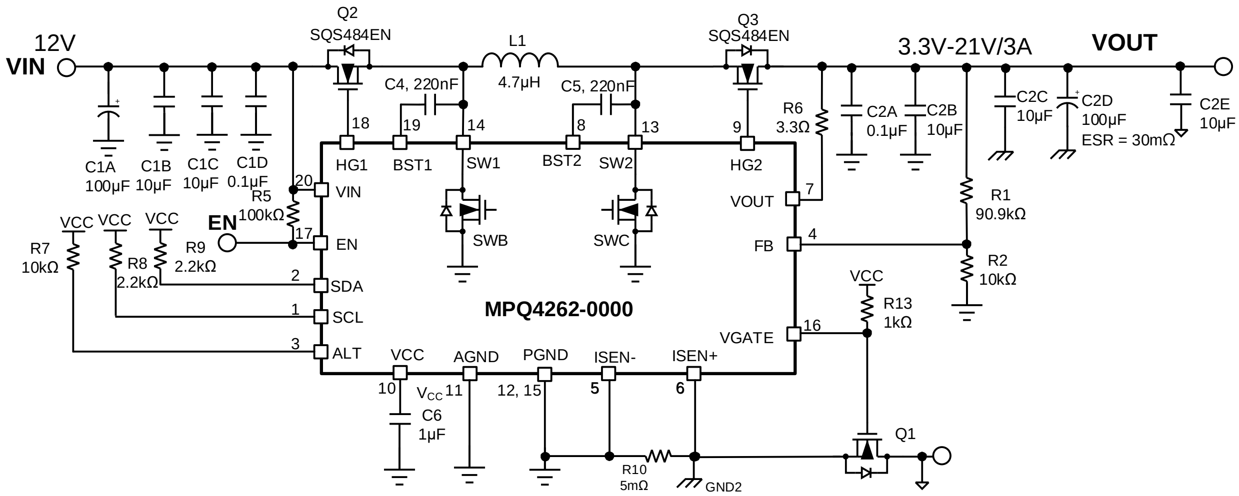


Figure 14: V_{IN} = 12V, V_{OUT} = 3.3V to 21V/3A (OPERATION Set to On) (9)

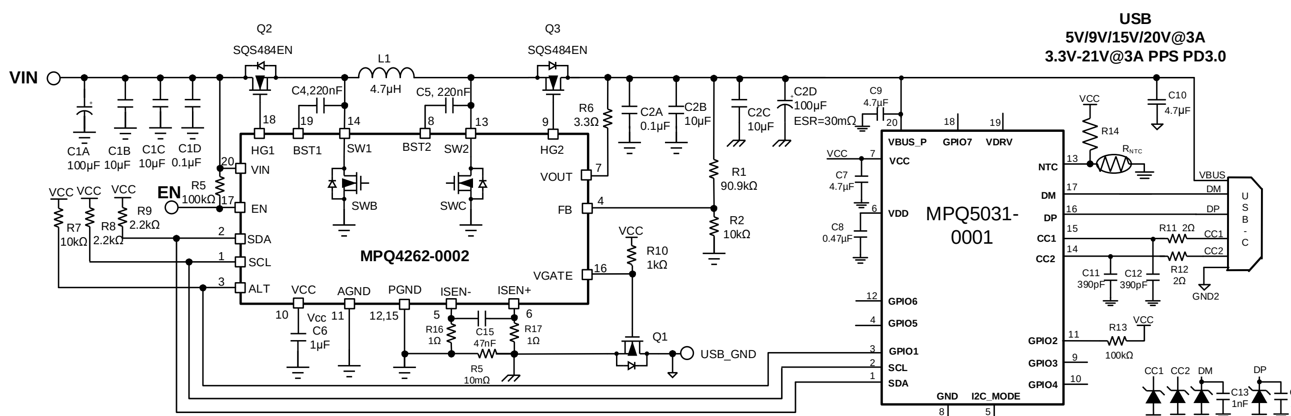


Figure 15: The MPQ4262 and MPQ5031 for a 60W PD Application (10)

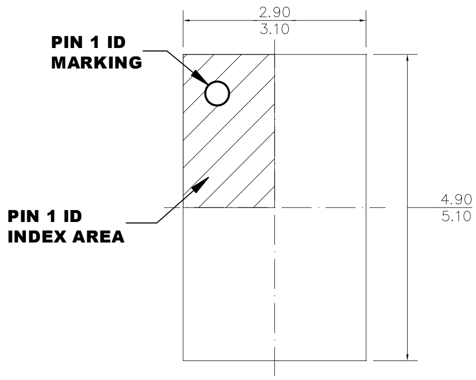
Notes:

9) The 5mΩ current-sense resistor can be removed. ISEN- and ISEN+ can be directly connected to GND without the output average current limit because the switching current limit still works.

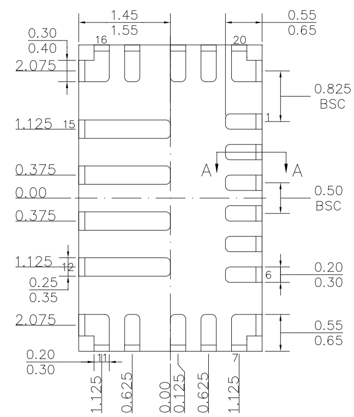
10) A 10mΩ current-sense resistor and RC filter are required to pass USB-IF PPS certification. The evaluation boards for the MPQ4262 and MPQ5031 can be use in PD reference designs.

PACKAGE INFORMATION

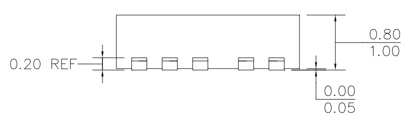
QFN-20 (3mmx5mm)



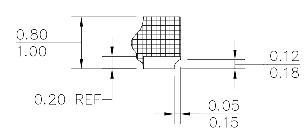
TOP VIEW



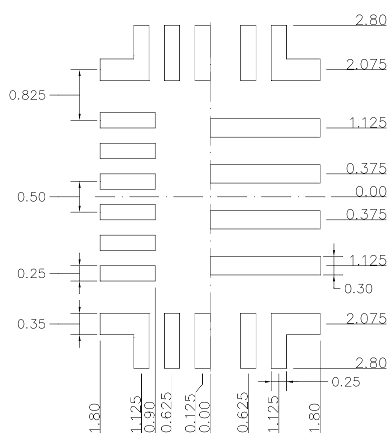
BOTTOM VIEW



SIDE VIEW



SECTION A-A

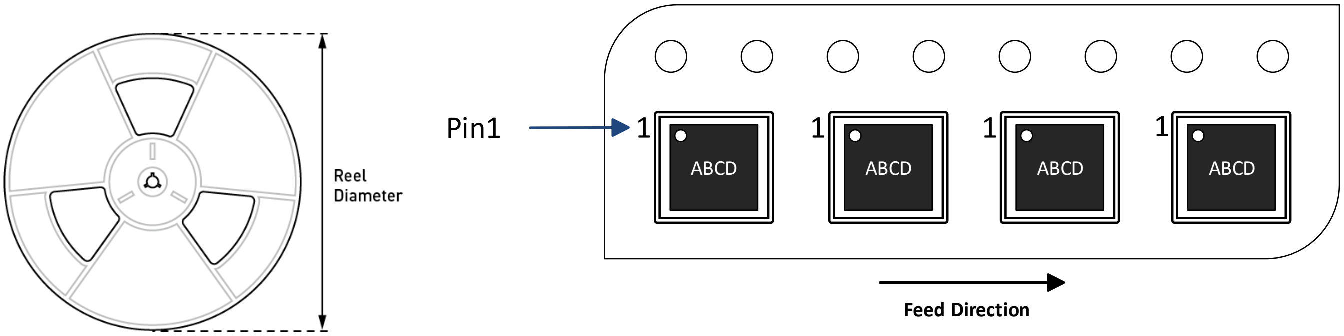


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4262GQVE-0000-AEC1-Z	QFN-20 (3mmx5mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4262GQVE-0001-AEC1-Z							
MPQ4262GQVE-0002-AEC1-Z							
MPQ4262GQVE-xxxx-AEC1-Z							

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/11/2021	Initial Release	-