Features

- Super Low Gate Charge
- Green Device Available
- Excellent Cdv/dt effect decline
- Advanced high cell density Trench technology
- 100% EAS Guaranteed

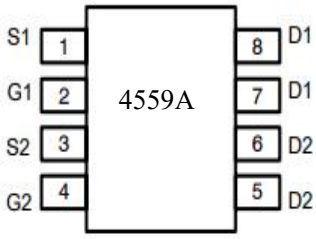
Bvdss	Rdson	ID
60V	30mΩ	6A
-60V	70mΩ	-5A

Application

- Power management in half bridge and in
- Load Switch
- DC-DC Converter

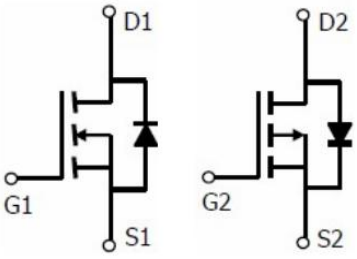
RoHS

Package



Marking and pin assignment

SOP-8 top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
4559A	4559A	SOP-8	5000

Absolute Maximum Ratings

Parameter	Symbol	Value		Unit
		N-Channel	P-Channel	
Drain-Source Voltage	V_{DS}	60	-60	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Continuous Drain Current	I_D@T_A =25℃, V_{GS}@10V[1]	6	-5	A
	I_D@T_A =70℃, V_{GS}@10V[1]	4	-3.5	A
Pulsed Drain Current[2]	I_{DM}	11	-8.5	A
Single Pulsed Avalanche Energy[3]	E_{As}	22.5	35.3	mJ
Avalanche Current	I_{AS}	22.6	-26.6	A
Total Power Dissipation[4]	P_D@T_A =25℃	2.5	2.5	W
Junction Temperature Range	T_J	-55~+150		℃
Storage Temperature Range	T_{STG}	-55~+150		℃

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Case[1]	$R_{\theta JC}$	62.5	℃/W
Thermal Resistance Junction-Ambient[1]	$R_{\theta JA}$	85	℃/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL4559A	SOP-8	2,4	5,6,7,8	1,3	Tape Reel

N-Channel Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V , I_D=-250uA	60	-	-	V
Static Drain-Source On-Resistance[3]	$R_{DS(ON)}$	V_{GS}=10V , I_D=5A	-	30	40	mΩ
		V_{GS}=-4.5V , I_D=3A	-	36	50	
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS} , I_D =250uA	1.0	1.6	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V ,V_{GS}=0V	-	-	1	uA
Gate to Body Leakage Current	I_{GSS}	V_{GS}=±20V , V_{DS}=0V	-	-	±100	nA
Forward Transconductance[4]	gfs	V_{DS}=5V , I_D=10A	-	15.5	-	S
Total Gate Charge	Q_g	V_{GS}=10V ,V_{DS}=30V , I_D=2.5A	-	20.3	-	nC
Gate-Source Charge	Q_{gs}		-	3.7	-	
Gate-Drain Charge	Q_{gd}		-	5.3	-	
Turn-On Delay Time	$T_{d(on)}$	V_{GS}=10V ,V_{DS}=30V , R_G=1.8Ω , I_D=5A	-	7.6	-	ns
Rise Time	T_r		-	20	-	
Turn-Off Delay Time	$T_{d(off)}$		-	15	-	
Fall Time	T_f		-	24	-	
Input Capacitance	C_{iss}	V_{DS}=25V , V_{GS}=0V , f=1MHz	-	1148	-	pF
Output Capacitance	C_{oss}		-	58.5	-	
Reverse Transfer Capacitance	C_{rss}		-	49.4	-	
Body Diode Reverse Recovery Time	t_{rr}	I_F=-5A, dI_F/dt=100A/μs	-	29	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	43	-	nC
Diode Forward Voltage	V_{SD}	I_S=5A,V_{GS}=0V	-	-	1.2	V
Continuous Source Current	I_S	-	-	-	6	A
Pulsed Drain to Source Diode Current	I_{SM}	-	-	-	20	A

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition : T_J=25℃,V_{DD}=30V,V_G=10V,L=0.5mH,Rg=25Ω,I_{AS}=8.7A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

P-Channel Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V , I_D=-250uA	-60	-	-	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-48V ,V_{GS}=0V, T_J=25℃	-	-	1	uA
		V_{DS}=-48V ,V_{GS}=0V, T_J=55℃	-	-	5	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V , V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS} , I_D =250uA	-1.0	-	-2.5	V
Drain-Source On-State Resistance[4]	$R_{DS(ON)}$	V_{GS}=-10V , I_D=-3.5A	-	70	100	mΩ
		V_{GS}=-4.5V , I_D=-3.1A	-	100	115	
Forward Transconductance	gfs	V_{DS}=-5V , I_D=-3A	-	8.5	-	S
Input Capacitance	C_{iss}	V_{DS} = -15V, V_{GS} =0V, f =1MHz	-	1137	-	pF
Output Capacitance	C_{oss}		-	76	-	
Reverse Transfer Capacitance	C_{rss}		-	50	-	
Total Gate Charge（-4.5V）	Q_g	V_{DS} =-48V, V_{GS} =-4.5V, I_D= -3A	-	12.1	-	nC
Gate-Source Charge	Q_{gs}		-	2.2	-	
Gate-Drain Charge	Q_{gd}		-	6.3	-	
Turn-On Delay Time	$T_{d(on)}$	V_{DD} =-15V, V_{GS} = -10V, R_G = 3.3Ω, I_D= -1A	-	9.2	-	ns
Rise Time	T_r		-	20.1	-	
Turn-Off Delay Time	$T_{d(off)}$		-	46.7	-	
Fall Time	T_f		-	9.4	-	
Diode Forward Voltage[2]	V_{SD}	I_S = -1A, V_{GS} = 0V, T_J=25℃	-	-	-1.2	V
Continuous Source Current[1,5]	I_S	V_G=V_D=0V,Force Current	-	-	-6	A

Notes:

1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The EAS data shows Max. rating . The test condition is V_{DD}=-25V,V_{GS}=-10V,L=0.1mH,I_{AS}=-24A

4.The power dissipation is limited by 150℃ junction temperature

5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

Fig.1 Typical Output Characteristics

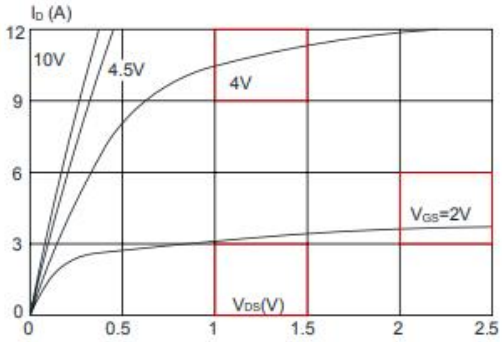


Fig.2 Typical Transfer Characteristics

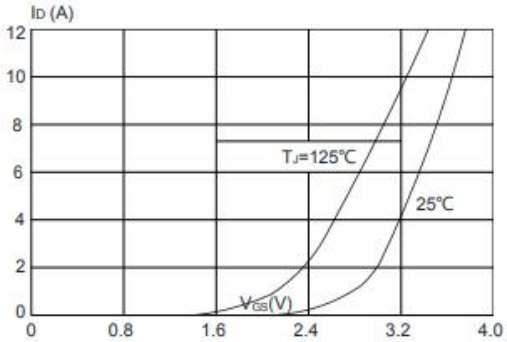


Fig.3 On-resistance vs. Drain Current

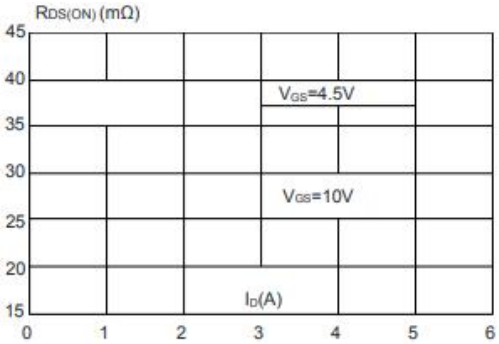


Fig.4 Body Diode Characteristics

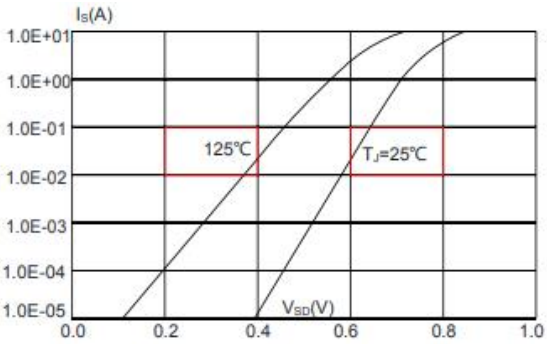


Fig.5 Gate Charge Characteristics

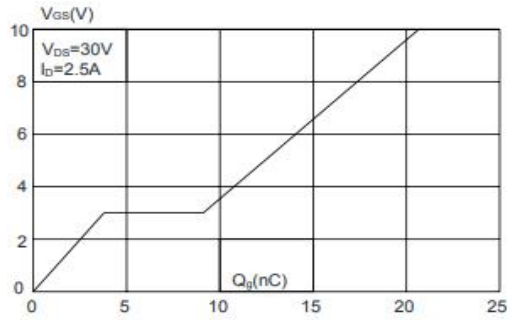


Fig.6 Capacitance Characteristics

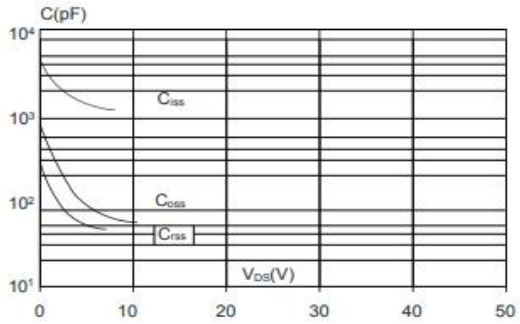


Fig.7 Normalized Breakdown Voltage vs. Junction Temperature

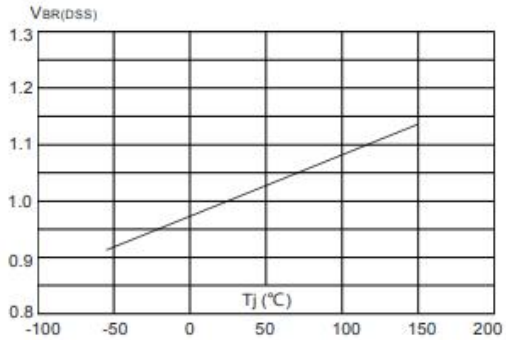


Fig.8 Normalized on Resistance vs. Junction Temperature

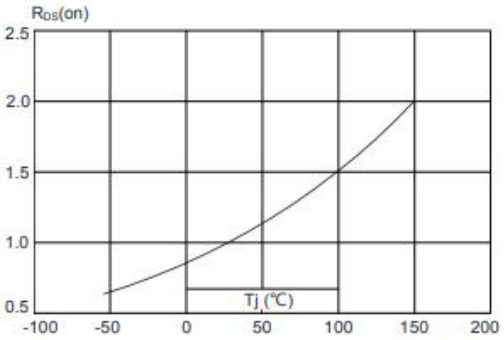


Fig.9 Maximum Safe Operating Area

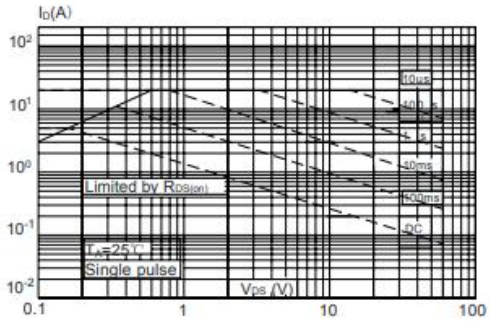


Fig.10 Maximum Continuous Drain Current vs. Ambient Temperature

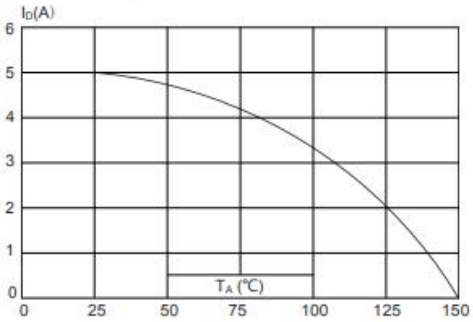
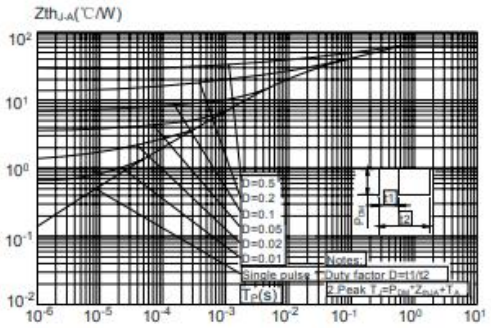


Fig.11 Normalized Maximum Transient Thermal Impedance



P-Channel Typical Characteristics

Fig.1 Typ. output characteristics

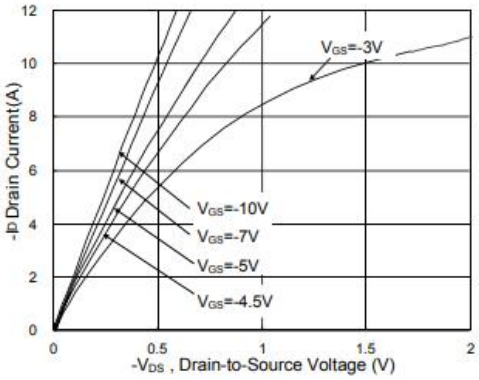


Fig.2 On-Resistance vs. G-S Voltage

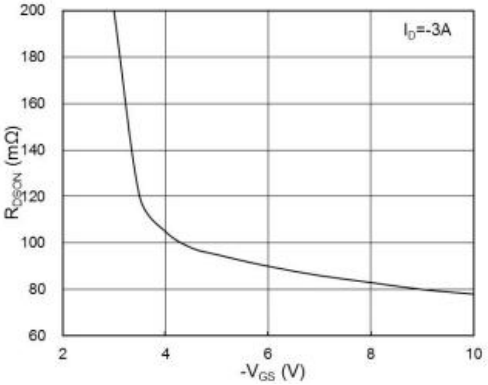


Fig.3 Source Drain Forward Characteristics

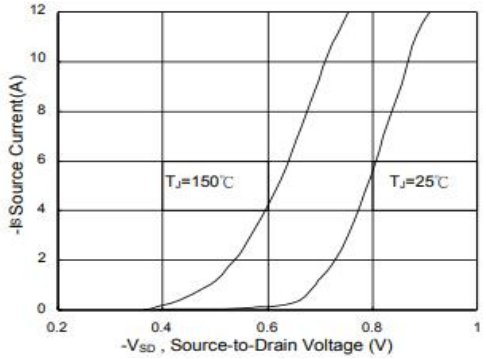


Fig.4 Gate-Charge Characteristics

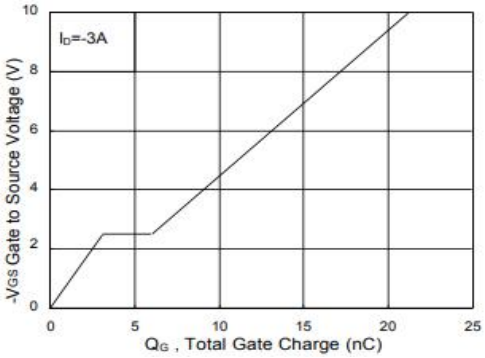


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

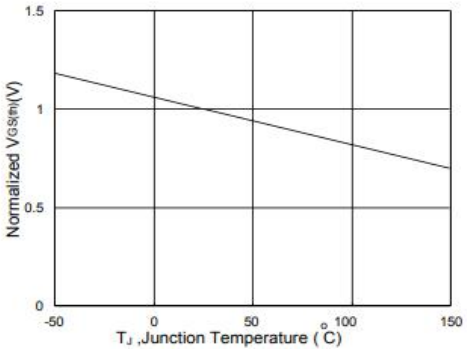


Fig.6 Normalized R_{DSON} vs. T_J

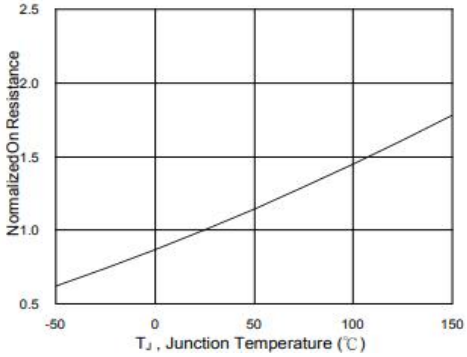


Fig.7 Capacitance

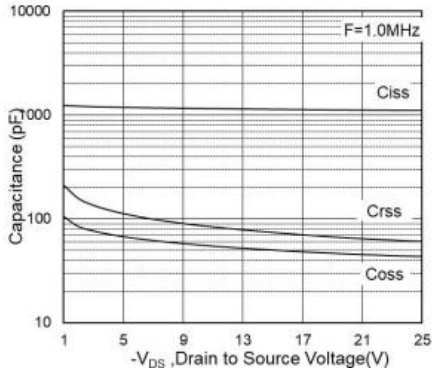


Fig.8 Safe Operating Area

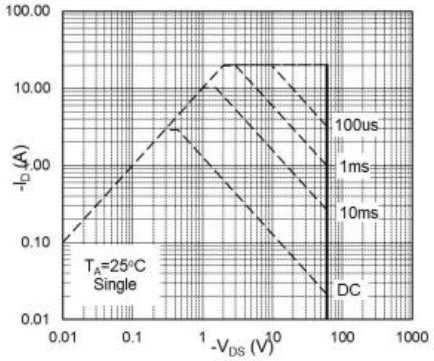


Fig.9 Normalized Maximum Transient Thermal Impedance

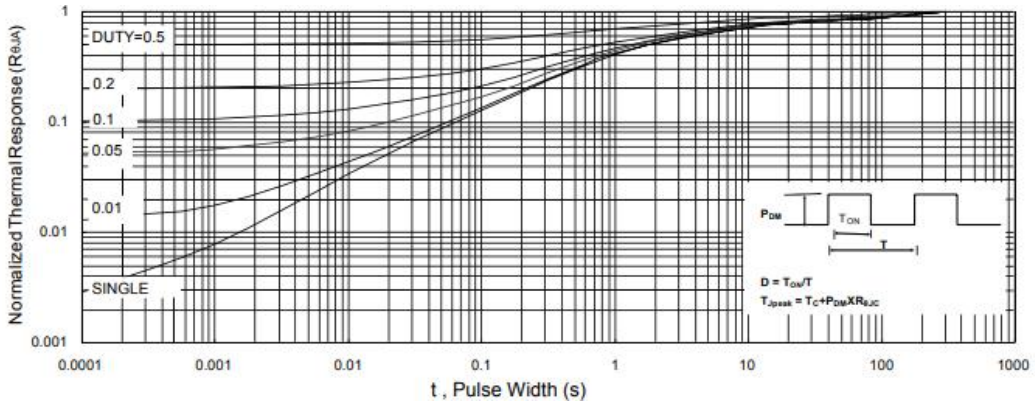


Fig.10 Switching Time Waveform

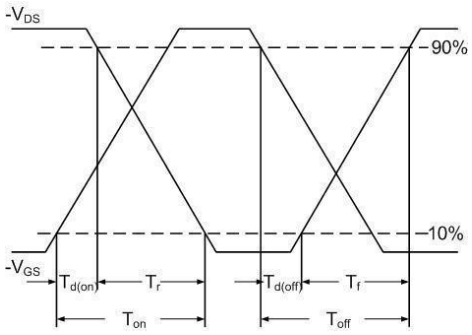
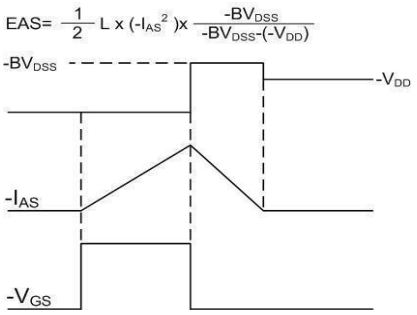
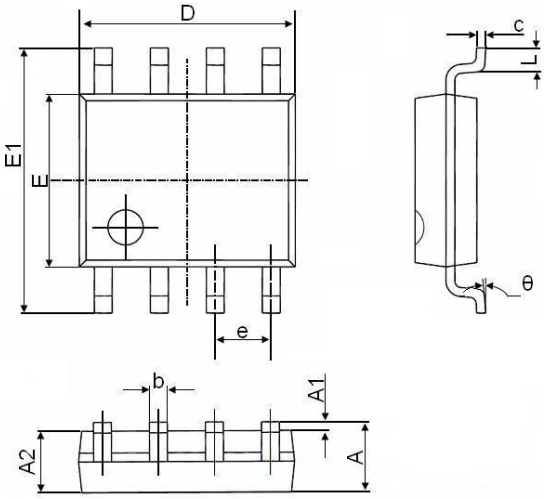


Fig.11 Unclamped Inductive Waveform



Package Dimensions SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important Notice and Disclaimer

HL Microelectronics reserves the right to make changes to this document and its products and specifications at any time without notice.
Customers should obtain and confirm the latest product information and specifications before final design, purchase or use.

HL Microelectronics makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, not does HL Microelectronics assume any liability for application assistance or customer product design.

HL Microelectronics does not warrant or accept any liability with products which are purchased or used for any unintended or unauthorized application.

No license is granted by implication or otherwise under any intellectual property rights of HL Microelectronics.

HL Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of HL Microelectronics.