ISOM811x 3.75-kV$_{RMS}$, Single-Channel Opto-Emulator with Analog Transistor Output

1 Features

- Drop-in replacement and pin-to-pin upgrade to industry-standard phototransistor optocouplers
- 1-channel LED-emulator input
- Current transfer ratio (CTR) at I_F = 5 mA, V_{CE} = 5 V:
  - ISOM8110, ISOM8115: 100% to 155%
  - ISOM8111, ISOM8116: 150% to 230%
  - ISOM8112, ISOM8117: 255% to 380%
  - ISOM8113, ISOM8118: 375% to 560%
- High collector-emitter voltage: V_{CE} (max) = 80 V
- Robust isolation barrier
  - Isolation rating: 3750-V_{RMS}
  - Working voltage: 500-V_{RMS}, 707-V_{PK}
  - Surge capability: up to 10-kV
- Temperature range: –55°C to +125°C
- Response time: 3 µs (typical) at V_{CE} = 10 V, I_C = 2 mA, R_L = 100 Ω
- Safety-related certifications planned:
  - UL 1577 recognition, 3750-V_{RMS} isolation
  - DIN EN IEC 60747-17 (VDE 0884-17) conformity per VDE
  - IEC 62368-1, IEC 61010-1 certifications
  - CQC GB 4943.1 certification

2 Applications

- Switching power supply
- Programmable Logic Controller (PLC)
- Motor drive I/O and position feedback
- Factory automation
- Data acquisition
- HEV/EV battery-management system (BMS)

3 Description

The ISOM811x devices are single-channel optocoupler-emulators with LED-emulator input and transistor output. The devices are pin-compatible and drop-in replacements for many traditional optocouplers, allowing enhancement to existing systems with no PCB redesign.

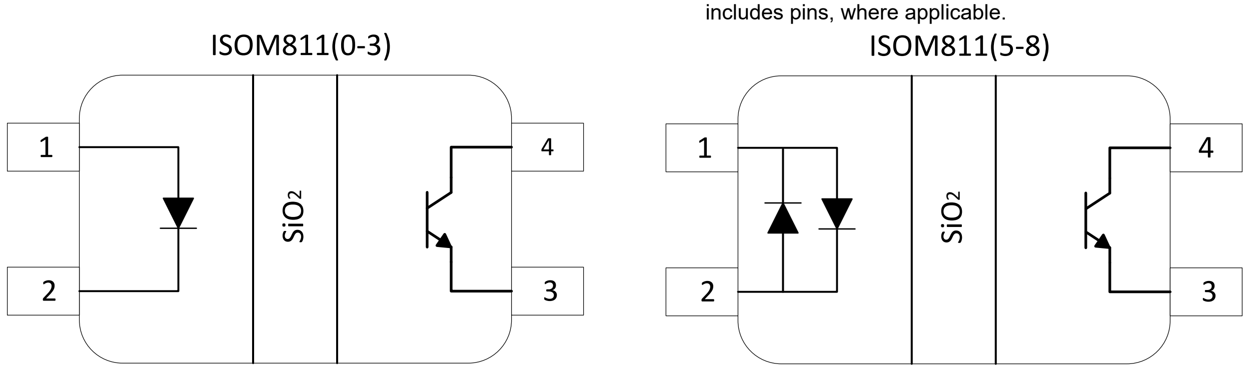
ISOM811x opto-emulators offer significant reliability and performance advantages compared to optocouplers, including high bandwidth, low turn-off delay, low power consumption, wider temperature ranges, and tight CTR and process controls resulting in small part-to-part skew. Since there is no aging effect or temperature variation to compensate for, the emulated LED input stage consumes less power than optocouplers.

ISOM811x devices are offered in small SOIC-4 packages with 2.54-mm and 1.27-mm pin pitchs, supporting a 3.75-kV$_{RMS}$ isolation rating and DC (ISOM811[0-3]) and bi-directional DC (ISOM811[5-8]) input options. The high performance and reliability of ISOM811x enables these devices to be used in power supply feedback design, motor drives, I/O modules in industrial controllers, factory automation applications, and more.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(3)	BODY SIZE (NOM)
ISOM811x	SO-4 (DFG)	7.0 mm × 3.5 mm	4.8 mm × 3.5 mm
	SO-4 (DFH)(2)	7.0 mm × 2.7 mm	4.8 mm × 2.7 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview only.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2023) to Revision A (December 2023)	Page
• Updated to Production Data for ISOM8110	1

5 Device Selection

Table 5-1. Device Selection

PART NUMBER[2]	CTR	PACKAGE[1]	PIN PITCH
ISOM8110, ISOM8115	100% to 155%	4-pin SOIC (DFG), 4-pin SOIC (DFH)	2.54-mm, 1.27-mm
ISOM8111, ISOM8116	150% to 230%		
ISOM8112, ISOM8117	255% to 380%		
ISOM8113, ISOM8118	375% to 560%		

1. DFH package is preview only.
2. ISOM8111-3 and ISOM8115-8 are preview only.

6 Pin Configuration and Functions

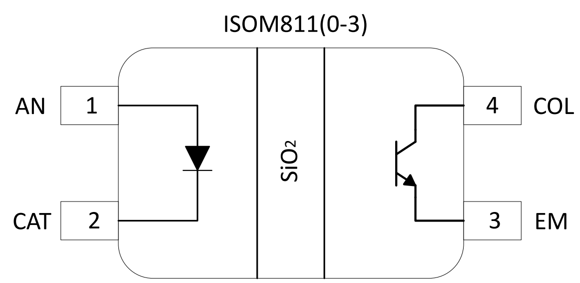


Figure 6-1. ISOM811(0-3) 4-Pin SOIC (Top View)

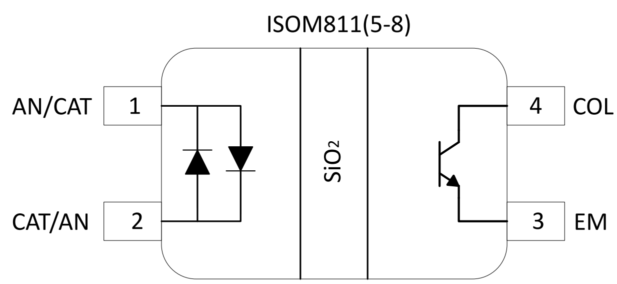


Figure 6-2. ISOM811(5-8) 4-Pin SOIC (Top View)

Table 6-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NO.	NAME		
1	AN	I	Anode connection of input LED emulator
2	CAT	I	Cathode connection of input LED emulator
3	EM	O	Emitter for transistor
4	COL	O	Collector for transistor

(1) I = Input, O = Output

7 Specifications

7.1 Absolute Maximum Ratings

See(1) (2)

			MIN	MAX	UNIT
$I_{F(max)}$	Maximum Input forward current	ISOM8110, ISOM8111, ISOM8112, ISOM8113		50	mA
		ISOM8115, ISOM8116, ISOM8117, ISOM8118		±50	mA
V_{CEO}	Collector-emitter voltage	ISOM8110, ISOM8111, ISOM8112, ISOM8113		80	V
		ISOM8115, ISOM8116, ISOM8117, ISOM8118		80	V
V_{ECO}	Emitter-collector voltage	ISOM8110, ISOM8111, ISOM8112, ISOM8113		7	V
		ISOM8115, ISOM8116, ISOM8117, ISOM8118		7	V
I_{FP}	Input pulse forward current (1 µs width)	ISOM8110, ISOM8111, ISOM8112, ISOM8113		1	A
I_{FP}	Input pulse forward current (1 µs width)	ISOM8115, ISOM8116, ISOM8117, ISOM8118		±1	A
V_R	Input reverse voltage at I_R = 10 µA	ISOM8110, ISOM8111, ISOM8112, ISOM8113		7	V
P_I	Input power dissipation	ISOM8110, ISOM8111, ISOM8112, ISOM8113		140	mW
		ISOM8115, ISOM8116, ISOM8117, ISOM8118		140	mW
I_C	Collector current	ISOM8110, ISOM8111, ISOM8112, ISOM8113		50	mA
		ISOM8115, ISOM8116, ISOM8117, ISOM8118		50	mA
P_C	Collector power dissipation	ISOM8110, ISOM8111, ISOM8112, ISOM8113		150	mW
		ISOM8115, ISOM8116, ISOM8117, ISOM8118		150	mW
P_T	Total power dissipation	ISOM8110, ISOM8111, ISOM8112, ISOM8113		290	mW
		ISOM8115, ISOM8116, ISOM8117, ISOM8118		290	mW
T_A	Ambient temperature	ISOM8110, ISOM8111, ISOM8112, ISOM8113	–55	125	°C
		ISOM8115, ISOM8116, ISOM8117, ISOM8118	–55	125	°C
T_J	Operating junction temperature	ISOM8110, ISOM8111, ISOM8112, ISOM8113		150	°C
		ISOM8115, ISOM8116, ISOM8117, ISOM8118		150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under the operational sections of this document. If used outside the listed operational conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All specifications are at T_A = 25 °C unless otherwise noted

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins [(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

THERMAL METRIC[(1)]		ISOM811x DFG (SOIC) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	288.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	173.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	192.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	121.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	190	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.4 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE 4-DFG	UNIT
IEC 60664-1				
CLR	External clearance(1)	Side 1 to side 2 distance through air	> 5	mm
CPG	External creepage(1)	Side 1 to side 2 distance across package surface	> 5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>400	V
	Material Group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
DIN VDE V 0884-11:2017 (6)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	707	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test	500	V_{RMS}
		DC voltage	707	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	5303	V_{PK}
V_{IMP}	Maximum impulse voltage (2)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	7200	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	$V_{ISOM} \geq 1.3 \times V_{IMP}$; tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b: At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3750	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) Testing is carried out in air to determine the surge immunity of the package.
(3) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.
(6) This coupler is suitable for *safe electrical insulation only* within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

7.5 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 61010-1, IEC 62368-1 and IEC 60601-1	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011	Plan to certify according to EN 61010-1:2010/A1:2019 and EN 62368-1:2014
Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned

7.6 Safety Limiting Values

Safety limiting[(1)] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SO-4 PACKAGE (DFG)						
I_S	Safety limiting input current	$R_{\theta JA}$= 288.8℃/W, V_F = 1.4 V, T_J = 150℃, T_A = 25℃			300	mA
		$R_{\theta JA}$=288.8℃/W, V_{CEO} = 40 V, T_J = 150℃, T_A = 25℃			10.5	mA
		$R_{\theta JA}$= 288.8℃/W, V_{CEO} = 24 V, T_J =150℃, T_A = 25℃			17.5	mA
		$R_{\theta JA}$= 288.8℃/W, V_{CEO} = 15 V, T_J = 150℃, T_A = 25℃			28	mA
P_S	Safety limiting total power	$R_{\theta JA}$= 288.8℃/W, T_J = 150℃, T_A = 25℃			420	mW
T_S	Maximum safety temperature				135	℃

(1) The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

7.7 Electrical Characteristics

All specifications are at T_A = 25 °C unless otherwise noted

PARAMETER		TEST CONDITIONS	GPN	MIN	TYP	MAX	UNIT
INPUT							
V_F	Input forward voltage	I_F = 5 mA	ISOM8110, ISOM8111, ISOM8112, ISOM8113		1.2	1.4	V
V_F	Input forward voltage	I_F = ±5 mA	ISOM8115, ISOM8116, ISOM8117, ISOM8118		1.2	1.5	V
I_R	Input reverse current	V_R = 5 V	ISOM8110, ISOM8111, ISOM8112, ISOM8113			10	uA
C_{IN}	Input capacitance	At 1 MHz, V_F = 0 V	ISOM8110, ISOM8111, ISOM8112, ISOM8113		35		pF
C_{IN}	Input capacitance	At 1 MHz, V_F = 0 V	ISOM8115, ISOM8116, ISOM8117, ISOM8118		6		pF
OUTPUT							
C_{CE}	Collector-emitter capacitance	1 MHz, V_F = 0 V	ISOM811x		12		pF
$V_{CE(SAT)}$	Collector-emitter saturation voltage	I_F = 20 mA, I_C = 1 mA	ISOM8110, ISOM8111, ISOM8112, ISOM8113			0.3	V
$V_{CE(SAT)}$	Collector-emitter saturation voltage	I_F = ±20 mA, I_C = 1 mA	ISOM8115, ISOM8116, ISOM8117, ISOM8118			0.3	V
Dark Current	Collector dark current	V_{CE} = 20 V, I_F = 0 mA	ISOM811x			100	nA
I_{EC}	Reverse current	V_{EC} = 7 V, I_F = 0 mA	ISOM811x			100	μA
IC_OFF	OFF_state collector current	V_F = 0.7 V, V_{CE} = 48 V	ISOM8110, ISOM8111, ISOM8112, ISOM8113			10	uA
IC_OFF	OFF_state collector current	V_F = ±0.7 V, V_{CE} = 48 V	ISOM8115, ISOM8116, ISOM8117, ISOM8118			10	uA
CTR(1)							
CTR	Current Transfer Ratio	I_C / I_F (T_A = 25°C), I_F = 0.5 mA, V_{CE} = 5 V	ISOM8110	55	130	195	%
			ISOM8115	55	130	195	%
			ISOM8111	80	180	290	%
			ISOM8116	80	180	290	%
			ISOM8112	135	300	480	%
			ISOM8117	135	300	480	%
			ISOM8113	195	440	710	%
			ISOM8118	195	440	710	%

All specifications are at T_A = 25 ℃ unless otherwise noted

PARAMETER		TEST CONDITIONS	GPN	MIN	TYP	MAX	UNIT
CTR	Current Transfer Ratio	I_C / I_F (T_A = 25°C), I_F = 2 mA, V_{CE} = 5V	ISOM8110	70	120	170	%
			ISOM8115	70	120	170	%
			ISOM8111	110	180	260	%
			ISOM8116	110	180	260	%
			ISOM8112	185	300	430	%
			ISOM8117	185	300	430	%
			ISOM8113	265	440	635	%
			ISOM8118	265	440	635	%
CTR	Current Transfer Ratio	I_C / I_F (T_A = 25°C), I_F = 5 mA, V_{CE} = 5 V	ISOM8110	100	120	155	%
			ISOM8115	100	120	155	%
			ISOM8111	150	180	230	%
			ISOM8116	150	180	230	%
			ISOM8112	255	300	380	%
			ISOM8117	255	300	380	%
			ISOM8113	375	440	560	%
			ISOM8118	375	440	560	%

(1) CTR (%) = (I_C / I_F) x 100%

7.8 Switching Characteristics

All specifications are at T_A = 25 ℃ unless otherwise noted

PARAMETER		TEST CONDITIONS	GPN	MIN	TYP	MAX	UNIT
AC							
t_r	Rise time, see Figure 8-2 and Figure 8-3	V_{CC} = 10 V, I_C = 2 mA, R_L= 100 Ω, C_L = 50 pF	ISOM8110		3.2		µs
			ISOM8113		1.1		µs
t_f	Fall time, see Figure 8-2 and Figure 8-3	V_{CC} = 10 V, I_C = 2 mA, R_L= 100 Ω, C_L = 50 pF	ISOM8110		4.0		µs
			ISOM8113		7.5		µs
T_{ON}	Turn on time, see Figure 8-2 and Figure 8-3	V_{CC} = 10 V, I_C = 2 mA, R_L= 100 Ω, C_L = 50 pF	ISOM8110, ISOM8115		5.7		µs
			ISOM8111, ISOM8116		9.5		µs
			ISOM8112, ISOM8117		8.1		µs
			ISOM8113, ISOM8118		20		µs
T_{OFF}	Turn off time, see Figure 8-2 and Figure 8-3	V_{CC} = 10 V, I_C = 2 mA, R_L= 100 Ω, C_L = 50 pF	ISOM8110, ISOM8115		3.6		µs
			ISOM8111, ISOM8116		2.3		µs
			ISOM8112, ISOM8117		1.7		µs
			ISOM8113, ISOM8118		0.68		µs
t_s	Storage time; time required for the output waveform to change from 0% (100%) to 10% (90%) when input is turned on and back off, see, see Figure 8-3	V_{CC} = 5 V, I_F = 1.6 mA, R_L = 4.7 kΩ	ISOM811x			21	µs
BW	Bandwidth, see Figure 8-4 and Figure 8-5	V_{IN_DC} = 5 V, V_{IN_AC} = 1 Vpk, R_{IN} = 2 kΩ V_{CC}= 5 V, R_{LOAD} = 100 Ω, C_L = 50 pF, measured at V_{CE} –3dB sinewave	ISOM8110, ISOM8115		680		kHz
			ISOM8111, ISOM8116		680		kHz
			ISOM8112, ISOM8117		680		kHz
			ISOM8113, ISOM8118		680		kHz

7.9 Typical Characteristics

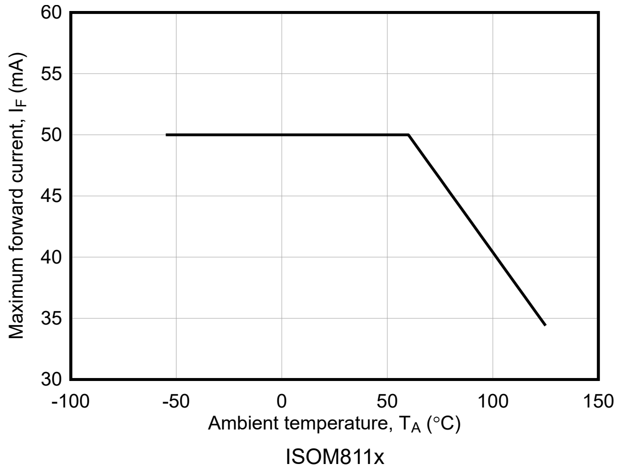


Figure 7-1. Maximum Forward Current vs Ambient Temperature

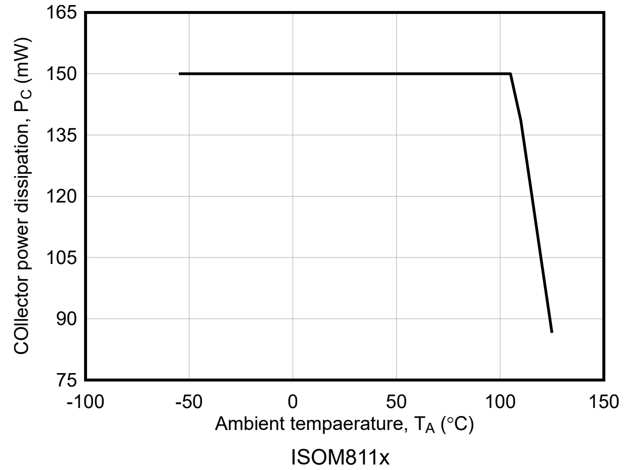


Figure 7-2. Maximum Collector Power Dissipation vs Ambient Temperature

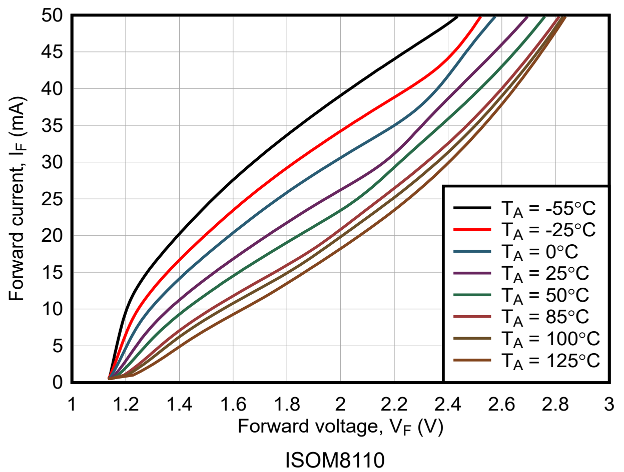


Figure 7-3. Forward Voltage vs Forward Current

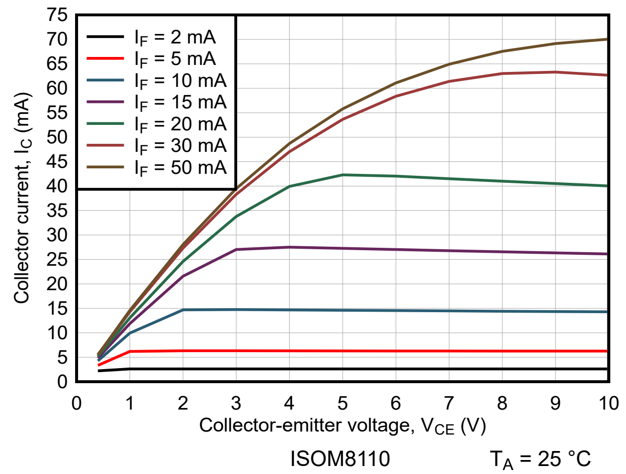


Figure 7-4. Collector Current vs Collector-Emitter Voltage

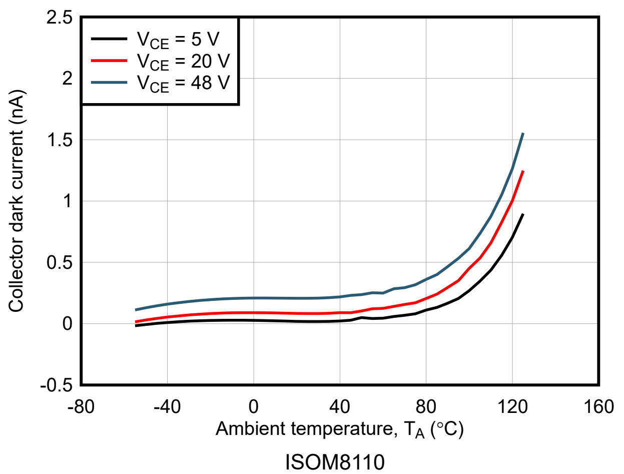


Figure 7-5. Collector Dark Current vs Ambient Temperature

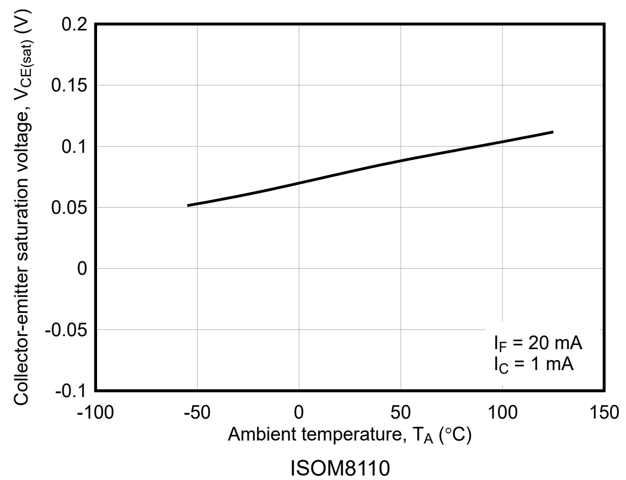
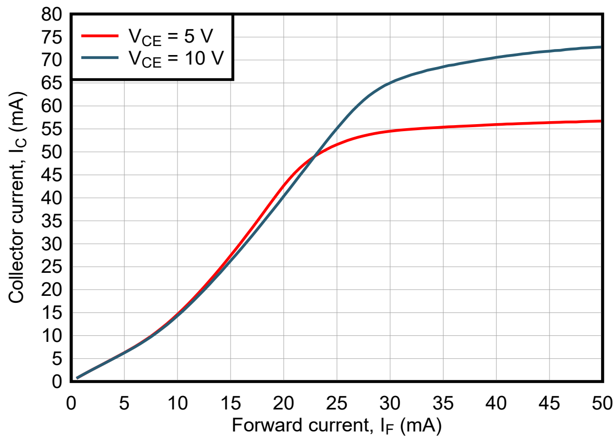
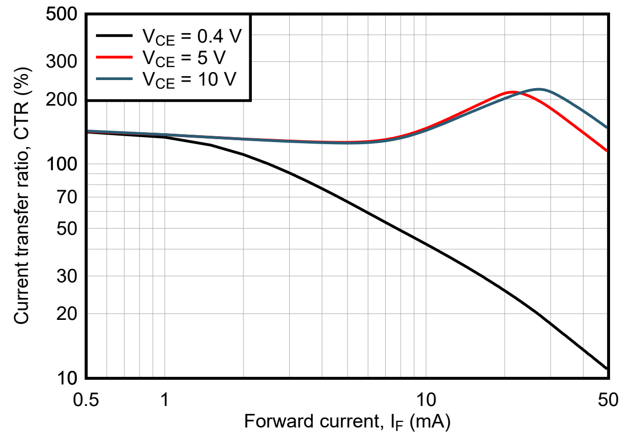


Figure 7-6. Collector-Emitter Saturation Voltage vs Ambient Temperature



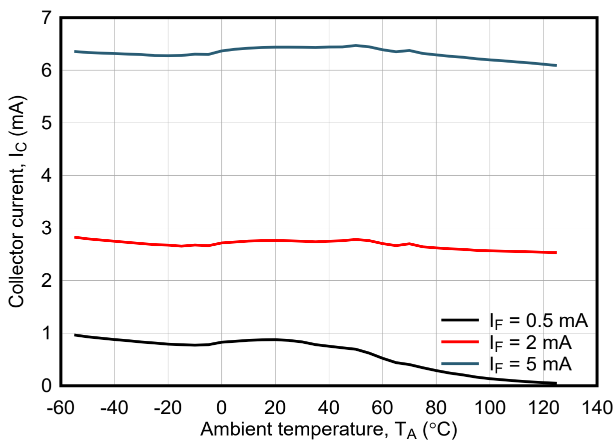
ISOM8110 T_A = 25 °C

Figure 7-7. Collector Current vs Forward Current



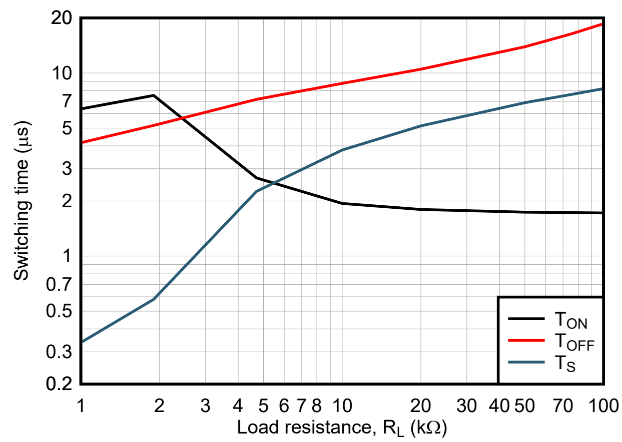
ISOM8110 T_A = 25 °C

Figure 7-8. Current Transfer Ratio vs Forward Current



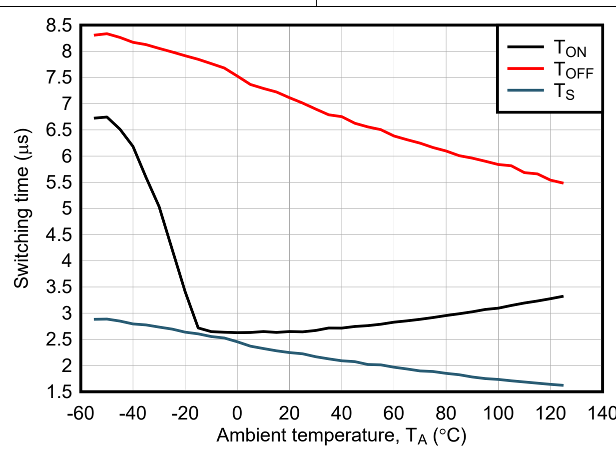
ISOM8110 V_{CE} = 5 V

Figure 7-9. Collector Current vs Ambient Temperature



I_F = 1.6 mA ISOM8110 V_{CC} = 5 V

Figure 7-10. Switching Time vs Load Resistance



I_F = 1.6 mA
R_L = 4.7 kΩ
ISOM8110
V_{CC} = 5 V

Figure 7-11. Switching Time vs Ambient Temperature

8 Parameter Measurement Information

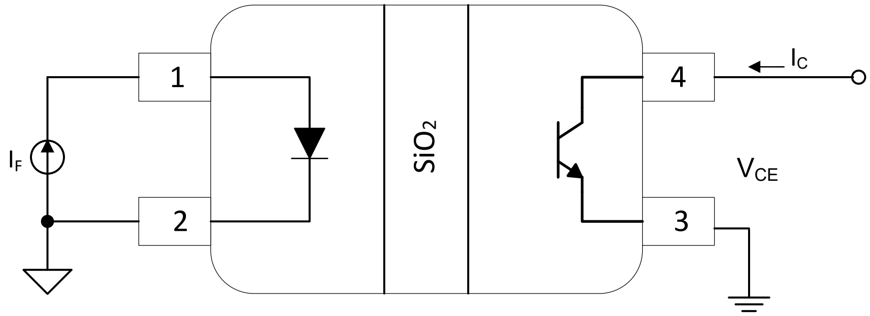


Figure 8-1. ISOM811x Test Circuit for CTR

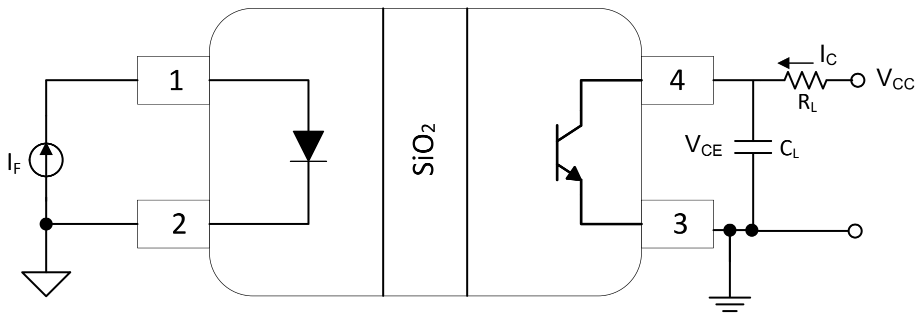


Figure 8-2. ISOM811x Test Circuit for Switching Timing

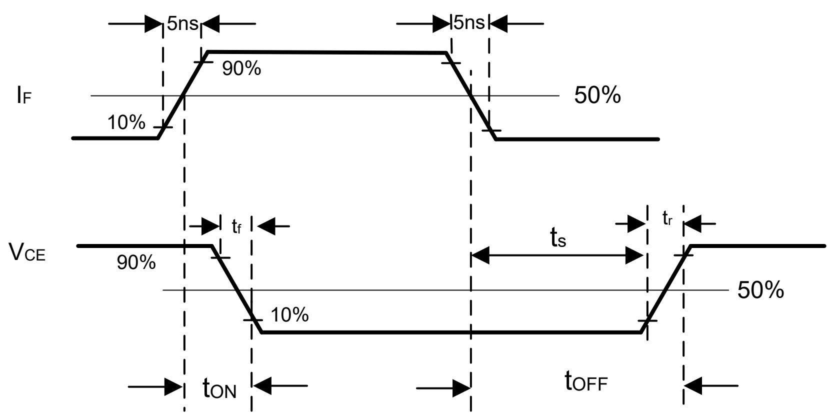


Figure 8-3. ISOM811x Switching Timing Waveforms

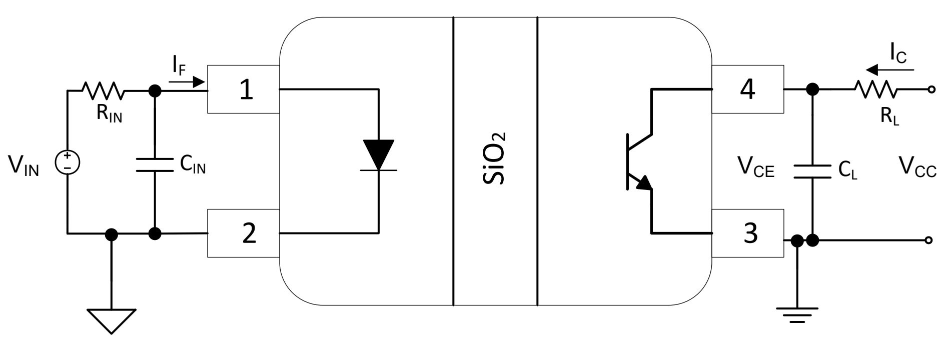


Figure 8-4. ISOM811(0-3) Test Circuit for Bandwidth

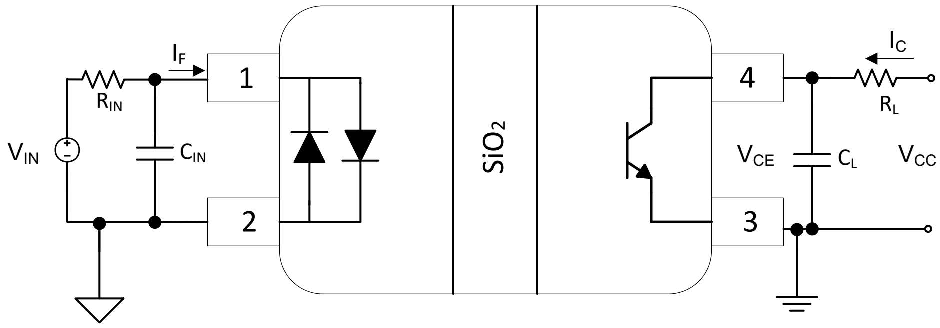


Figure 8-5. ISOM811(5-8) Test Circuit for Bandwidth

9 Detailed Description

9.1 Overview

The ISOM811x opto-emulators are pin-compatible, single-channel, drop-in replacements for many traditional optocouplers. While standard optocouplers use an LED as the input stage, ISOM811x uses an emulated LED as the input stage. The input and output stages are isolated by TI's proprietary silicon dioxide-based (SiO_2) isolation barrier. This isolation technology makes ISOM811x resistant to the wear-out effects found in optocouplers that degrade performance with increasing temperature, forward current, and device age. Ordering options include four different ranges of current transfer ratio (CTR) and input options supporting uni-polar and bi-polar DC flow.

The ISOM811x family of devices isolate DC and bi-directional DC signals and offer performance, reliability, and flexibility advantages not available with traditional optocouplers.

The functional block diagram of ISOM811x devices are shown in Section 9.2. The input signal is transmitted across the isolation barrier using an on-off keying (OOK) modulation scheme. The transmitter sends a high-frequency carrier across the barrier that contains information on how much current is flowing through the input pins. The receiver demodulates the signal after advanced signal conditioning and produces the signal through the output stage. These devices also incorporate advanced circuit techniques to maximize bandwidth and minimize radiated emissions. Figure 9-3 shows conceptual details of how the OOK scheme works.

9.2 Functional Block Diagram

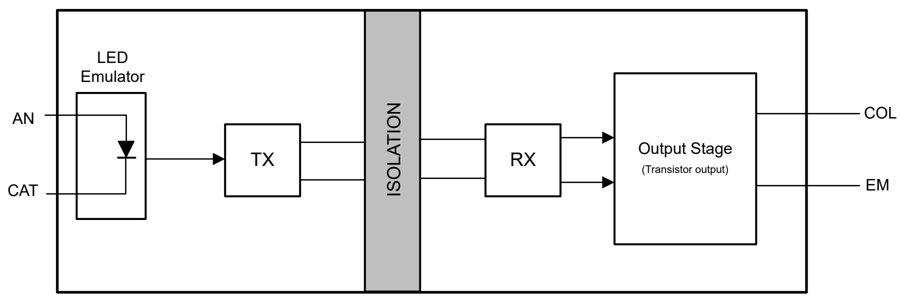


Figure 9-1. Conceptual Block Diagram of an Opto-emulator ISOM811(0-3)

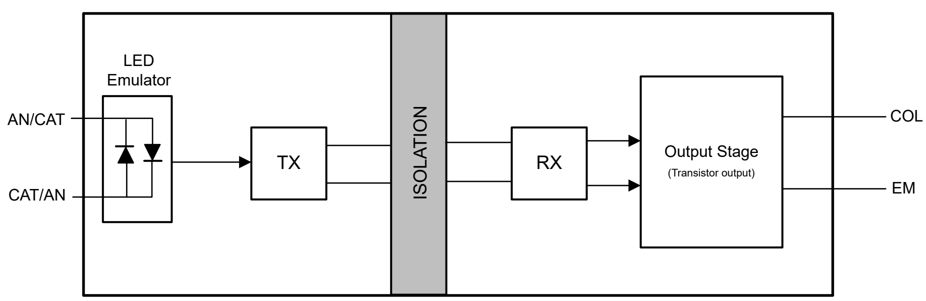


Figure 9-2. Conceptual Block Diagram of an Opto-emulator ISOM811(5-8)

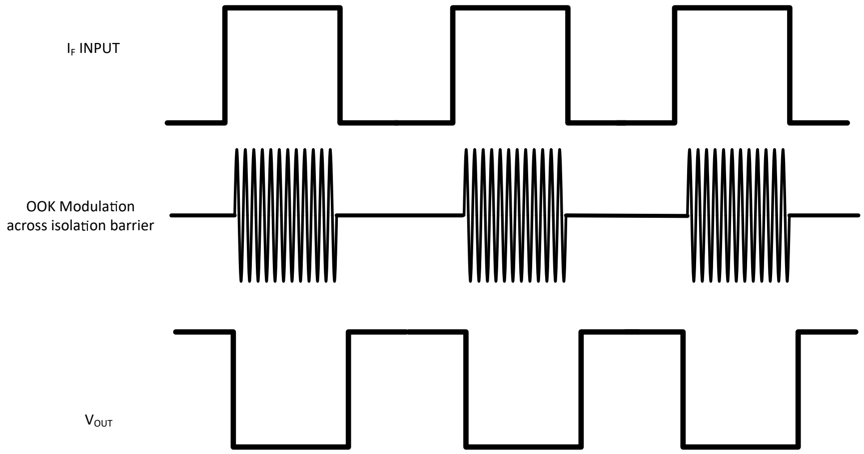


Figure 9-3. On-off Keying (OOK) Based Modulation Scheme

9.3 Feature Description

The ISOM811x devices isolate DC and bi-directional DC signals. ISOM811x has an open-collector output with four different CTR options. All devices support an isolation withstand voltage of 3750 V_{RMS} between side 1 and side 2.

9.4 Device Functional Modes

Table 9-1 lists the functional modes for the ISOM811x devices.

Table 9-1. Function Table

CTR[1]	PART NUMBER	Input type
100% to 155%	ISOM8110	DC
	ISOM8115	Bidirectional DC
150% to 230%	ISOM8111	DC
	ISOM8116	Bidirectional DC
255% to 380%	ISOM8112	DC
	ISOM8117	Bidirectional DC
375% to 560%	ISOM8113	DC
	ISOM8118	Bidirectional DC

1. I_F = 5 mA, T_A = 25 °C, V_{CE} = 5 V.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISOM811x devices are single-channel opto-emulators with LED-emulator input and transistor output. The devices use on-off keying modulation to transmit data across the isolation barrier. The input stage is isolated from the driver stage by TI's proprietary silicon dioxide-based (SiO_2) isolation barrier which provides robust isolation. With wider temperature ratings than traditional optocouplers, ISOM811x opto-emulators can provide reliable signal isolation in harsh environments.

The ISOM811x devices are capable of sinking current when subjected to an external load being connected to the device. Like typical transistor output optocouplers, the output current will depend on the input current level (I_F) and the current transfer ratio (CTR). With multiple CTR options (100% - 560%), low input current, high bandwidth, low turn-off delay, low power consumption, and wider temperature range, ISOM811x devices are ideal for use in a variety of industries such as factory automation, building automation, e-mobility, automotive, avionics, medical, and power delivery.

10.1.1 Typical Application

ISOM811x opto-emulators are commonly used in the feedback control loops of isolated power supplies. These devices are used to solve the problem of feeding back current while isolating the primary and secondary domains to regulate the output voltage.

In power supplies, the output voltage is isolated from main input voltage using a transformer (for example: flyback converter). For analog power supply units, the controller IC is usually on the primary side of the transformer. For closed loop control, it is necessary to measure the output voltage on the secondary side and feed it back to the controller on the primary. The most common way of achieving this is using an opto-emulator such as ISOM811x, error amplifier (commonly TL431), and a voltage comparator to form a feedback loop across the isolation barrier

Figure 10-1 illustrates a typical isolated power supply. In this implementation, the output voltage is sensed by an error amplifier via the resistor divider (R1 and R2). Depending on the voltage level that it senses, the TL431 can drive the current of the ISOM811x higher or lower which is then compared to a voltage reference. The information is passed across the isolation barrier through ISOM811x to the primary side, where the PWM control circuit modulates the power stage to regulate the output voltage. The TL431 and ISOM811x play an important role for stable feedback and control loop.

The ISOM811x devices enable improvements in transient response, reliability, and stability as compared to commonly used optocoupler as the CTR is stable over wide temperature range of -55°C to 125°C providing a small, low-cost, highly reliable, and easy-to-design solution.

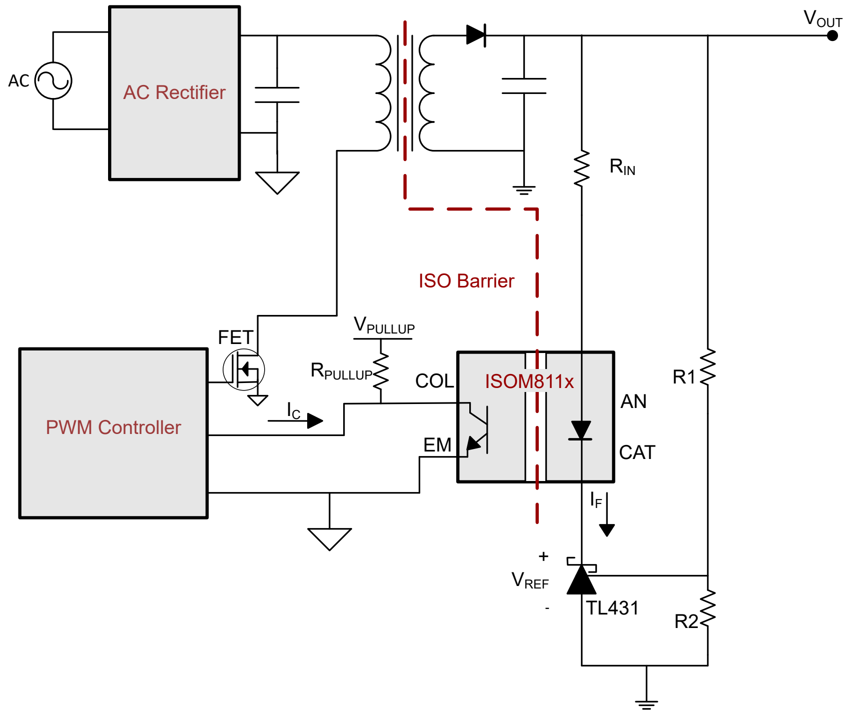


Figure 10-1. Typical Isolated Power Supply Application Using ISOM811x

10.1.1.1 Design Requirements

To design with ISOM811x devices, use the parameters listed in Table 10-1.

Table 10-1. Design Parameters

PARAMETER	VALUE
Input forward current range, I_F	0.5 mA (min), 50 mA (max)
Current transfer ratio at I_F = 5 mA, CTR	100% to 155%
Collector current tolerance, I_C	50 mA (max)
Collector-emitter voltage (saturation), $V_{CE(SAT)}$	0.3 V (max)
Input forward voltage, V_F	1.2 V (typ)

10.1.1.2 Detailed Design Procedure

This section presents the design procedure for using the ISOM811x opto-emulators. External components should be selected to operate ISOM811x within the *Recommended Operating Conditions*. The following recommendations on component selection focus on the design of a typical feedback control loop for an isolated flyback converter.

When using an optocoupler in a feedback control loop for an isolated power supply, many variables can affect how to properly use the optocoupler, including the output voltage of the power supply and the type of controller the feedback signal is being sent to. For this example, let's assume the output voltage of this power supply, V_{OUT}, is 5 V, and the PWM controller being used has an integrated error amplifier with a COMP pin that acts as the output of this amplifier.

Sizing R_{PULLUP}

The transistor output of ISOM811x will operate in active, saturation, reverse, and cut-off regions, just like a regular transistor. To ensure the output does not get damaged when it is saturated, the minimum value of R_{PULLUP} can be calculated for a given pull-up voltage, V_{PULLUP}, in Equation 1 below:

$$R_{PULLUP} > \frac{V_{PULLUP} - V_{CE(SAT)}}{I_{C(MAX)}} \quad (1)$$

For the example of a feedback loop application, we can calculate the minimum required value for R_{PULLUP} for a given V_{PULLUP} of 10 V, the max output voltage of the error amplifier ($V_{COMP(MAX)}$ of 2.5 V, and the max output current of the error amplifier is internally clamped at 1.6 mA. The equation to calculate R_{PULLUP} is shown in Equation 2 below:

$$R_{PULLUP} > \frac{V_{PULLUP} - V_{COMP(MAX)}}{I_{COMP(CLAMP)}} = \frac{10\,V\; - \;2.5\,V}{1.6\,mA} = 4.66\,k\Omega \quad (2)$$

Sizing R_{IN}

The input side of ISOM811x is current-driven. To limit the amount of current flowing into the AN pin, it is recommended that a series resistor, R_{IN}, is used in series with the input as shown in Figure 10-1.

Depending on how the ISOM811x device is being used, the value of R_{IN} can vary quite a bit. However, at a high level, to make sure the input does not get damaged, the minimum value of R_{IN} can be calculated for a given input voltage, V_{IN}, in Equation 3 below:

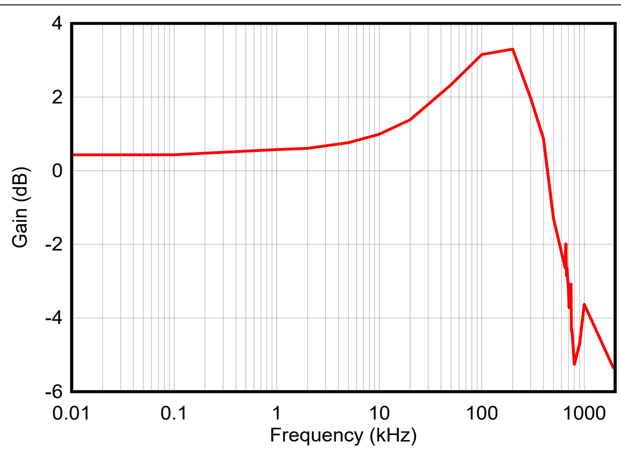
$$R_{IN} > \frac{V_{IN} - V_F}{I_{C(MAX)}} \quad (3)$$

However, in the use case of a feedback loop, R_{IN} directly affects the mid-band gain of the loop. Let's assume the TL431 has been configured to give a reference voltage, V_{REF}, of 2.5 V and R_{PULLUP} is 5 kΩ. Equation 4 is used to calculate the maximum value of R_{IN} ensuring that V_{COMP} voltage on the primary side can be pulled to the saturation voltage of the ISOM811x, $V_{CE(SAT)}$.

$$R_{IN} < \frac{(V_{OUT} - V_{REF} - V_F) \times R_{PULLUP} \times CTR_{MIN}}{V_{PULLUP} - V_{CE(SAT)}} = \frac{(5\,V - 2.5\,V - 1.2\,V) \times 5\,k\Omega \times 100\%}{10\,V \; - \; 0.3\,V} = 670\,\Omega \quad (4)$$

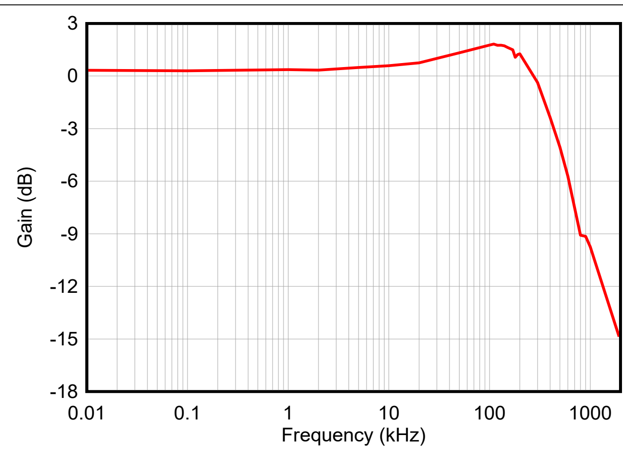
10.1.1.3 Application Curves

The following curves show ISOM8110 bandwidth performance over different loading conditions where V_{IN} = 5 V_{DC} + 2 V_{PK}. See Figure 8-4 for setup details.



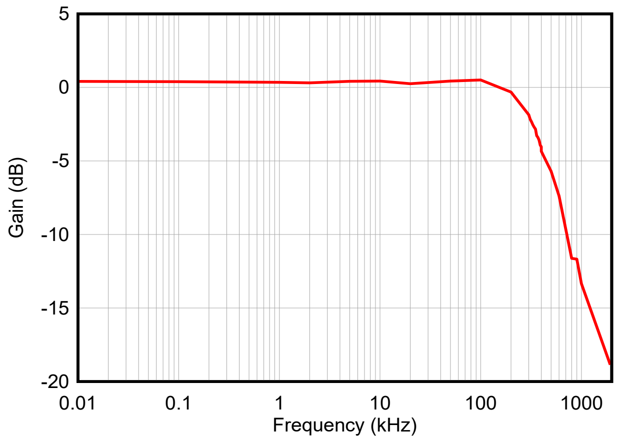
C_{IN} = 5 pF R_{IN} = 2 kΩ C_L = 50 pF R_L = 100 Ω V_{CC} = 5 V

Figure 10-2. Bandwidth at R_L = 100 Ω



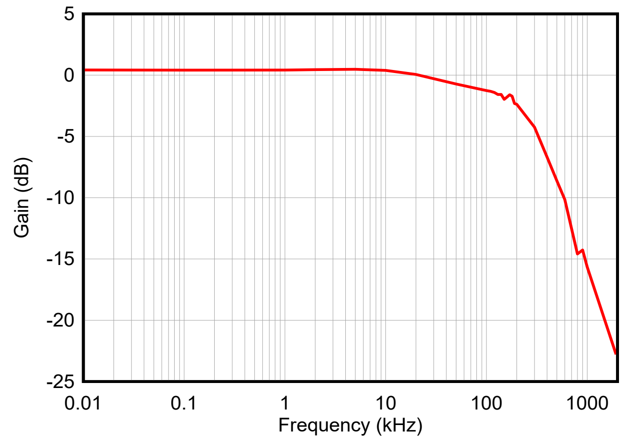
C_{IN} = 5 pF R_{IN} = 2 kΩ C_L = 50 pF R_L = 1 kΩ V_{CC} = 8 V

Figure 10-3. Bandwidth at R_L = 1 kΩ



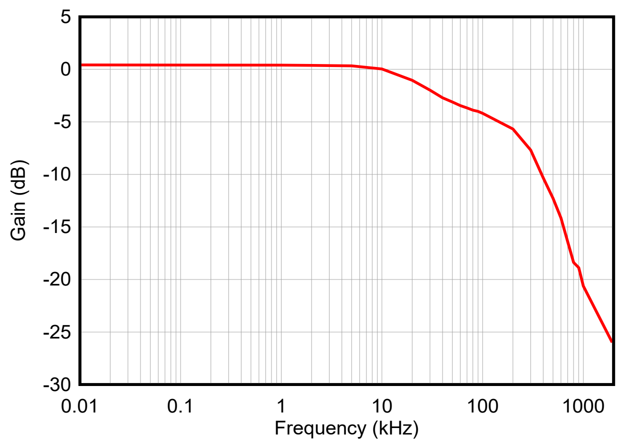
C_{IN} = 5 pF R_{IN} = 2 kΩ C_L = 50 pF R_L = 2 kΩ V_{CC} = 10 V

Figure 10-4. Bandwidth at R_L = 2 kΩ



C_{IN} = 5 pF R_{IN} = 2 kΩ C_L = 50 pF R_L = 4.7 kΩ V_{CC} = 10 V

Figure 10-5. Bandwidth at R_L = 4.7 kΩ



C_{IN} = 5 pF R_{IN} = 2 kΩ C_L = 50 pF R_L = 10 kΩ V_{CC} = 45 V

Figure 10-6. Bandwidth at R_L = 10 kΩ

10.2 Power Supply Recommendations

ISOM811x does not require a dedicated power supply to operate since there is no supply pin. Take care to not violate recommended I/O specifications for proper device functionality.

10.3 Layout

10.3.1 Layout Guidelines

- The device connections to ground should be tied to the PCB ground plane using a direct connection or two vias to help minimize inductance.
- The connections of capacitors and other components to the PCB ground plane should use a direct connection or two vias for minimum inductance.

10.3.2 Layout Example

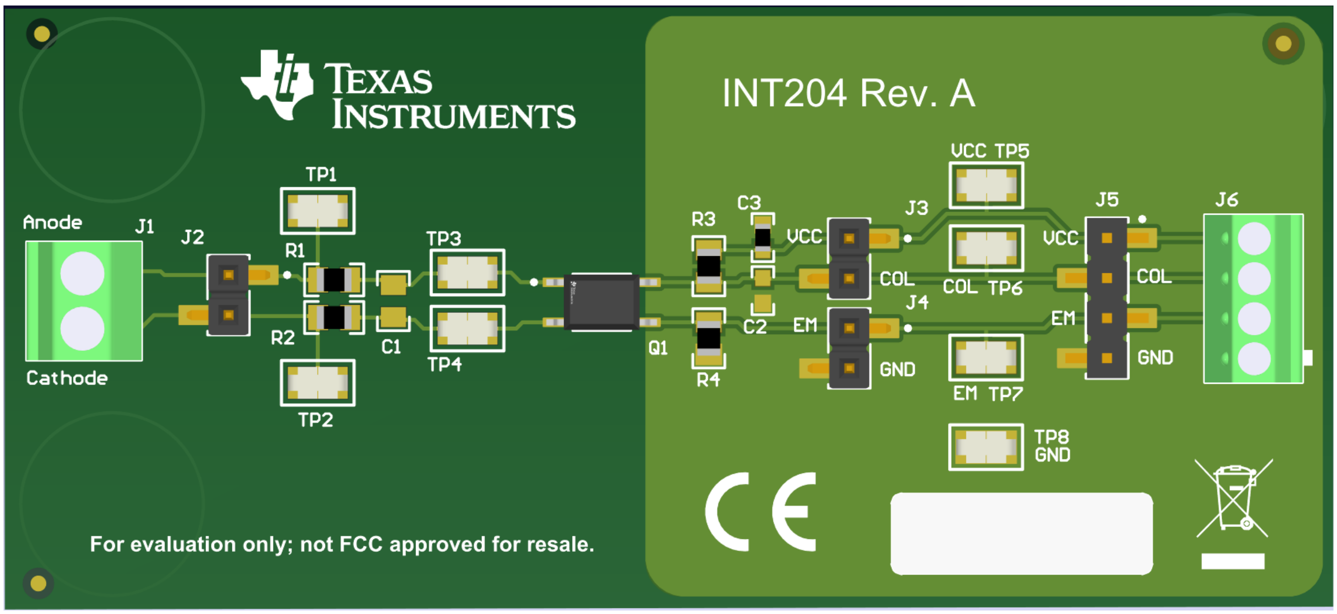


Figure 10-7. Layout Example of ISOM811x with a Single Layer Board

11 Mechanical, Packaging, and Orderable Information

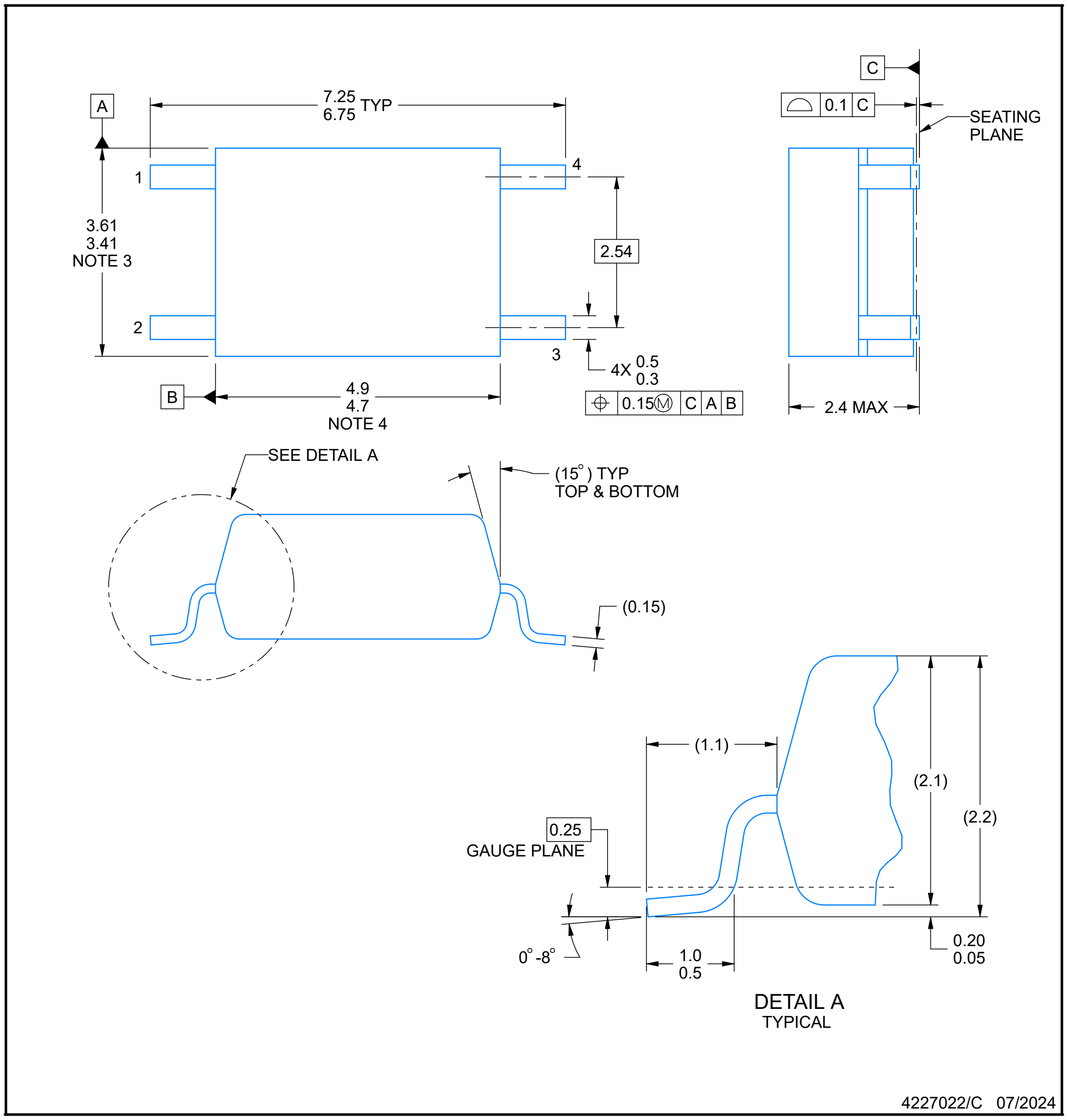
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DFG0004A

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

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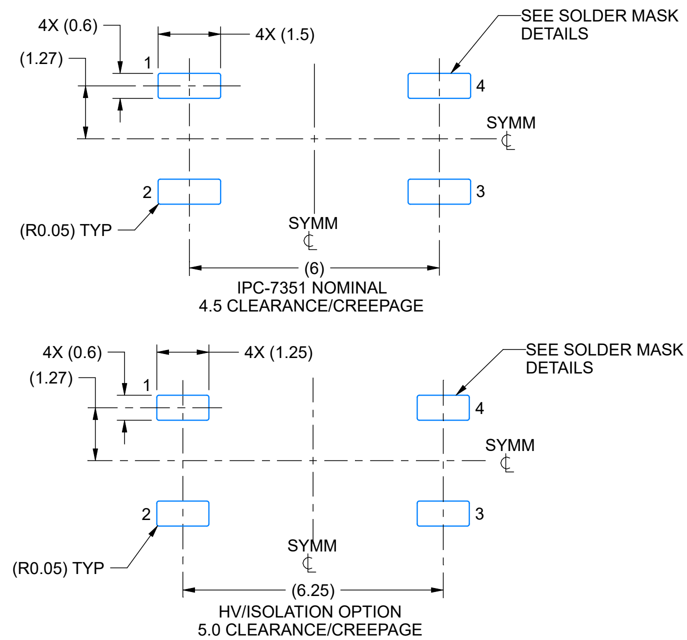
EXAMPLE BOARD LAYOUT

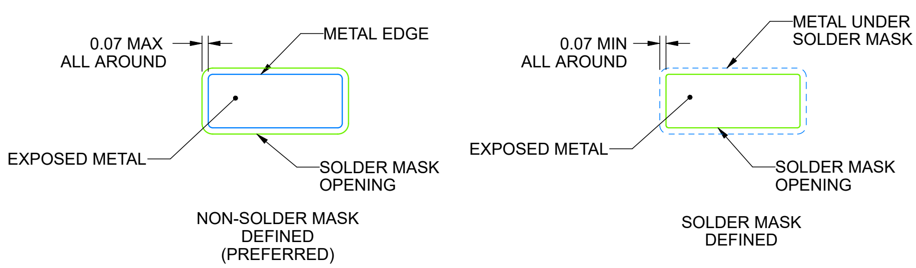
DFG0004A

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X



SOLDER MASK DETAILS

4227022/C 07/2024

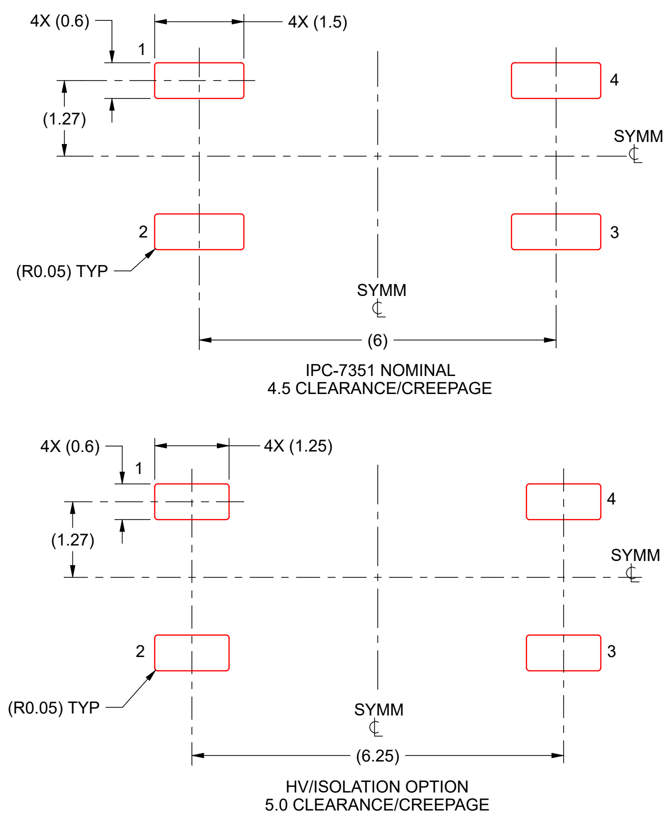
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DFG0004A **SOIC - 2.4 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

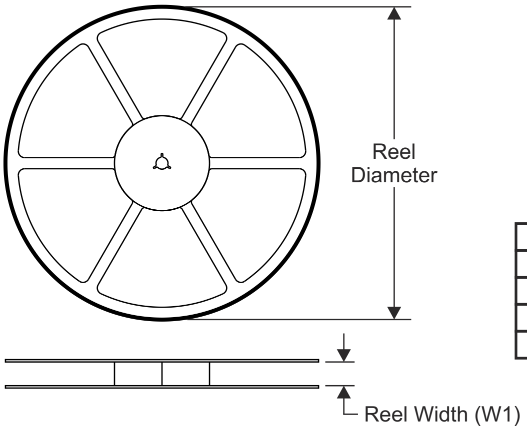
4227022/C 07/2024

NOTES: (continued)

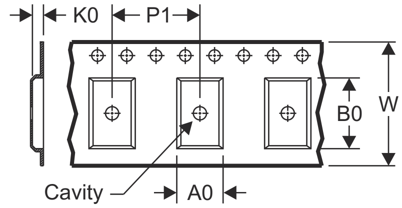
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

11.1 Tape and Reel Information

REEL DIMENSIONS

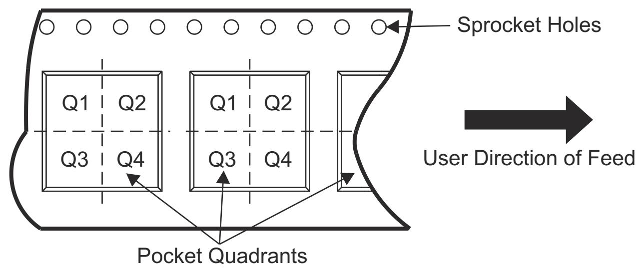


TAPE DIMENSIONS



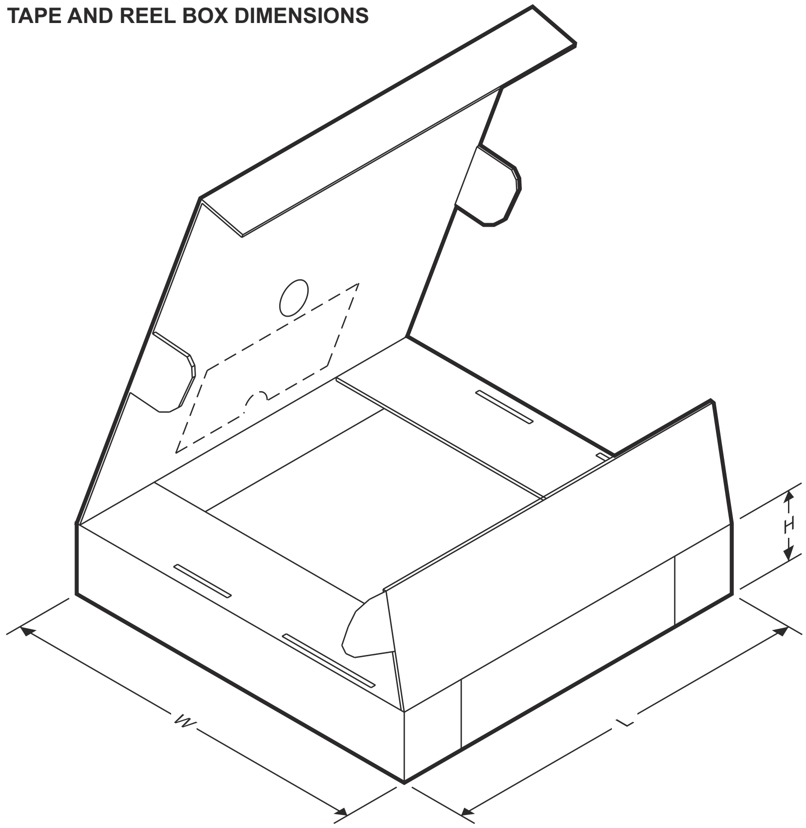
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOM8110DFGR	SO-4	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



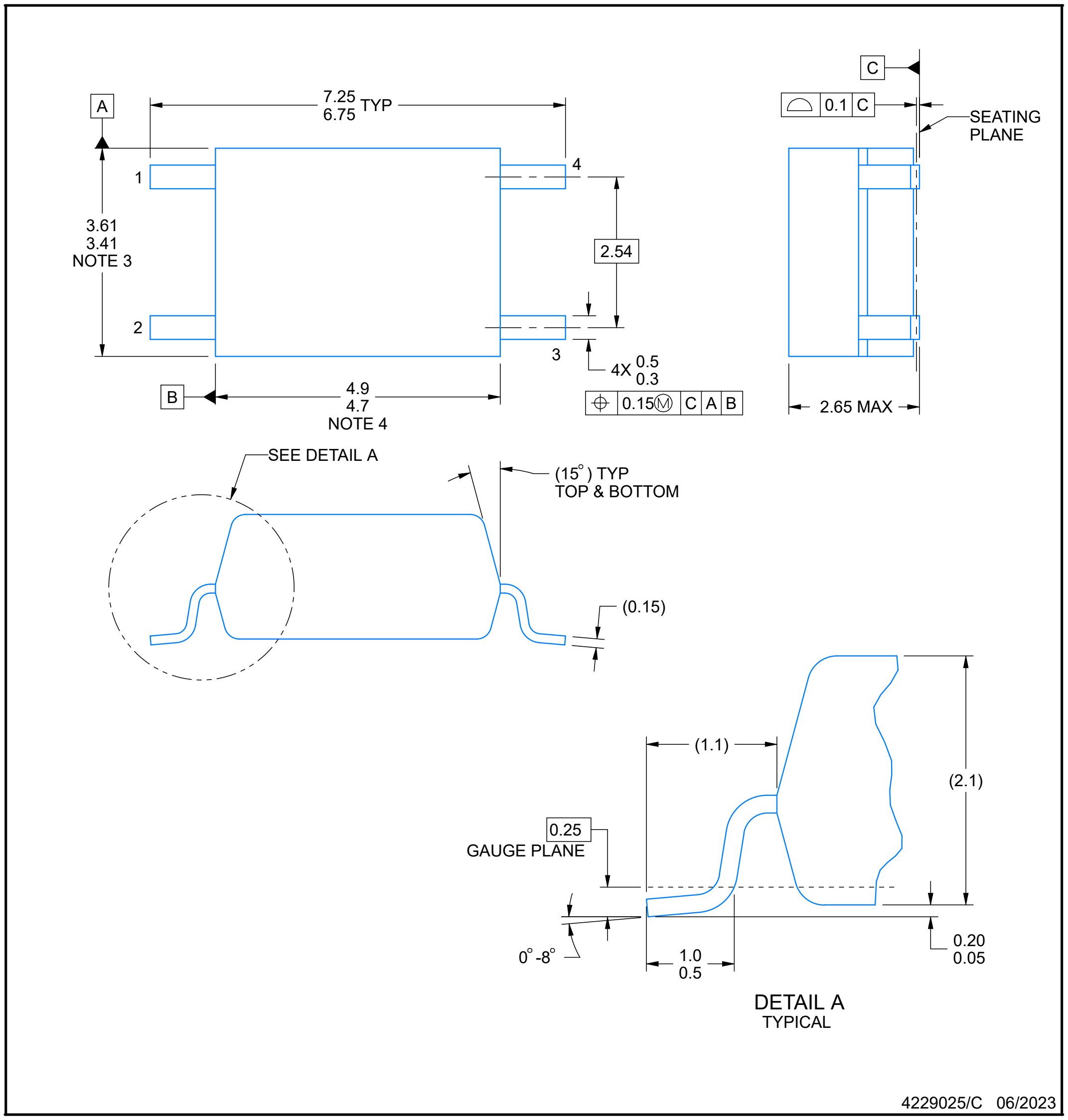
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOM8110DFGR	SO-4	DFG	4	2000	356.0	356.0	35.0

PACKAGE OUTLINE

DFG0004A-C01

SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

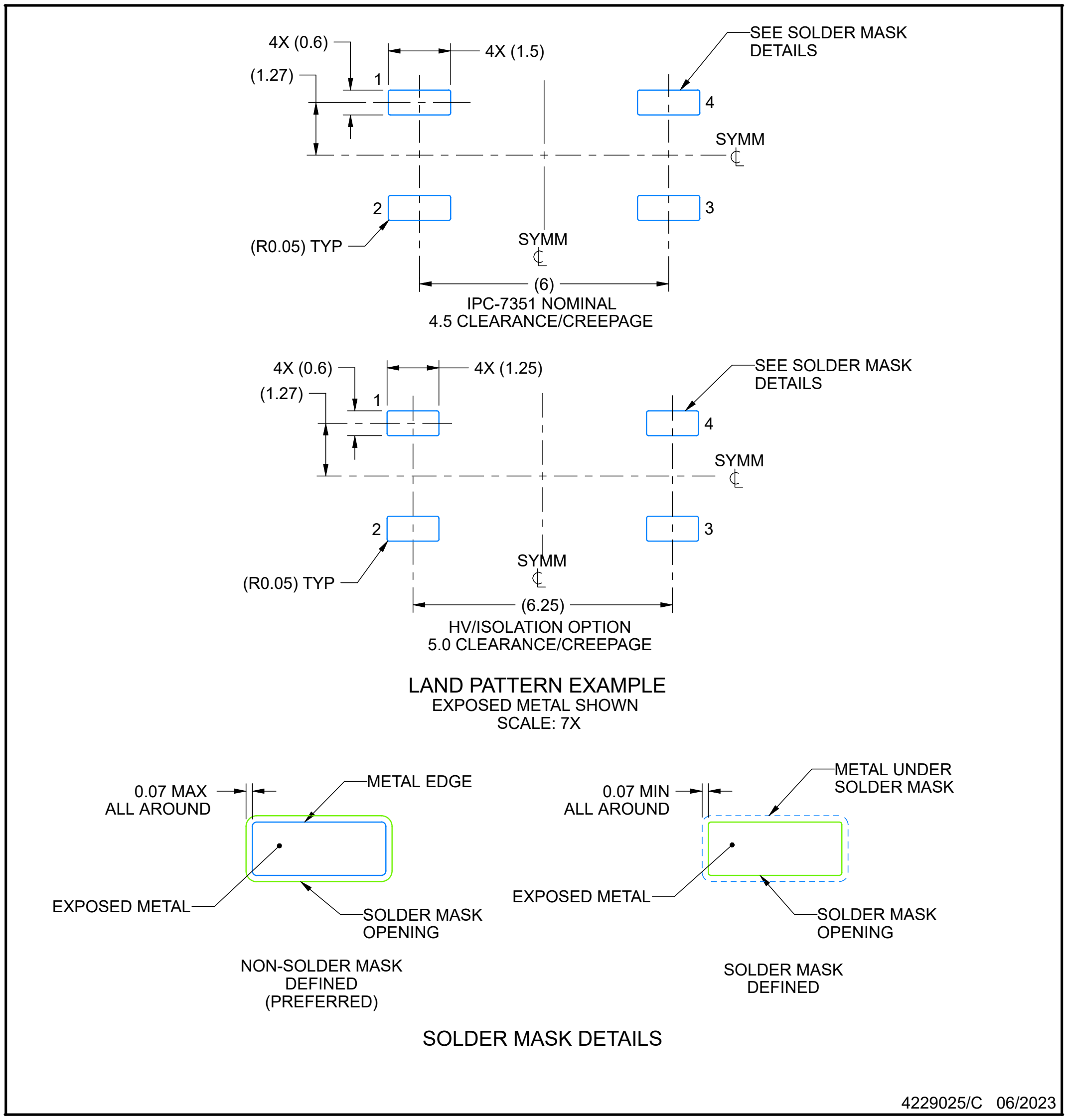
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

DFG0004A-C01

SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

TEXAS INSTRUMENTS
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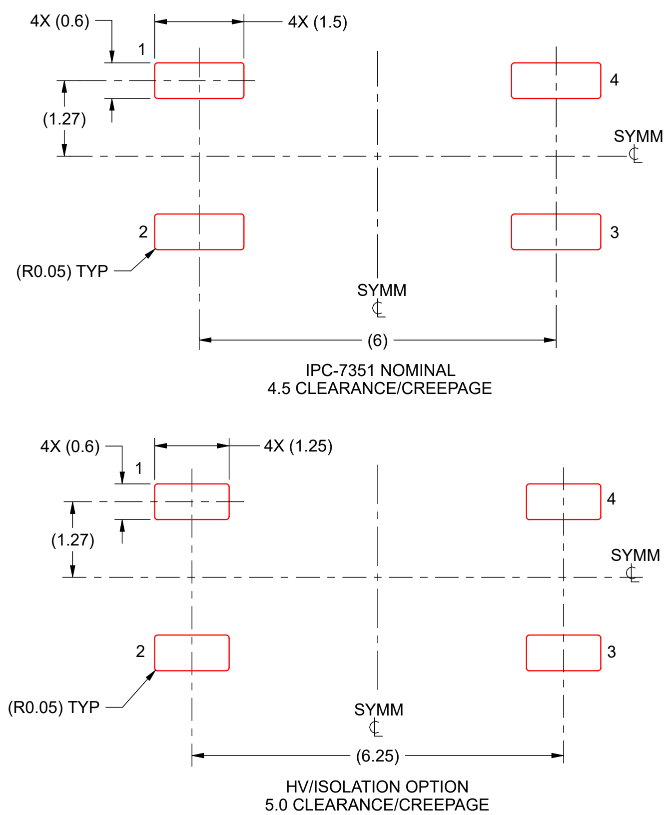
EXAMPLE STENCIL DESIGN

DFG0004A-C01

SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4229025/C 06/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISOM8110DFGR	ACTIVE	SOIC	DFG	4	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8110	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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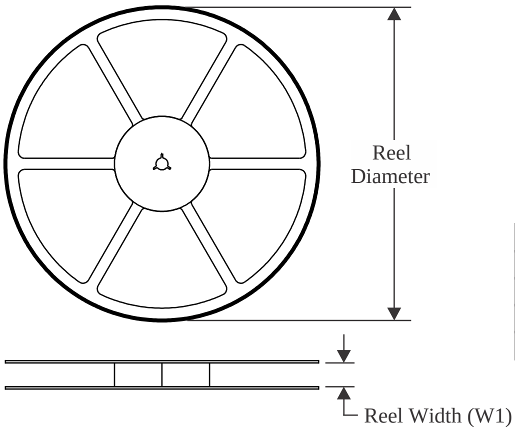
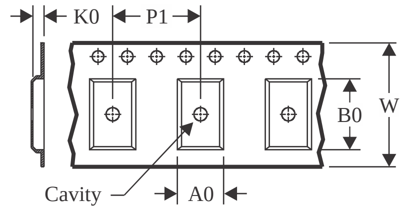
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

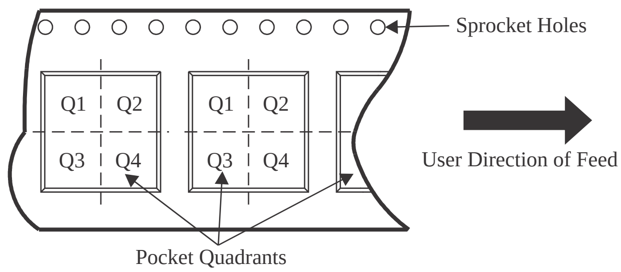


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

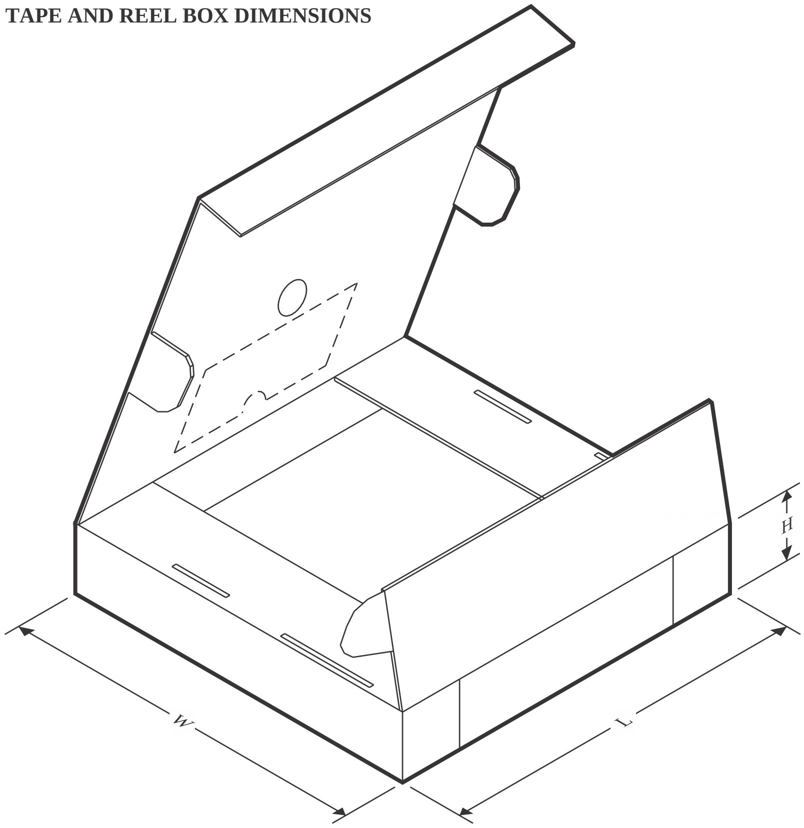
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOM8110DFGR	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

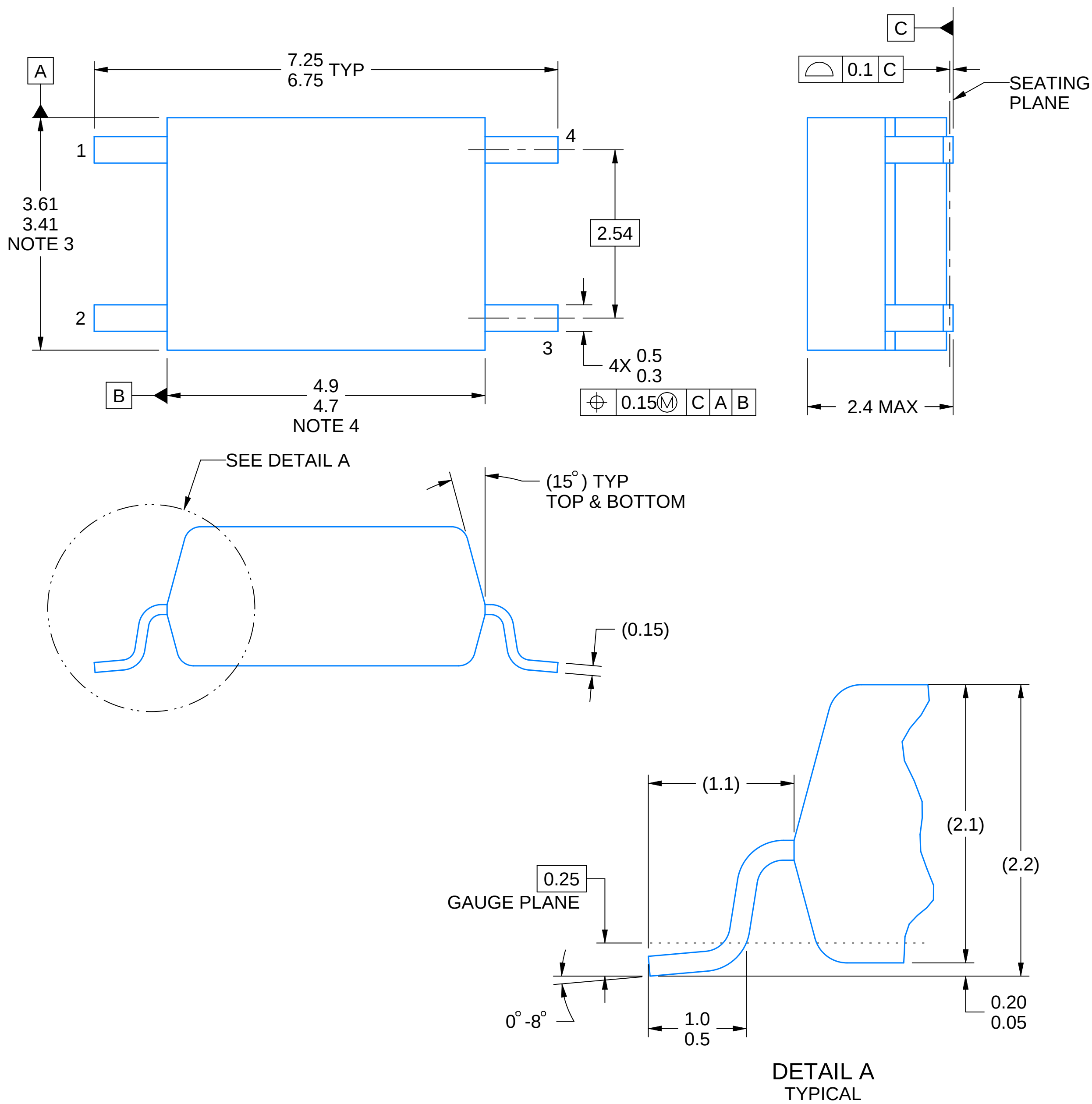
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOM8110DFGR	SOIC	DFG	4	2000	356.0	356.0	35.0

DFG0004A

PACKAGE OUTLINE

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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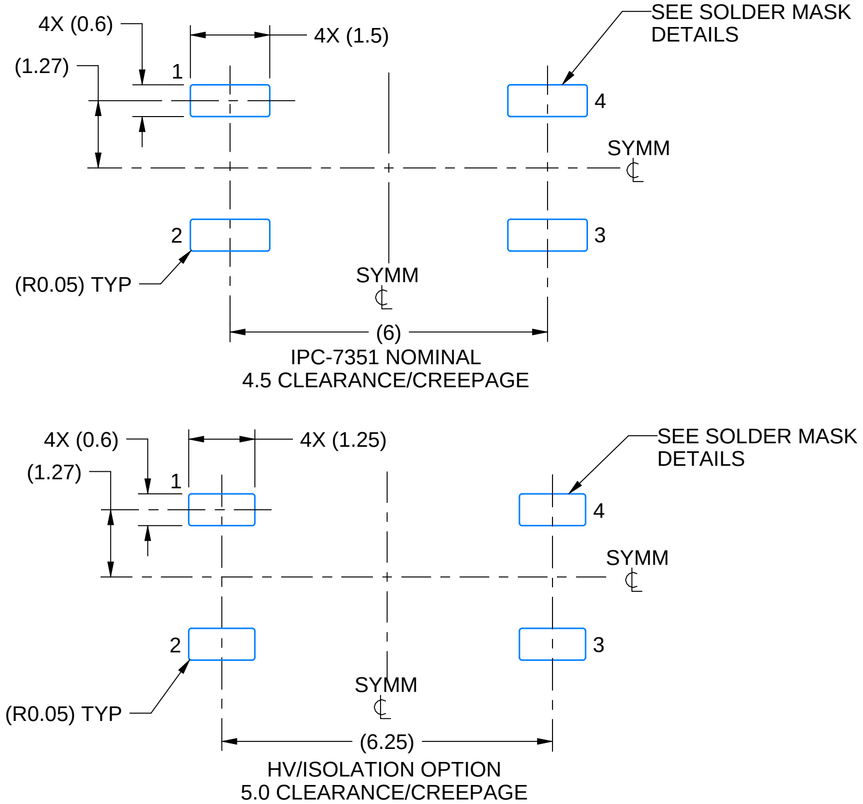
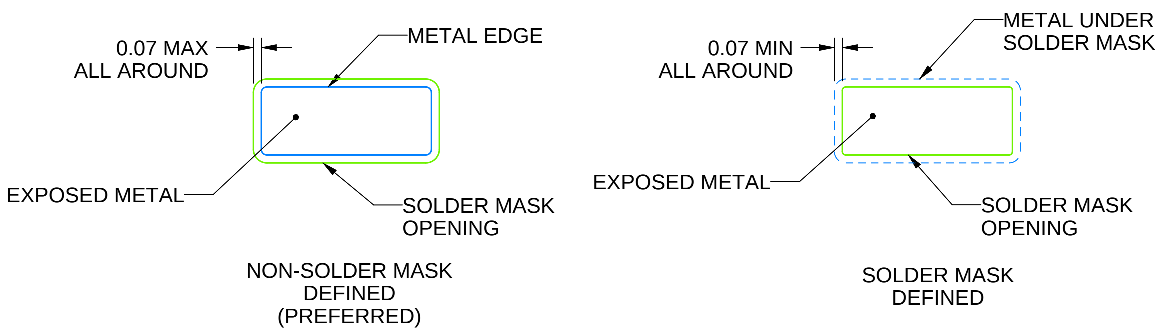
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X



SOLDER MASK DETAILS

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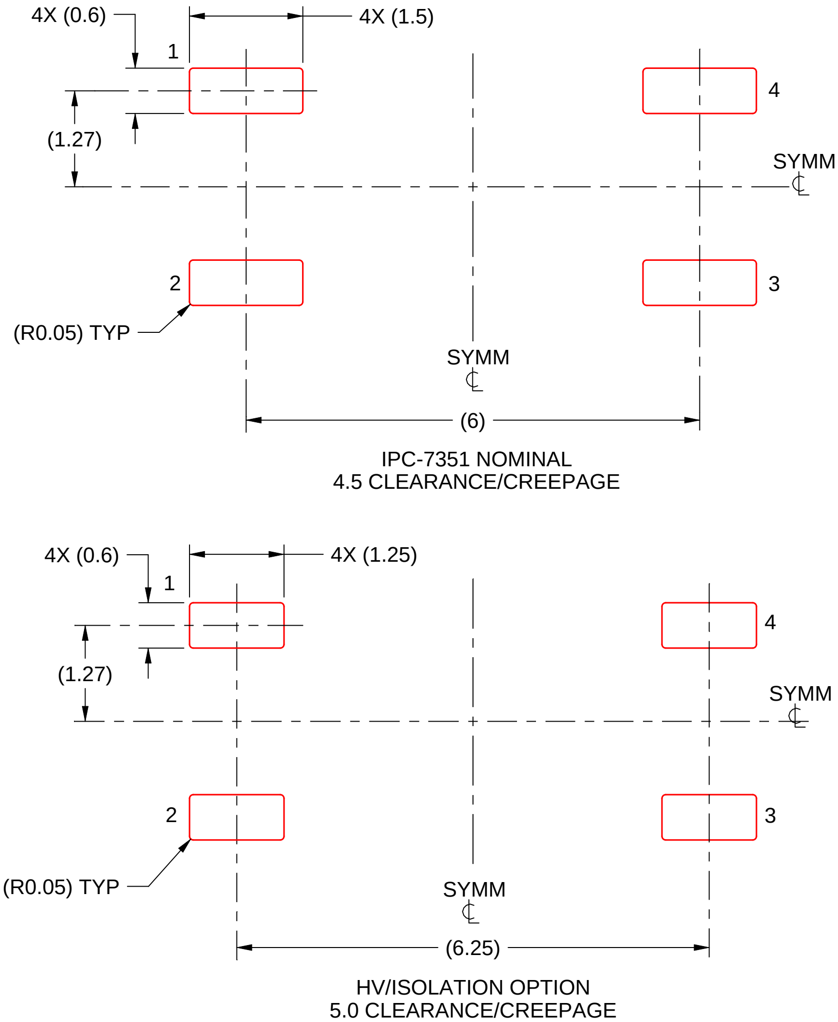
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.