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Telephony Chipset for CPE

DXS Series

DXS101 (PEF32001VSV12, PEF32001VSV13)

Data Sheet

MaxLinear Confidential

Revision 2.0, 2022-03-11
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Revision History

Current:	**Revision 2.0, 2022-03-11**
Previous:	**Revision 1.2, 2017-10-24**
Page	**Major changes since previous revision**
All	This document was rebranded from Intel to MaxLinear, including the logo and Legal Notice page. All product names were rebranded by removing Intel® from their names.
All	Added the DXS101 (PEF32001VSV13) device.
25	**Section 4.1.2 Timing SPI Interface**: Removed t_{DCLKh} and added t_{DCLKl} in **Figure 8** and **Table 15**.
33	**Table 23 Absolute Maximum Ratings**: Added the **Digital input and output pin pad supply voltage 1.8 V** parameter.
36	Updated **Schmitt Trigger Input Levels** in **Figure 14** and **Table 28**.
67	Added **Section 9 Chip Identification and Ordering Information**.
68	Updated **Literature References**.

Table of Contents

List of Figures

List of Tables

Preface

This data sheet describes the hardware features of the DXS101 device in a PG-VQFN-44 package. This device is a member of MaxLinear's Telephony Chipset for CPE, DXS Series.

Use this document alongside the other DXS Series documents listed in the **Literature References**.

To simplify matters, the following synonyms are used:

DXS

Synonym used for these devices belonging to MaxLinear's Telephony Chipset for CPE, DXS Series.

- DXS101 (PEF32001VSV12, PEF32001VSV13)

SLIC

Synonym used for the SLIC-part of the DXS101 device.

Organization of this Document

This document is organized as follows:

- **Chapter 1**, **Introduction**
  A general description including key features/requirements and typical applications.
- **Chapter 2**, **Pin Description**
  Pin layout and pin description.
- **Chapter 3**, **Hardware Behavior and Handling**
  Description of clocking, reset behavior and test modes.
- **Chapter 4**, **Interface Description**
  Serial, PCM, CSI and GPIO interfaces.
- **Chapter 5**, **Electrical and Transmission Characteristics**
  Transmission performance, operating conditions and characteristics, limit values.
- **Chapter 6**, **Application Circuit**
  External components required for typical applications.
- **Chapter 7**, **Hardware Design Guidelines**
  Layout recommendations and design guidelines for board design.
- **Chapter 8**, **Package Outlines**
  Illustrations and dimensions of the package outlines.
- **Literature References** and **Standards References**

1 Introduction

MaxLinear's DXS101 combines a single-channel analog codec and a high-voltage SLIC in a single package of type PG-VQFN-44 (described in this data sheet), or PG-VQFN-68 (refer to [4]).

The device is optimized for Customer Premises Equipment (CPE) and for Small and Medium-sized Enterprise (SME) applications.

The DXS101 implements a single-channel telephone line interface to provide all the necessary voice interface functions between the subscriber line and the PCM/SPI interface. The DXS101 is a single-package line-interface solution with a reduced footprint.

A high-accuracy DC design, as well as patented ring current regulation and ring voltage generation serve to reduce the power consumption of DXS Series devices to among the best values available on the market. The relevant quasi-balanced ringing feature is described in detail in the DXS System Description [3].

All the relevant parameters are programmable via software. This allows hardware designs based on the DXS Series devices to serve evolving worldwide standards without requiring changes to the PCB design.

Building on MaxLinear's proven technological expertise, DXS101 simplifies the design of VoIP-enabled devices, while reducing development time and effort as well as the overall bill of materials (BOM).

A system package is provided by combining the chip with MaxLinear's DXS Device Driver. **Chapter 1.1** provides an overview of the supported features.

1.1 DXS101 Features

- Fully programmable codec and SLIC system solution with enhanced signal processing capabilities and integrated 1.5 V regulator
- Minimized external component count to allow high board density designs
- Low Bill of Materials (BoM)
- Green package - RoHS 6 compliant

1.1.1 Codec/SLIC

- AC transmission performance parameters programmable according to ITU-T Q.552 for worldwide use (country-specific programming for parameters such as AC impedance matching, hybrid balance, transmit and receive gain, frequency response) according to ITU-T Q.552
- Integrated balanced and unbalanced ringing capability - software programmable up to 144 V peak ringing voltage (depending on external components), frequency range between 15 and 50 Hz, crest factor programmable
- Loop start signaling
- Ground start signaling
- Ground key indication
- Polarity reversal
- DC Ring Trip Detection
- AC Ring Trip Detection
- Fast Ring Trip Detection
- Ringing with DC offset
- Automatic ring current regulation
- Support for message waiting indication with glow lamp
- On-hook transmission
- PCM Interface G.711 A-law/µ-law or 16-bit linear
- Wideband support (16 kHz, 16-bit linear)
- CID type 1, 2 transmission support

1.1.2 Test and Measurement

- Integrated test and diagnostic functions for local loop monitoring according to GR-909
- 3-element resistance and capacitance measurements
- Test for detection of connected phones
- Calibration state to increase the measurement accuracy
- PCM loop-back mode
- AC level meter

1.1.3 Signaling

- Two integrated programmable tone generators, for test and DTMF tone generation
- Integrated CID FSK generator with high level framing support for ITU-T V.23, Bell 202
- Integrated metering pulse generation
- Integrated ringing generator with programmable amplitude, DC offset and crest factor
- DTMF receiver
- Universal Tone Detector (UTD)
- Boosted AC level for howler tone

1.1.4 Driver/API

- DXS Library available for Linux*
- DXS API **[2]**

1.1.5 Host Interface

- Serial peripheral interface (SPI), compatible with the Motorola SPI and the MaxLinear SCI
- Combined Serial Interface (CSI)

1.1.6 Miscellaneous

- Integrated 1.5 V regulator (see **Chapter 3.2.1**)
- DC/DC controller (pulse width modulator)
- Minimized power dissipation by regulating the required line feeding voltage
- Message waiting indication with glow lamp
- Low power standby mode with off-hook detection capability
- On-chip PLL

1.2 Logic Symbol

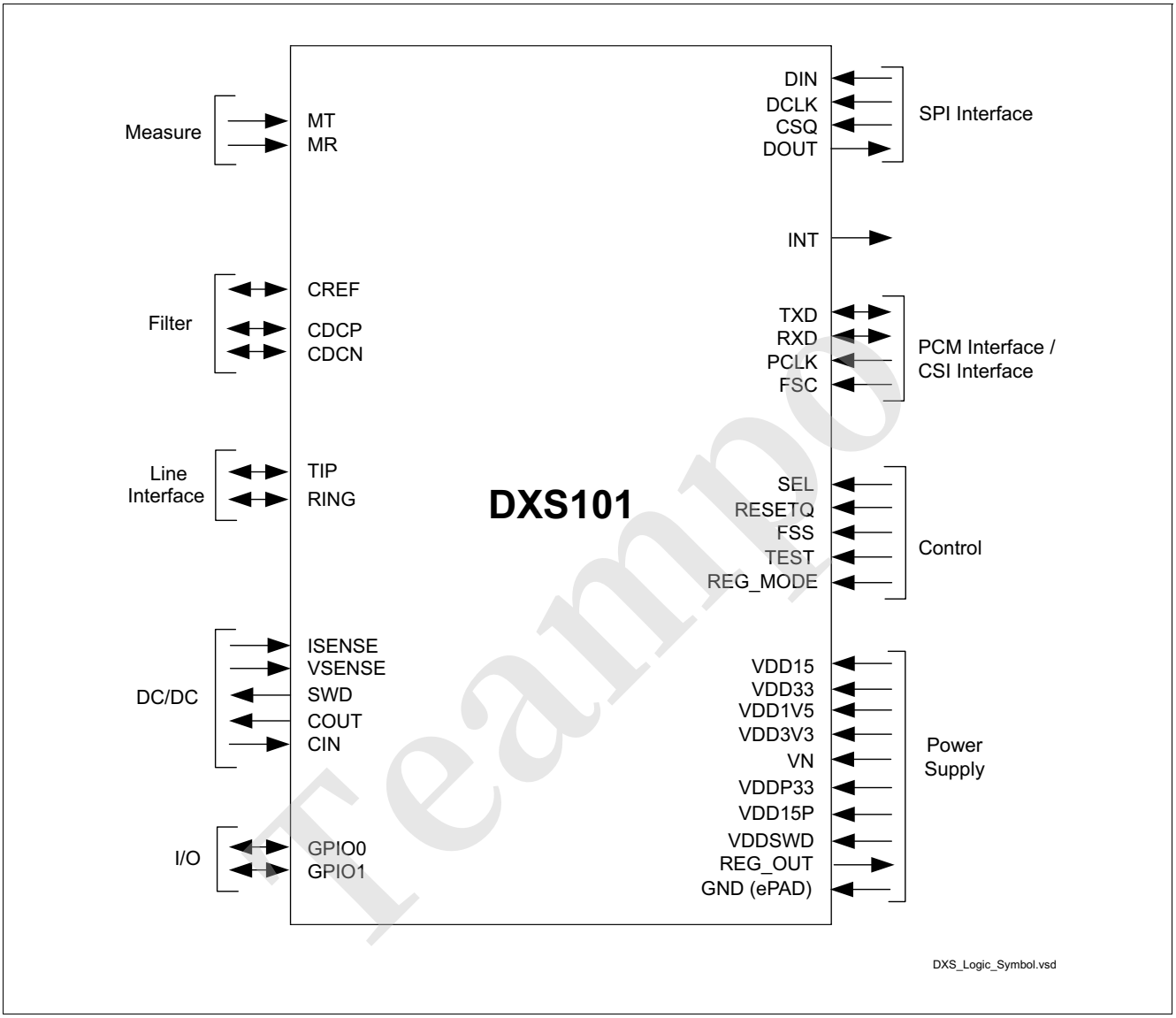


Figure 1 Logic Symbol for DXS101 (PG-VQFN-44)

2 Pin Description

2.1 Abbreviations

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Input. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal. Digital levels.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	I/O is a bidirectional input/output signal. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
PU	Pull-up
OD	Open-Drain. The corresponding pin has two operational states: active low and tristate. This allows the implementation of a wired-OR connection used by multiple devices. An external pull-up is required to sustain the inactive state until another agent drives it. This must be provided by the central resource.
TS	Tristate capability: The corresponding pin has 3 operational states: low, high and high-impedance.
PP	Push-Pull. The corresponding pin has 2 operational states: active low and active high (identical to output with no type attribute).

2.2 Pin Description for DXS101 (PG-VQFN-44)

2.2.1 Pin Diagram for DXS101 (PG-VQFN-44)

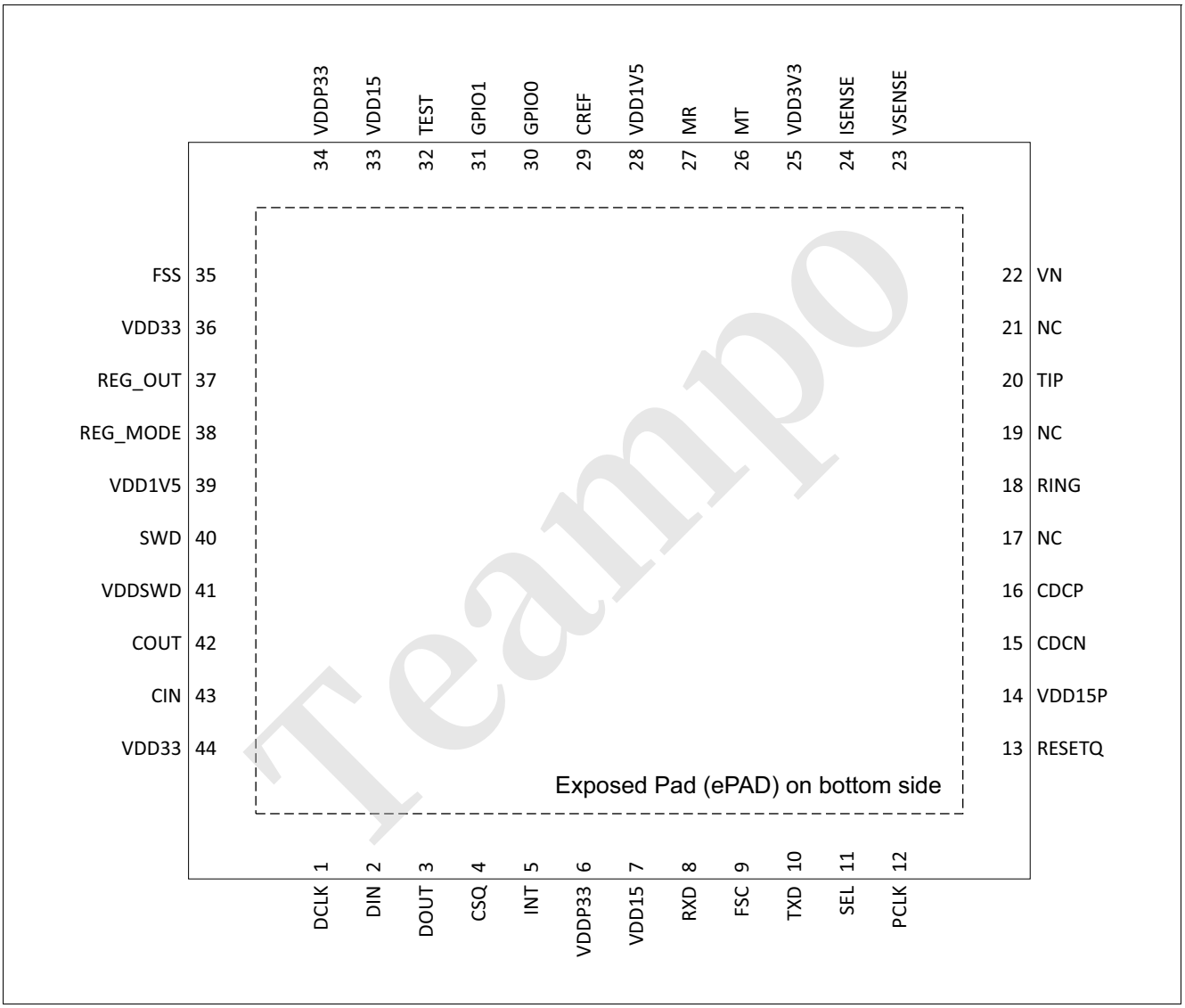


Figure 2 Pin Diagram for DXS101 in PG-VQFN-44 (Top View)

Note: Ground GND of the device is available on the exposed pad (ePAD) and must be electrically connected to PCB ground.

2.2.2 Power and Ground Pins

Ground GND of the device is available on the exposed pad (ePAD) and must be electrically connected to the PCB ground.

Table 3 Exposed Pad (ePAD)

Pin No.	Name	Pin Type	Buffer Type	Function
–	–	GND	–	**Ground**

Table 4 Power Pins

Pin No.	Name	Pin Type	Buffer Type	Function
28, 39	VDD1V5	PWR	–	**+1.5 V Analog Supply Voltage**
25	VDD3V3	PWR	–	**+3.3 V Analog Supply Voltage**
36, 44	VDD33	PWR	–	**+3.3 V Digital Supply Voltage for DC/DC Converter**
6, 34	VDDP33	PWR	–	**Pad Supply Voltage** Typically 3.3 V, but 2.5 V or 1.8 V are also possible.
37	REG_OUT	PWR	–	**Output of +1.5 V Regulator**
7, 33	VDD15	PWR	–	**+1.5 V Digital Supply Voltage**
14	VDD15P	PWR	–	**+1.5 V Supply Voltage for PLL**
41	VDDSWD	PWR	–	**Positive Supply for SWD Pin/Charge Pump Output**
22	VN	PWR	–	**Regulated Negative SLIC Battery Voltage**

2.2.3 Reference and Reset Pins

Table 5 Reference and Reset Pins

Pin No.	Name	Pin Type	Buffer Type	Function
29	CREF	AI/O	–	**External Filter Capacitor** 220 nF
13	RESETQ	I	–	**Chip Reset** Active low
38	REG_MODE	I	–	**1.5 V Supply Select** • External 1.5 V supply: Leave open • Internal 1.5 V supply: Connect via 1.5 Ω resistor or 3.3 µH coil directly to VDD1V5 (pin 39), see **Chapter 3.2.1**.
35	FSS	PWR	–	**Production Test** Connect to GND
32	TEST	I	–	**Production Test** Connect to GND

2.2.4 Host Interface Pins

When the PCM/SPI interface is selected via pin SEL, the PCM and SPI interface functions are on separate Host Interface pins. When the CSI interface is selected, the PCM interface and CSI interface functions are multiplexed on four of the Host Interface pins: TXD, RXD, PCLK and FSC as summarized in **Table 6**.

Table 6 Host Interface Pins

Pin No.	Name	Pin Type	Buffer Type	Function
11	SEL	I	–	**Select Interface** Connect to GND for **PCM/SPI** interface Connect to VDDP33 for **CSI** interface
10	TXD	I/O	OD	**PCM Data Transmit / CSI Output** **PCM/SPI**: Output PCM highway **CSI**: CSI data output, status of interrupt pin INT
8	RXD	I/O	OD	**PCM Data Receive / CSI Input** **PCM/SPI:** Input PCM highway **CSI:** CSI data input
12	PCLK	I	–	**PCM Data Clock / CSI Clock** **PCM/SPI:** PCM data clock, reference clock for PLL **CSI:** CSI data clock, reference clock for PLL
9	FSC	I	–	**PCM Frame Synchronization and SPI Chip Select** **PCM/SPI:** PCM frame synchronization 8 kHz **CSI:** PCM frame synchronization 8 kHz and SPI chip select status
4	CSQ	I	–	**SPI Chip Select** Chip select, active low When the CSI interface is selected, connect to GND.
3	DOUT	O	TS	**SPI Data Out** When the CSI interface is selected, leave unconnected.
2	DIN	I	–	**SPI Data In** When the CSI interface is selected, connect to GND.
1	DCLK	I	–	**SPI Data Clock** When the CSI interface is selected, connect to GND.
5	INT	O	OD	**Interrupt**

2.2.5 Analog Test, Filter and Gain Pins

Table 7 Analog Test, Filter and Gain Pins

Pin No.	Name	Pin Type	Buffer Type	Function
16	CDCP	AI/O	–	**DC Voltage Filter** External capacitance for DC voltage filtering
15	CDCN	AI/O	–	**DC Voltage Filter** External capacitance for DC voltage filtering
26	MT	AI	–	**Measurement, Tip** Input for measurement and testing from Tip
27	MR	AI	–	**Measurement, Ring** Input for measurement and testing from Ring

2.2.6 Subscriber Interface Pins

Table 8 Subscriber Interface Pins

Pin No.	Name	Pin Type	Buffer Type	Function
20	TIP	AI/O	–	**Tip** Subscriber loop connection, Tip
18	RING	AI/O	–	**Ring** Subscriber loop connection, Ring

2.2.7 DC/DC Control Pins

Table 9 DC/DC Control Pins

Pin No.	Name	Pin Type	Buffer Type	Function
24	ISENSE	AI	–	**Current Sense Input** Sense pin for limitation of switch transistor current
23	VSENSE	AI	–	**Voltage Sense Input** Sense pin for DC/DC converter output voltage
40	SWD	O	PP	**Switching Driver Output** Switching transistor driver output
42	COUT	AO	–	**Connection for Charge Pump Capacitor**
43	CIN	AI	–	**Connection for Charge Pump Capacitor**

2.2.8 General Purpose IO Pins

Table 10 General Purpose IO Pins

Pin No.	Name	Pin Type	Buffer Type	Function
30	GPIO0	I/O	PP	**General Purpose I/O** Used as a DC/DC converter output pin in the case of a Buck-or-Boost Converter for -48 V (BB48).
31	GPIO1	I/O	PP	**General Purpose I/O**

2.2.9 Not Connected Pins

Table 11 Not Connected Pins

Pin No.	Name	Pin Type	Buffer Type	Function
17, 19, 21	NC	NC	–	**Do Not Connect**

3 Hardware Behavior and Handling

3.1 Operating Modes

Table 12 provides a brief overview of the DXS operating modes. Refer to the DXS System Description [3] for a full description of the modes listed here, and for more information on the additional modes provided by the DXS, such as those relevant to line testing, calibration and ground start.

Table 12 Operating Modes Description

Operating Mode	Description
DISABLED	The DXS Series device is disconnected from the phone line (impedance ~250 kΩ). DC/DC converter is switched off.
STANDBY	Low power mode. DC feeding is active and hook detection is active. No AC transmission is possible. Overtemperature detection and clock-fail detection is active.
ACTIVE	Voice transmission and on/off-hook detection as well as line monitoring possible. DC line feeding with programmed DC characteristic.
RINGING	Generation of high-voltage ring signal using patented supply voltage tracking concept.

3.1.1 Sleep State

When the channel is in STANDBY or DISABLED mode and the mailboxes are empty, the DXS Series device automatically switches to the sleep state (lowest possible power consumption), when this feature has previously been enabled via the API. In this case, the DXS internal system clock is switched off, and only the DC/DC converter control is clocked. A wakeup out of the sleep state is triggered when the subscriber goes off-hook, or when the DXS is accessed via a command on the SPI interface.

3.2 Hardware Behavior and Handling

3.2.1 1.5 V Regulation

The DXS Series device is either operated using an external 1.5 V supply, or by taking advantage of its integrated 1.5 V regulator in systems where a 1.5 V supply is not available. When an external 1.5 V supply is used, the REG_MODE pin must be left open, allowing the device to be supplied from this external 1.5 V source (see **Figure 3** a)).

When the integrated 1.5 V regulator is used, it is run in either linear mode or step-down (buck) mode depending on these requirements:

- For lowest cost applications, select linear mode by connecting the REG_MODE pin to GND. Add a 1.5 Ω resistor between REG_OUT and VDD15 (see **Figure 3** b)). The regulator operates as an LDO.
- When the lowest possible power dissipation is desired, connect the REG_MODE pin to VDD3V3 and place a coil of approx. 3.3 µH between REG_OUT and VDD15 (see **Figure 3** c)). The regulator operates in step-down mode with an efficiency of approx. 80%.

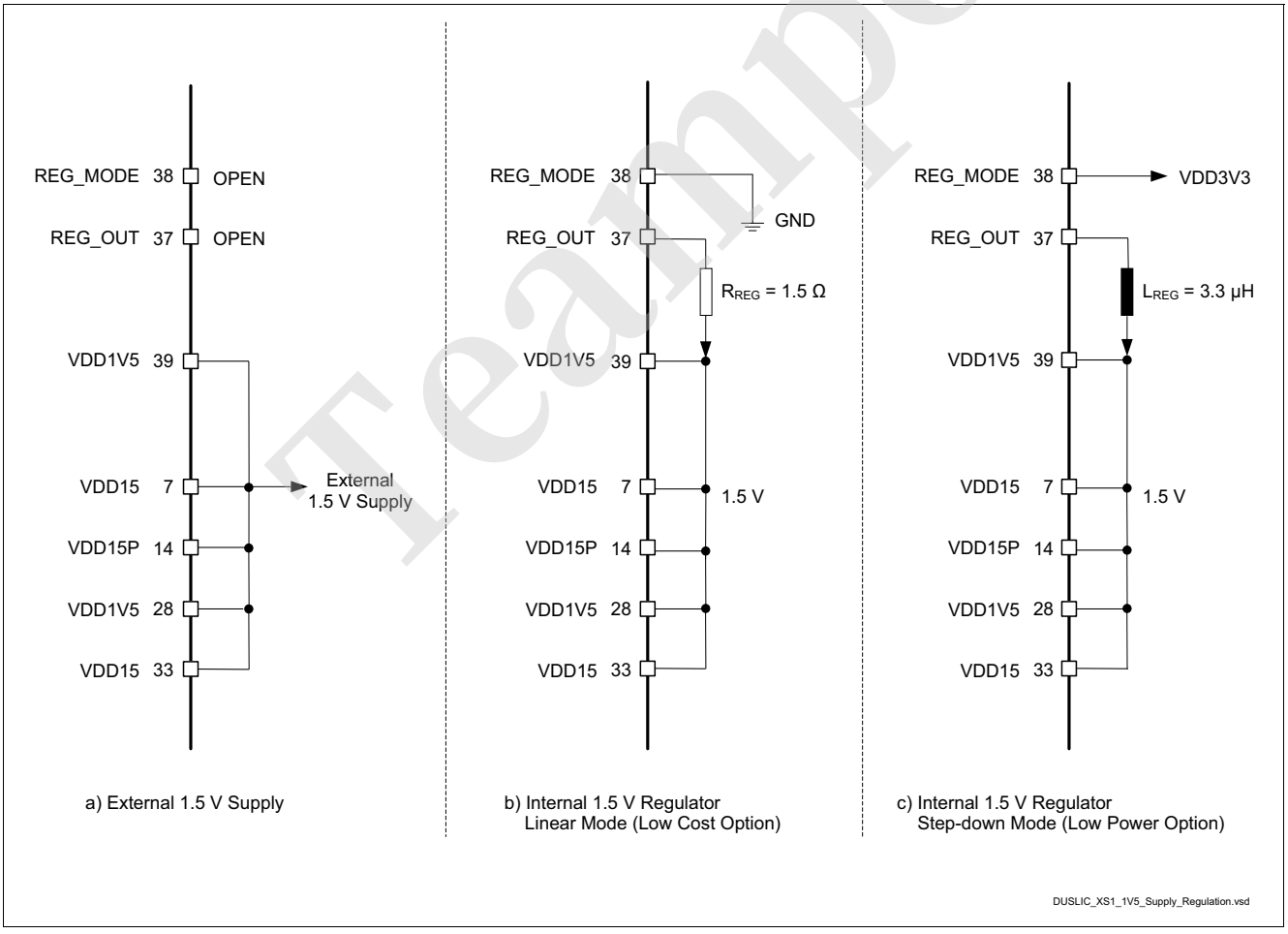


Figure 3 1.5 V Supply Regulation

3.2.2 Clocking and Clock Fail Handling

The DXS Series device requires these clocks: frame synchronization clock (FSC) and PCM interface clock (PCLK).

The PCLK and FSC clock signals must fulfill the timing specification described in **Chapter 4.2**. The jitter phase noise requirements for specified analog performance are given in **Figure 4**. PCLK must be phase-locked to FSC. The supported PCLK frequencies of the device are listed in **Table 17**. The PCLK and FSC clocks must be provided at all times to ensure correct operation of the device and the clock signal frequencies must not be changed on the fly.

If the PCLK clock fails, which corresponds to a PLL unlock (see **Figure 5**), correct operation is no longer guaranteed and correct operation of the SPI interface is not ensured. A Clock Fail event is put into the command outbox and the channel is set to Emergency Shutdown (ESD) mode (refer to **[3]**). Moreover, the readout of the mailbox may fail especially for high frequency SPI access (see **Table 15** for more details). A hardware reset is required to safely recover from such a clock fail situation.

Nevertheless, in the case of Clock Fail events (for example, due to a scheduled CPE software update), it is possible to disable the automatic switching to ESD mode via the DXS API. This prevents DC feeding voltage drops during the software update phase, which may take several seconds to be completed. Such voltage drops are not acceptable in certain situations, for example where alarm systems are connected to the subscriber loop.

Table 13 Clocks

Pin	Description	Frequency
FSC	Frame synchronization clock (mandatory). Synchronizes internal clocks and voice interface.	f_{FSC} = 8 kHz
PCLK (PCM)	Clock for voice interface (mandatory). Only multiples of 512 kHz are allowed. This clock is also used for the internal PLL.	64*f_{FSC} to 1024*f_{FSC} in steps of 64*f_{FSC} depending on the number of time slots (see **Table 17**).

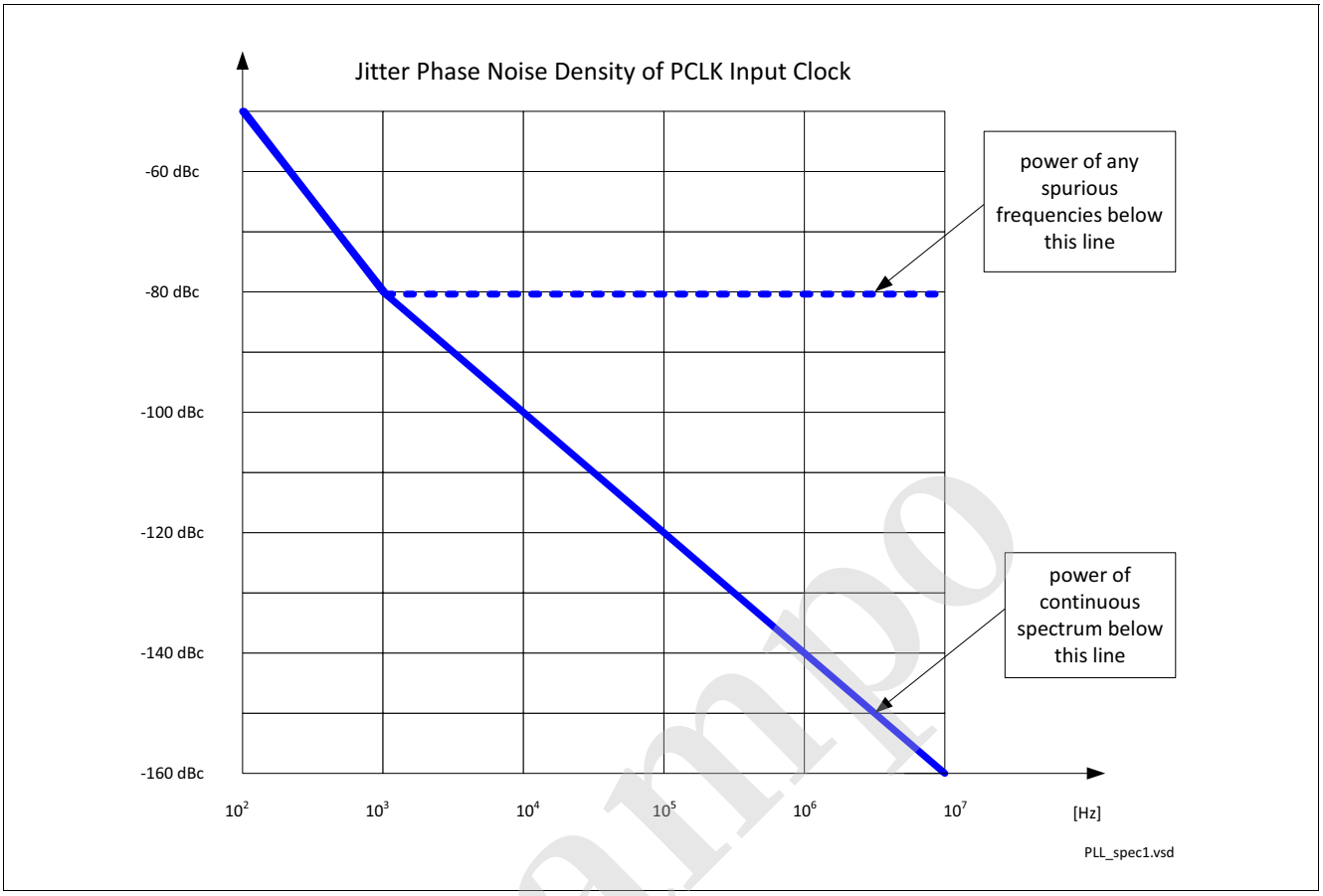


Figure 4 PCLK Jitter Phase Noise Requirements

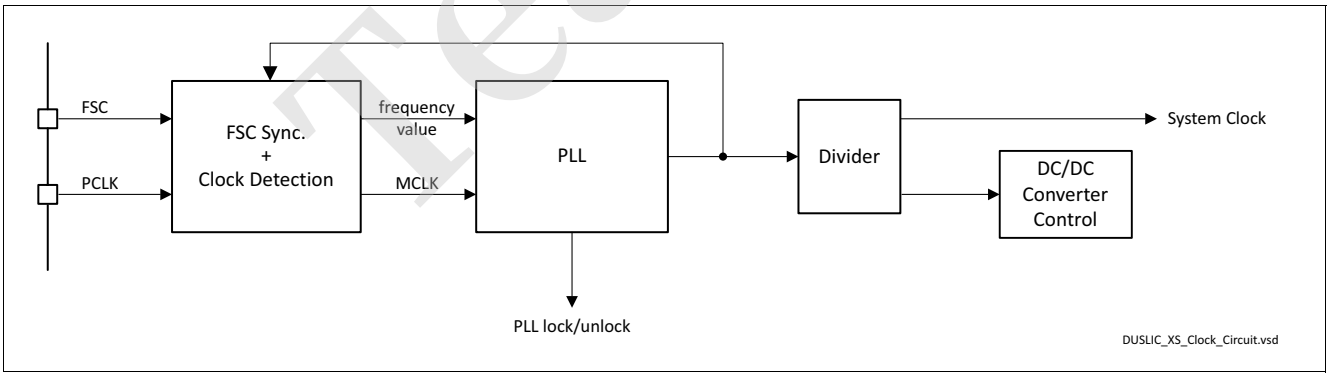


Figure 5 Clock Fail Indication

3.2.3 Reset

To perform a hardware reset of the DXS Series device, the signal on the RESETQ input pin must be set to low for at least 20 µs (t_{res} ≥ 20 µs). RESETQ has a spike rejection function that safely suppresses spikes with a duration of less than 2 µs (t_{rej} ≤ 2 µs).

Pulling the RESETQ input pin low resets the chip (see **Figure 6**) and causes the following actions to be performed:

- All I/O pins are deactivated (tristate high impedance).
- All outputs are inactive.
- Internal PLL is stopped.
- DC/DC converter switch control (SWDx) is deactivated.
- Internal clocks are deactivated.
- The chip is in a Reset State.

With the rising edge of the reset signal, the external clocks (FSC, PCLK) must already be stable. Changing the clock frequency without a reset is not allowed. Then the following actions are performed:

- Clock detection.
- PLL synchronization.
- Activation of reset routine: the internal reset routine requires approximately 2 ms to complete (including PLL start up and clock synchronization).
- When the reset routine is finished, a boot finished event is generated, the line is in the DISABLED state and the DXS Series device is accessible for the first time.

Figure 6 shows the reset sequence for the hardware reset caused by a signal on the RESETQ pin.

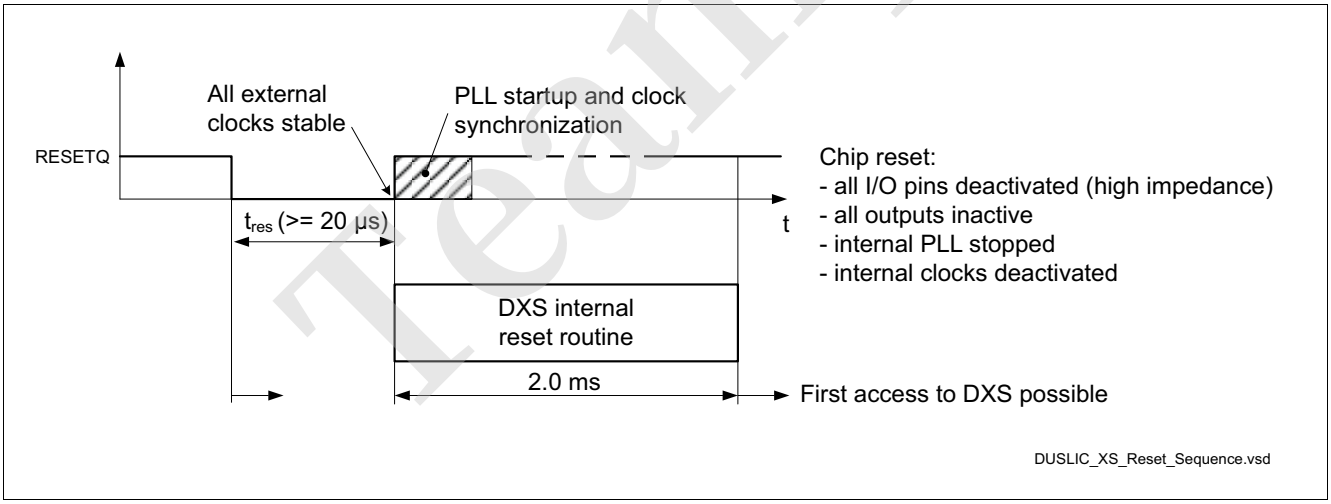


Figure 6 DXS Reset Sequence

4 Interface Description

To program the DXS Series device and perform data transfers from/to the DXS, a serial microcontroller interface and PCM interface are used, or alternatively a Combined Serial Interface (CSI) is used.

Serial Microcontroller Interface

- The serial peripheral interface (SPI) is compatible with the Motorola SPI and the MaxLinear SCI.

PCM Interface

- The DXS Series device has one PCM interface providing a single external PCM highway, which allows concurrent operation with the serial microcontroller interface.

Combined Serial Interface (CSI)

- It is possible to use the Combined Serial Interface instead of the separate PCM and SPI interfaces. It combines the communication of voice data and control information in one serial interface, and allows the SPI and PCM interface functions to be multiplexed on the same pins.

GPIO Interface

- The DXS Series device provides two configurable IO pins (GPIO0, GPIO1) for general use[1]. The DXS API provides a programming interface to configure, control and read the GPIO pins (see [2]).

Input/Output Waveform for AC Interface Timing Characteristics

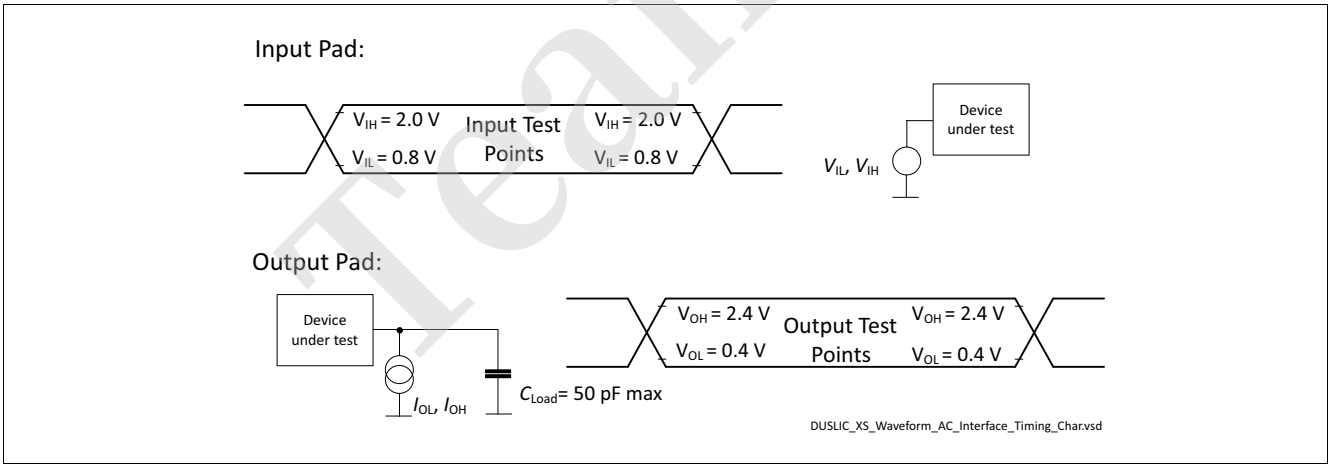


Figure 7 Waveform for AC Tests

During AC testing the CMOS inputs are driven at a low level of 0.8 V and a high level of 2.0 V, see Figure 7. The CMOS outputs are measured at 0.4 V and 2.4 V respectively.

1) When the Buck-or-Boost DC/DC Converter for -48 V (BB48) is used, the GPIO0 pin is reserved for driving the switching transistor.

4.1 SPI Interface

The serial peripheral interface of the DXS Series device represents one of the SPI interface modes of the Motorola* PowerQUICC* family (SPI slave mode). The data are serialized with the MSB first.

Note: The DXS always operates as a slave device.

4.1.1 Signal Description for SPI Interface

Table 14 SPI Interface Signals

Signal Name	Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
CSQ	CSQ	I	–	Chip select signal starting a read or write access to DXS.
DCLK	DCLK	I	–	Data clock supplied to DXS.
DIN	DIN	I	–	Data input carries data from the master device to the DXS.
DOUT	DOUT	O	TS	Data output carries data from the DXS to a master device.

1) For an explanation of the abbreviations see **Table 1**.
2) For an explanation of the abbreviations see **Table 2**.

The transfer characteristics for the input pins are described in **Chapter 5.3.3 Schmitt Trigger Input Levels**.

4.1.2 Timing SPI Interface

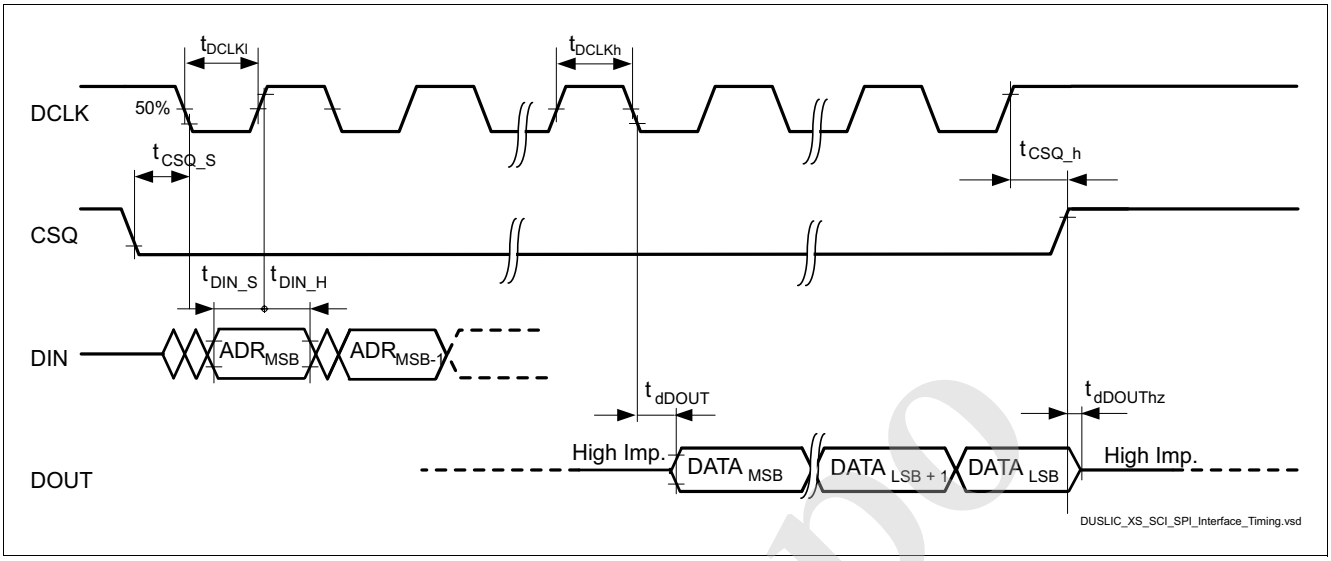


Figure 8 SPI Interface Timing

Note:

1. *The data clock DCLK may only be applied during data transfer.*
2. *3-wire signaling is also supported. DIN and DOUT may be connected together.*

Table 15 Timing Values for SPI Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DCLK high time	t_{DCLKh}	49	–	–	ns	–
		200	–	–	ns	Clock fail[1)]
DCLK low time	t_{DCLKl}	49	–	–	ns	–
		200	–	–	ns	Clock fail[1)]
CSQ setup time	t_{CSQ_s}	5	–	–	ns	–
CSQ hold time	t_{CSQ_h}	15	–	–	ns	–
DIN setup time[2)]	t_{DIN_s}	5	–	–	ns	–
DIN hold time[2)]	t_{DIN_h}	5	–	–	ns	–
DOUT delay time[3)]	t_{dDOUT}	13	–	17.4 ns + 0.4 [ns/pF] * C_{Load} [pF]	ns	–
DOUT delay time to high Z	$t_{dDOUThz}$	–	–	10	ns	–

1) To access the SPI interface when a PCLK Clock Fail occurs (see **Chapter 3.2.2**), a minimum of 200 ns is required.

2) t_{DIN_s} and t_{DIN_h} minimum values must not be lower than 50% of the clock transition time of DCLK. It must be ensured that the clock transition time of DCLK is <10 nsec.

3) All the delay times consist of two components: an intrinsic time (min. time) caused by internal processing, and a second component caused by external circuitry (C_{Load}).

4.1.3 Logical Access

The DXS Series device uses 32-bit mailboxes for reading and writing commands. However, SPI access in 8-bit mode is also supported in order to be compatible with, for example, MaxLinear's Puma™ chipsets.

32-bit mode: One 16-bit SPI header followed by multiple 32-bit words.

8-bit mode: One 16-bit SPI header followed by one 32-bit word, split into 6 times 8-bit access.

4.2 PCM Interface

The serial PCM interface transfers A-Law or µ-Law compressed voice data. It also transfers linear data, in which case two successive time slots are used. In the 16-bit linear/16 kHz mode, the PCM interface uses four consecutive time slots for data transfer (e.g. time slots 0, 1, 2, 3). It is also possible to configure the interface to use two consecutive time slots for the first 16-bit/16 kHz sample, and after 62.5 µs, the second 16-bit/16 kHz sample is sent using another two consecutive time slots. This results in, for example, occupied time slots 0, 1, 16, and 17.

4.2.1 Signal Description for PCM Interface

Table 16 describes the PCM interface signals.

Table 16 PCM Interface Signals

Signal Name	Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
PCLK	PCLK	I	–	PCM interface data clock.
FSC	FSC	I	–	Frame synchronization for PCM interface and PLL input.
TXD	TXD	O	TS	PCM interface data output.
RXD	RXD	I	TS	Data input for highway 1 of PCM interface.

1) For an explanation of the abbreviations see Table 1

2) For an explanation of the abbreviations see Table 2

Transfer characteristics for input pins are described in **Chapter 5.3.3 Schmitt Trigger Input Levels**.

The FSC pulse identifies the beginning of a receive or transmit frame for the highway (see **Figure 9**). The PCLK clock signal synchronizes the data transfer on the TXD and RXD lines. In each active time slot, bytes are serialized with the MSB first. As a default setting, the rising edge indicates the start of the bit, while the falling edge latches the contents of the received data on RXD. When double-clock rate is selected (PCLK clock rate is twice the data rate), the first rising edge indicates the start of a bit, while, by default, the second falling edge latches the contents of the data line RXD.

The DXS allows for flexible programming of the PCM interface. For more information, see **Chapter 4.2.1.1**.

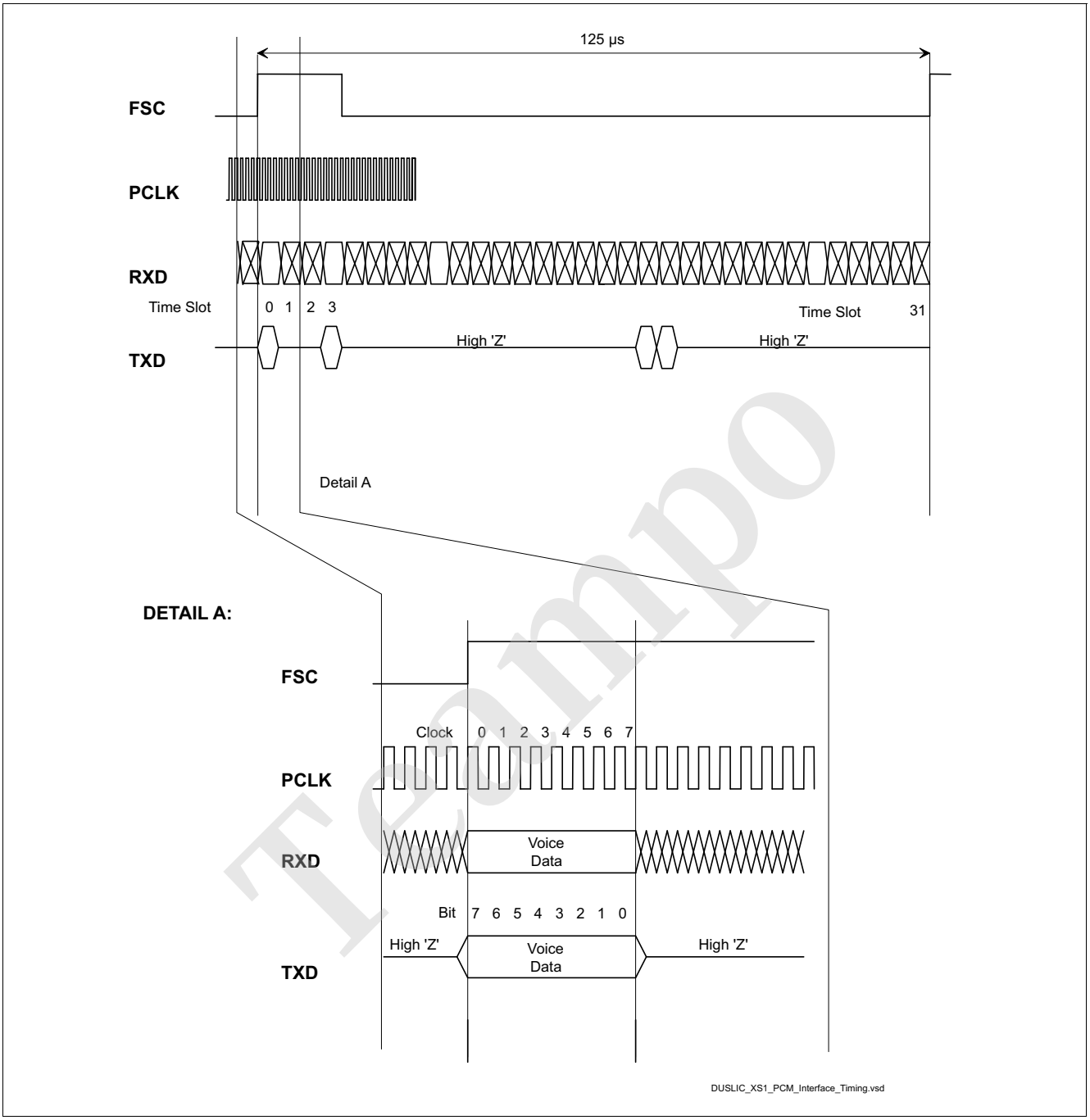


Figure 9 General PCM Interface Timing

The data rate of the interface varies from 256 kbit/s to 8192 kbit/s. A frame may consist of up to 128 time slots of 8 bits each. The time slot assignment for the channel is programmable. Receive and transmit time slots are also individually programmable.

Table 17 shows PCM interface frequency examples; other frequencies between 512 kHz and 8.192 MHz are also possible, e.g., 1536 kHz. The number of valid time slots is defined by the formulas at the end of **Table 17**.

Table 17 DXS PCM Interface Configuration

Clock Rate PCLK [kHz]	Single/Double Clock [1/2]	Time Slots [per highway]	Data Rate [kbit/s]
512	2	4	256
512	1	8	512
1024	2	8	512
1024	1	16	1024
2048	2	16	1024
2048	1	32	2048
4096	2	32	2048
4096	1	64	4096
8192	2	64	4096
8192	1	128	8192
f = n*64*f_{FSC}, n ∈ [1,16][1)]	1	f/64	f
f = n*64*f_{FSC}, n ∈ [1,16][1)]	2	f/128	f/2

1) n ... integer values, f_{FSC} = 8 kHz

4.2.1.1 PCM Highway

The output of an internal driver is only active (push/pull) in the programmed time slots, otherwise it is in tristate mode. Therefore, both highway signals RXD and TXD need a pull-up resistor to ensure stable signals in the unused time slots.

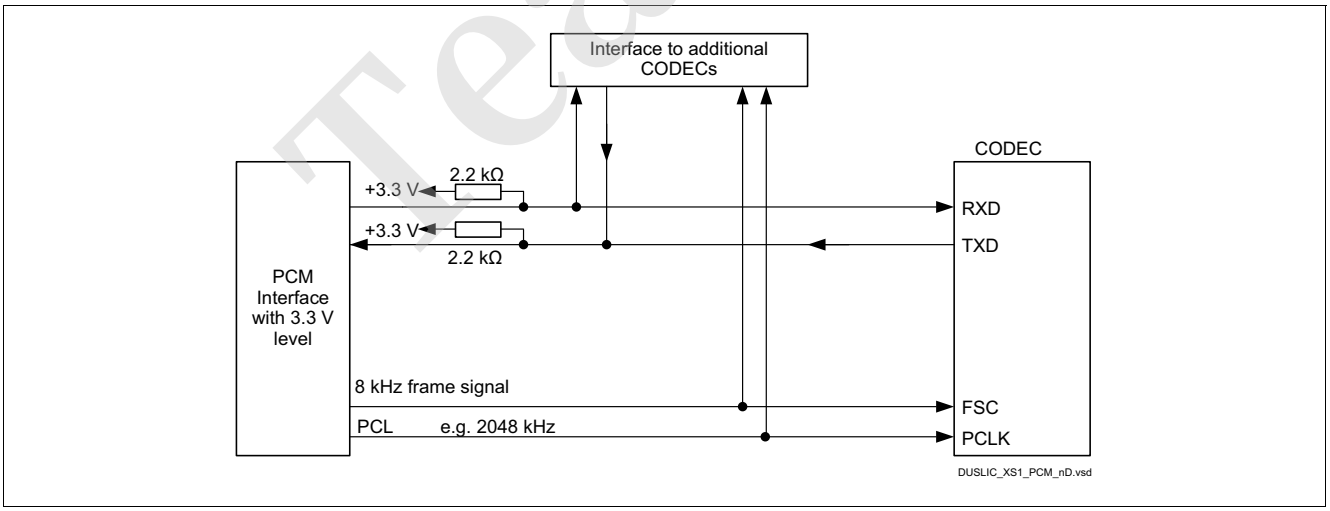


Figure 10 +3.3 V PCM Highway with No Driver

Both the PCM highway output (TXD) and input (RXD) must connected to +3.3 V using 2.2 kΩ pull-up resistors.

4.2.2 Timing PCM Interface

4.2.2.1 Single-Clocking Mode

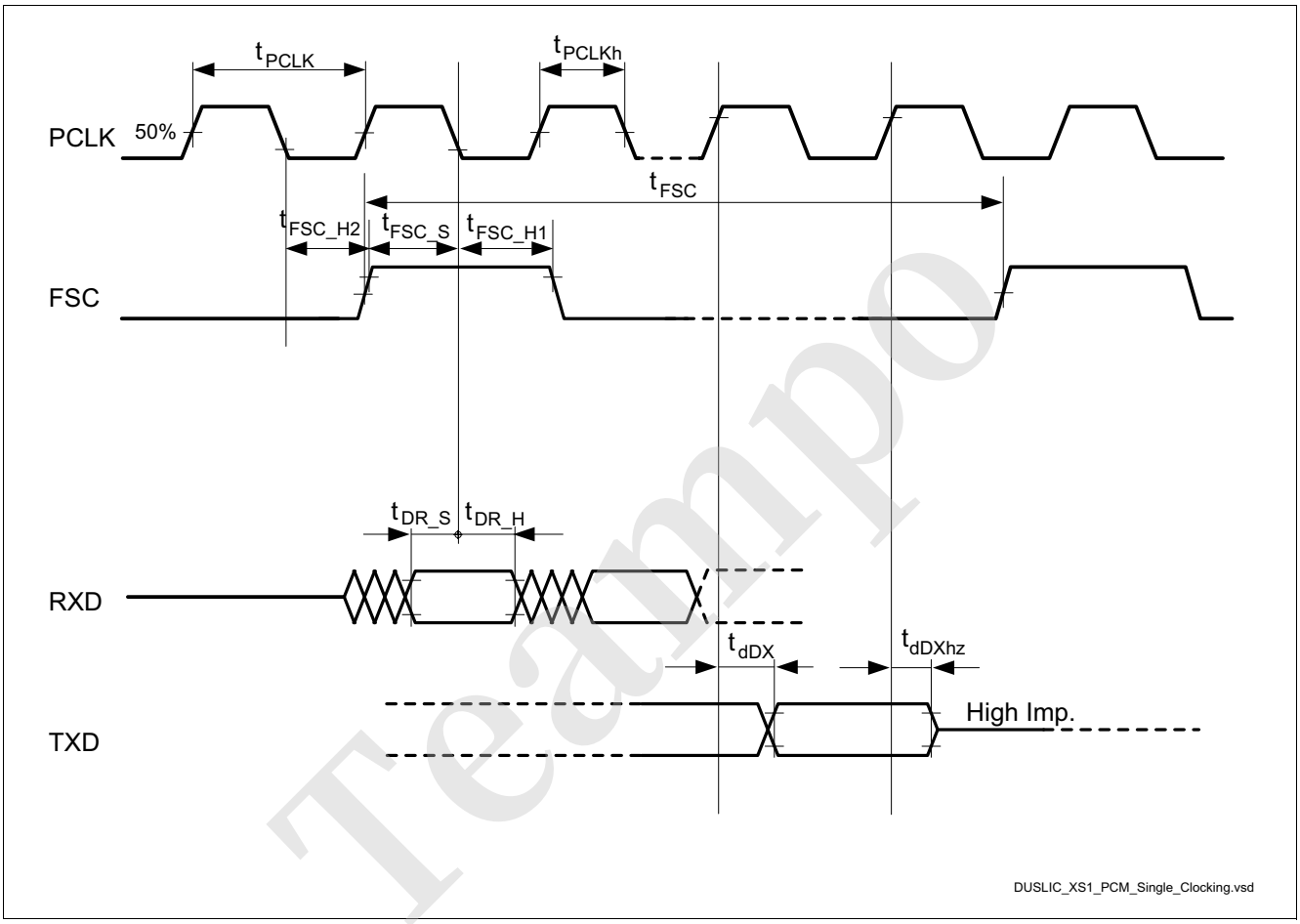


Figure 11 PCM Interface Timing – Single-Clocking Mode

Table 18 Timing Values for PCM Interface (Single-Clocking Mode)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Period PCLK[1)]	t_{PCLK}	1/8192	–	1/512	ms	–
PCLK high time	t_{PCLKh}	0.4 x t_{PCLK}	–	0.6 x t_{PCLK}	ms	–
Period FSC[1)]	t_{FSC}	–	125	–	µs	–
FSC setup time	t_{FSC_S}	10	–	–	ns	–
FSC hold time 1	t_{FSC_H1}	40	–	t_{FSC} - t_{PCLK} - t_{FSC_S}[2)]	ns	–
FSC hold time 2	t_{FSC_H2}	40	–	–	ns	–
RXD setup time	t_{DR_S}	10	–	–	ns	–
FSC jitter time	–	–	–	± 0.2 x t_{PCLK}	ms	–
RXD hold time	t_{DR_H}	10	–	–	ns	–

Table 18 Timing Values for PCM Interface (Single-Clocking Mode) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TXD delay time[3)]	t_{dDX}	0	–	18 + 0.4 [ns/pF] x C_{Load} [pF]	ns	–
TXD delay time to high Z	t_{dDXhz}	–	–	50	ns	–

1) The PCLK frequency must be an integer multiple of the FSC frequency (n*64*f_{FSC}, n = 1..16).
2) This is to ensure that the FSC is low for at least one t_{PCLK} within t_{FSC}.
3) All delay times are made up of two components: an intrinsic time (min-time), caused by internal processing, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

4.2.2.2 Double-Clocking Mode

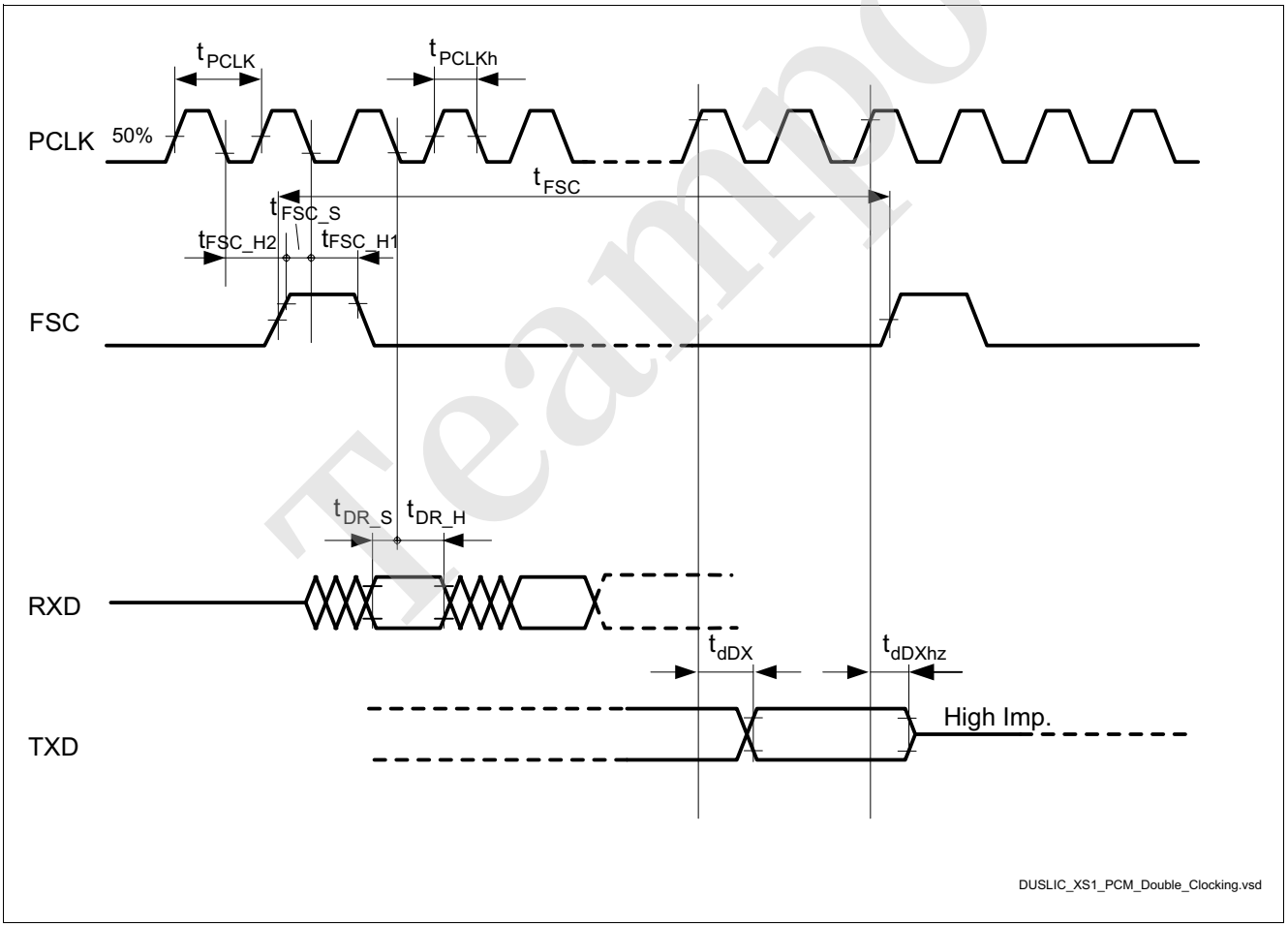


Figure 12 PCM Interface Timing – Double-Clocking Mode

Table 19 Timing Values for PCM Interface (Double-Clocking Mode)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Period PCLK[1)]	t_{PCLK}	1/8192	–	1/512	ms	–
PCLK high time	t_{PCLKh}	0.4 x t_{PCLK}	–	0.6 x t_{PCLK}	ms	–

Table 19 Timing Values for PCM Interface (Double-Clocking Mode) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Period FSC[1)]	t_{FSC}	–	125	–	µs	–
FSC setup time	t_{FSC_S}	10	–	–	ns	–
FSC hold time 1	t_{FSC_H1}	40	–	t_{FSC} - t_{PCLK} - t_{FSC_S}[2)]	ns	–
FSC hold time 2	t_{FSC_H2}	40	–	–	ns	–
FSC jitter time	–	–	–	±0.2 x t_{PCLK}	ms	–
RXD setup time	t_{DR_S}	10	–	–	ns	–
RXD hold time	t_{DR_H}	10	–	–	ns	–
TXD delay time[3)]	t_{dDX}	25	–	t_{dDX_min} + 0.4 [ns/pF] x C_{Load} [pF]	ns	–
TXD delay time to high Z	t_{dDXhz}	–	–	50	ns	–

1) The PCLK frequency must be an integer multiple of the FSC frequency (n*64*f_{FSC}, n = 1..16).
2) This is to ensure that the FSC is low for at least one t_{PCLK} within t_{FSC}.
3) All delay times are made up of two components: an intrinsic time (min-time), caused by internal processing, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

4.3 CSI Interface

The CSI is a combined serial interface that uses one half of the PCLK period to transmit voice data and the other half to transmit control data (see **Figure 13**). The FSC signal is used to indicate both the frame-synchronization signal and a signal showing when control data is valid, similar to the chip select signal. The voice transmission during one half of the PCLK period is fully compatible with the PCM interface.

4.3.1 Signal Description for CSI Interface

Table 20 CSI Interface Signals

Signal Name	Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
PCLK	PCLK	I	–	CSI data clock, reference clock for PLL.
FSC	FSC	I	–	PCM frame synchronization 8 kHz and chip select status.
TXD	TXD	I/O	OD	CSI data output, status of interrupt pin INT.
RXD	RXD	O	OD	CSI data input

1) For an explanation of the abbreviations see **Table 1**.
2) For an explanation of the abbreviations see **Table 2**.

Transfer characteristics for input pins are described in **Chapter 5.3.3 Schmitt Trigger Input Levels**.

4.3.2 Timing CSI Interface

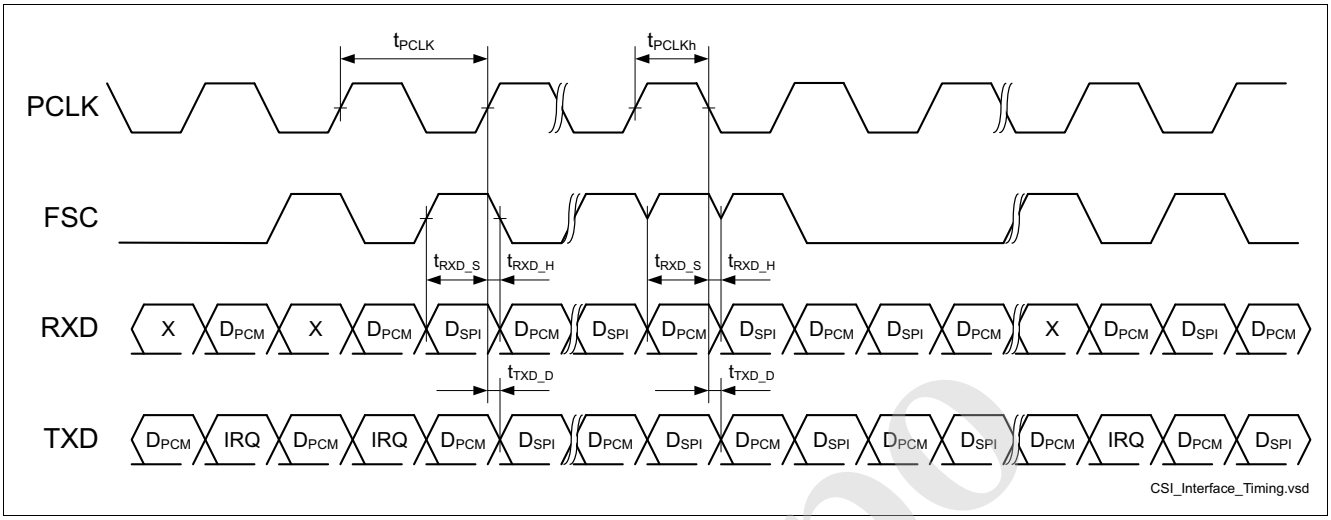


Figure 13 CSI Interface Timing

Table 21 Timing Values for CSI Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Period PCLK[1)]	t_{PCLK}	1/8192	–	1/512	ms	–
PCLK high time	t_{PCLKh}	0.4 x t_{PCLK}	–	0.6 x t_{PCLK}	ms	–
RXD setup time[2)]	t_{RXD_S}	10	–	–	ns	–
RXD hold time[2)]	t_{RXD_H}	5	–	–	ns	–
TXD delay time	t_{TXD_D}	3	–	8 ns + 0.4 [ns/pF] x C_{Load} [pF]	ns	–

1) The PCLK frequency must be an integer multiple of the FSC frequency (n*64*f_{FSC}, n = 1..16).

2) RXD setup and RXD hold time specifications are valid for both rising and falling edges of PCLK.

Table 22 Supported PCLK Frequencies

Clock Rate PCLK [kHz]	Time Slots [per highway]	Data Rate [kbit/s]
512	8	512
1024	16	1024
2048	32	2048
4096	64	4096
8192	128	8192
f = n*64*f_{FSC}, n $\in$ [1,16][1)]	f/64	f

1) n ... integer values, f_{FSC} = 8 kHz

5 Electrical and Transmission Characteristics

5.1 Absolute Maximum Ratings

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 23 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltages at VDD15, VDD1V5, VDD15P referred to GND	–	-0.3	–	1.65	V	–
Supply voltages at VDD33, VDDP33, VDD3V3 referred to GND	–	-0.3	–	3.63	V	–
Supply voltages at VDDSWD	–	-0.3	–	5.5	V	–
Supply voltages differences VDD15, VDD1V5, VDD15P	–	-0.3	–	0.3	V	–
Analog test, filter and gain pins	–	-0.3	–	3.63	V	V_{DD3V3} = 3.3 V, V_{DD1V5} = 1.5 V, V_{GND} = 0 V
Digital input and output pins	–	-0.3	–	3.63	V	V_{DD33} = 3.3 V, V_{DD15} = 1.5 V, V_{GND} = 0 V
Digital input and output pin pad supply voltage 1.8 V	–	-0.3	–	2.1	V	V_{DD33} = 1.8 V, V_{DD15} = 1.5 V, V_{GND} = 0 V
Digital input leakage current per pin	I_L	-50	–	50	µA	$0 \le V_{in} \le V_{DD33}$
DC input or output current on any input or output pin	–	–	–	100	mA	(free from latch-up)
Storage temperature	T_{STG}	-55	–	125	°C	–
Ambient temperature under bias	T_A	-40	–	85	°C	–
Maximum junction temperature	T_J	–	–	150	°C	–
Total supply voltage (SLIC)	V_{DD3V3} - V_N	–	–	154	V	–
ESD Robustness						
ESD voltage	–	–	–	1.5	kV	HBM, Human Body Model ([26])
ESD voltage, all pins	–	–	–	0.75	kV	CDM, Charged Device Model ([27])

5.2 Foreign Line Voltages

External voltages applied to the line outputs may cause large currents in the SLIC. The resulting on-chip power dissipation must be limited to prevent thermal destruction when the overtemperature protection is unable to react fast enough due to high local power density. The safe power dissipation values are highly dependent on duration. They are definable in terms of voltage and current limits directly on the TIP and RING pins (see **Table 24** and **Table 25**).

Table 24 Voltage Limits on Output Pins

Voltage Duration	Pins	Min. Voltage [V]	Max. Voltage [V]
Continuous	TIP, RING	V_N - 0.4	+5
< 10 ms	TIP, RING	V_N - 5	+10
< 100 µs	TIP, RING	V_N - 10	+20
< 1 µs	TIP, RING	V_N - 15	+40

Table 25 Current Limits on Output Pins

Current Duration	Pins	Min. Current [A]	Max. Current [A]
Continuous	TIP, RING	-0.1	0.1
< 10 ms	TIP, RING	-0.5	0.5
< 100 µs	TIP, RING	-1.0	1.0
< 1 µs	TIP, RING	-1.5	1.5

These limits are typical values. They are valid simultaneously and, together with external circuitry, determine the protection requirements.

5.3 Operating Range

V_{GND} = 0 V

Table 26 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltages at VDD15, VDD1V5, VDD15P referred to GND	–	1.425	1.5	1.575	V	1)
Supply voltages at VDD33, VDD3V3 referred to GND	–	3.135	3.3	3.465	V	–
Supply voltages at VDDP33 referred to GND	–	1.71	–	3.465	V	–
Supply voltages at VDDSWD referred to GND	–	3.135	–	5	V	–
Analog test, filter and gain pins	–	0	–	3.3	V	V_{DD3V3} = 3.3 V, V_{DD1V5} = 1.5 V
Analog pin for passive devices CREF referred to GND	–	0.5	0.7	0.9	V	V_{DD1V5} = 1.5 V
Ambient temperature under bias	T_A	-40	–	85	°C	–
Junction temperature under bias2)	T_J	-40	–	125	°C	–
Digital Input/Output Pins (I/O pins, GPIO pins)3)						
High-level input voltage	V_{IH}	2.0	–	3.6	V	$V_{OUT} \geq V_{OH}$ (min)
Low-level input voltage	V_{IL}	-0.3	–	0.8	V	$V_{OUT} \leq V_{OL}$ (max)
High-level output voltage	V_{OH}	2.4	–	–	V	I_{OH} = -3 mA
Low-level output voltage	V_{OL}	–	–	0.4	V	I_{OL} = 3 mA
Average input leakage current per pin	I_{IL}	–	–	20	µA	V_{DD33} = 3.3 V, V_{GND} = 0 V; all other pins are floating, V_{IN} = 0 V or 3.3 V
Input capacitance on digital signal pins	–	–	–	5	pF	–
Input transition rise or fall time on digital signal pins	–	0	–	5	ns	–
Output transition rise or fall time on digital signal pins	–	–	–	7.4	ns	$C_{Load,max}$ = 50 pF
Analog Input Pins (MT, MR)						
Analog input pins referred to GND	–	0.3	–	2.7	V	V_{DD3V3} = 3.3 V
Generated battery voltage	V_N	-150	–	-12	V	–

1) While the external supply voltage is turned on, the 1.5 V ±5% must be guaranteed.

2) Operation up to 150°C is possible. However, a permanent junction temperature exceeding 125°C could degrade device reliability.

3) See **Chapter 4.1.1** for more details on input voltage levels for SPI Interface.

5.3.1 Thermal Resistance

Table 27 lists the thermal resistance parameters.

Table 27 Thermal Resistance PG-VQFN-44

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction to case, top	$R_{th,\ JC\text{-}Top}$	–	18	–	K/W	–
Junction to case, bottom	$R_{th,\ JC\text{-}Bottom}$	–	5.1	–	K/W	–
Junction to ambient	$R_{th,\ JA}$	–	28.6	–	K/W	4-layer, 76.2 x 114.3 mm^2 board with thermal vias

5.3.2 Power-On Sequence

There are no specific requirements for the power-on sequence for the VDD15, VDD1V5, VDD33, VDD3V3, and VDDP33 voltages. Signal voltages must not be applied until the supply voltages on these power pins are stable.

5.3.3 Schmitt Trigger Input Levels

Specific interface pins and all digital pins with input function are of Schmitt Trigger type. The corresponding voltage input levels are shown in Figure 14 and described in Table 28.

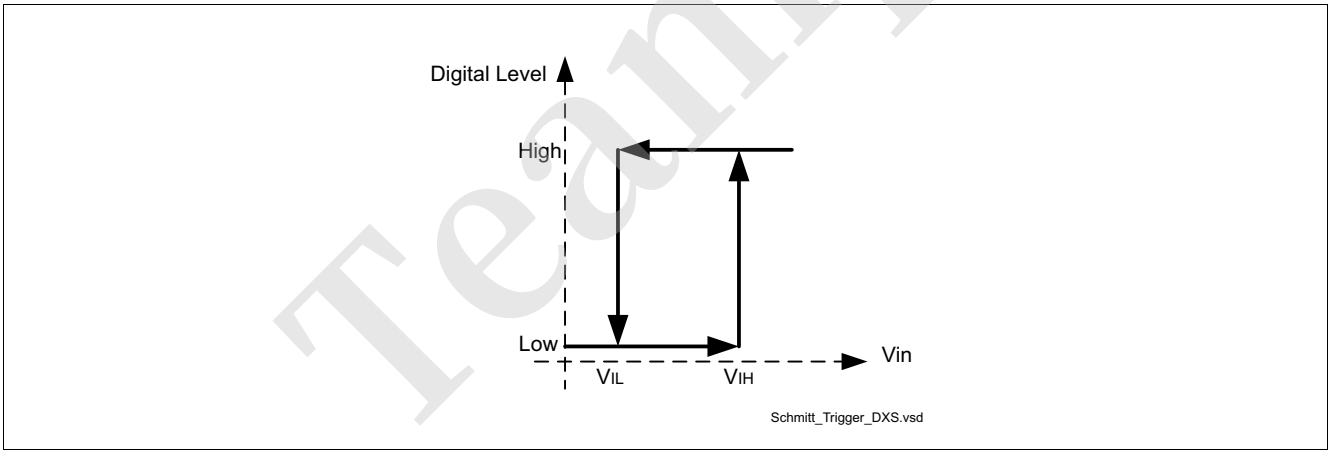


Figure 14 Schmitt Trigger Input Levels

Table 28 Schmitt Trigger Input Levels

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
High-level input voltage	V_{IH}	–	1.7	–	V	VDDP = 3.3 V
		–	0.96	–	V	VDDP = 1.8 V
Low-level input voltage	V_{IL}	–	1.25	–	V	VDDP = 3.3 V
		–	0.80	–	V	VDDP = 1.8 V

5.4 Supply Current and Power Dissipation

The values in **Table 29** and **Table 30** are valid for T_A = 25 °C. The line voltage V_{TR} is set to 40 V and the overhead voltage V_{OVH} is set to 5 V.

Table 29 VN Currents for DXS101 (TIP-RING Open)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VN current **STANDBY**	$I_{N,STBY}$	–	0.25	–	mA	Excludes the current through R_M
VN current **ACTIVE**	$I_{N,ACT}$	–	3.2	–	mA	Open loop, includes the current through R_M
		–	2.3	–	mA	With Automatic Sense Bias Enabled (XTCOS)
VN current **RINGING**	$I_{N,RINGING}$	–	3.2	–	mA	Open loop, includes the current through R_M

Table 30 VDD33 and VDD15 Currents for DXS101 (TIP-RING Open)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VDD33 current **DISABLED**	$I_{DD33,DIS}$	–	0.7	–	mA	–
VDD33 current **STANDBY**	$I_{DD33,STBY}$	–	4	–	mA	–
VDD33 current **STANDBY**	$I_{DD33,STBYLP}$	–	1.3	–	mA	**Sleep State**
VDD33 current **ACTIVE**	$I_{DD33,ACT}$	–	16	–	mA	–
VDD15 current **DISABLED**	$I_{DD15,DIS}$	–	37	–	mA	–
VDD15 current **DISABLED**	$I_{DD15,DISLP}$	–	9	–	mA	**Sleep State**
VDD15 current **STANDBY**	$I_{DD15,STBY}$	–	37	–	mA	–
VDD15 current **STANDBY**	$I_{DD15,STBYLP}$	–	9	–	mA	**Sleep State**
VDD15 current **ACTIVE**	$I_{DD15,ACT}$	–	68	–	mA	–

Power dissipation is always a key parameter in modern dense board designs, but it is particularly important in a highly integrated approach such as the DXS. Whereas the VDD supply currents given above cause a constant on-chip dissipation P_{QDD}, the situation is slightly more complex with the generated battery supply voltage V_N. Power P_{VN} consists of the quiescent power P_{QN} due to V_N bias currents (see **Table 29**) and additional power resulting from any DC line current $I_{L,DC}$. This component P_L consists of a part P_O dissipated in the output stage and the load power P_{Load} (load R_L including loop resistance and protection resistors).

$$P_{VN} = P_{QN} + P_L = P_{QN} + P_O + P_{Load} \quad (1)$$

The total power dissipation of the DXS is:

$$P_{DIS} = P_{QDD} + P_{QN} + P_O = P_Q + P_O \quad (2)$$

The total power consumption of the DXS is:

$$P_{CON} = P_{QDD} + P_{QN} + P_O + P_{Load} \quad (3)$$

Table 31 to **Table 34** show examples of quiescent power dissipation values.

Table 31 Power Calculation in STANDBY Mode with Sleep State

Voltage Supply	U [V]	I [mA]	P [mW]	Notes
VN Supply	40	0.25	10	VN bias current
VN Supply	40	0.04	2	External DC/DC resistor 1 MΩ
VDD 3.3 V Supply	3.3	0.80	3	Low voltage part
VDD 1.5 V Supply	1.5	4.30	6	Low voltage part
VN Supply	40	0.03	1	External measurement resistor 1.5 MΩ
			22	**Total power consumption (P_{CON})**
			19	**SLIC power dissipation (P_{DIS})**

Table 32 Power Calculation in ACTIVE Open Mode

Voltage Supply	U [V]	I [mA]	P [mW]	Notes
VN Supply	45	2.30	104	VN bias current
VN Supply	45	0.20	9	External DC/DC resistor 220 kΩ ($R6$)
VDD 3.3 V Supply	3.3	16.00	53	Low voltage part
VDD 1.5 V Supply	1.5	51.00	77	Low voltage part
			242	**Total power consumption (P_{CON})**
			233	**SLIC power dissipation (P_{DIS})**

Table 33 Power Calculation in ACTIVE Mode With R_{LINE} = 300 Ω Line Termination

Voltage Supply	U [V]	I [mA]	P [mW]	Notes
VN Supply	14.5[1)]	3.20	46	VN bias current
VN Supply	14.5	23.00	333	Line current
VDD 3.3 V Supply	3.3	16.00	53	Low voltage part
VDD 1.5 V Supply	1.5	51.00	77	Low voltage part
			509	**Total power consumption (P_{CON})**
	8.6	23.00	197	Power external resistor (R_{LINE} + 2*R_{PROT})
			312	**SLIC power dissipation (P_{DIS})**

1) See **Equation (4)**.

$$V_N = I_{L,DC} (R_{Int,Tip} + R_{Int,Ring} + 2*R_{PROT} + R_{LINE}) + V_{OVH} = 14.5\ V \quad (4)$$

These conditions apply to **Table 34**:
V_{Ring} = 50 V_{RMS}, f_{Ring} = 20 Hz, V_{DC} = 12 V, V_{OVH} = 5 V, Load = 3 US REN.

Table 34 Power Calculation in RINGING Mode With 3 REN

Voltage Supply	U [V]	I [mA]	P [mW]	Notes
VN Supply[1)]			1255	Average VN power, see also **Table 35**
VDD 3.3 V Supply	3.3	16.00	53	Low voltage part
VDD 1.5 V Supply	1.5	43.00	65	Low voltage part

Table 34 Power Calculation in RINGING Mode With 3 REN (cont'd)

Voltage Supply	U [V]	I [mA]	P [mW]	Notes
			1372	**Total power consumption (P_{CON})**
			987	Power external load
			385	**SLIC power dissipation (P_{DIS})**

1) VN supply in power-optimized tracking mode for ringing.

Table 35 summarizes the calculation of ring power components.

Table 35 Calculation of Ring Power Components

Mode	Load	VN [V]	P_{QN} [mW]	P_O [mW]	P_{Load} [mW]
RINGING[1]	Ringer equiv. $Z = R_L + 1/j\omega C = Z_L e^{i\varphi}$	Tracking supply[2]: $V_N(t) = -\lvert V_{Ring}(t) + V_{DC} \rvert - V_{OVH}$	$-2/\pi * V_{N,peak} * I_{N,ACT}$	$2/\pi * V_{Ring,peak} / Z_L * V_{OVH}$	$(V_{Ring,peak})^2 * \cos\varphi / (2*Z_L)$

1) Sinusoidal ringing $V_{Ring}(t)$ with peak ring voltage $V_{Ring,peak}$ and DC voltage V_{DC}; power values are time averages.
2) For more details refer to the description of quasi-balanced ringing in the System Description [3].

It is also possible to calculate the power required from the VS supply, P_{VS}. VS must deliver the total VN power P_{VN} plus all the losses arising from the DC/DC conversion, P_{Loss}. These include the losses in the external converter parts (switch transistor, inductor, capacitor and diode). Thus:

$$P_{VS} = P_{VN} + P_{Loss} = P_{VN} / \eta \quad (5)$$

It is possible to regard this as a definition of efficiency η. As P_{Loss} includes some virtually constant components (for example SLIC bias current, switching losses), the efficiency depends on power, degrading at low P_{VN} values. Furthermore it depends on the switch transistor, the inductor, the operation mode and the switching frequency. Typical efficiency values range from 60 to 85%.

The instantaneous power dissipation during ringing varies over the ring period. The relationships given in **Table 35** apply to the average power, which together with the efficiency determines the power/current requirements on the VS supply (see **Table 36**). However, when dimensioning the DC/DC components, the maximum power values with respect to the switching cycle must be taken into account. For sinusoidal ring voltages, these differ from the average values by a factor of 2 and π/2, respectively. **Table 36** contains both average and peak ring power values.

$$V_{N,peak} = V_{Ring} * \sqrt{2} + V_{DC} + V_{OVH} \quad (6)$$

$$I_{N,peak} = (V_{Ring} / Z) * \sqrt{2} + I_{N,ACT} \quad (7)$$

The total power consumption is calculated using this equation:

$$P_{TOT} = P_{VS} + P_{VDD,1V5} + P_{VDD,3V3} \quad (8)$$

Table 36 Calculated Typical P_{VS} and Total Power Consumption

Mode	Load /Conditions	P_{VN} [mW]	Efficiency	P_{VS} [mW]	IS_{avg} [mA]	$P_{VDD,1V5}$ [mW]	$P_{VDD,3V3}$ [mW]	P_{TOT} [mW]
STANDBY with **Sleep State**	**Table 31**	13	0.5	25	2	6	3	34
ACTIVE, open	**Table 32**	113	0.65	173	14	77	53	303
ACTIVE, 300 Ω	**Table 33**	379	0.7	542	45	77	53	671

Table 36 Calculated Typical P_{VS} and Total Power Consumption (cont'd)

Mode	Load /Conditions	P_{VN} [mW]	Efficiency	P_{VS} [mW]	IS_{avg} [mA]	$P_{VDD,1V5}$ [mW]	$P_{VDD,3V3}$ [mW]	P_{TOT} [mW]
RINGING, average power measured over a ring period	**Table 34**	1255	0.7	1793	149	65	53	1910
RINGING, peak power measured in a ring period	**Table 34**	2868	0.7	4097	341	65	53	4214

Table 37 shows measured typical power consumption values in different operating modes for the DXS101 and DC/DC converter. The values assume a loop current I_{TRANS} = 23 mA, R_{LINE} = 300 Ω, 2*R_{PROT} = 72 Ω, V_{LIM} = 40 V.

Table 37 Measured Typical Power Consumption Values in Different Operating Modes

Mode	Total Power Consumption (Incl. Codec and DC/DC Losses)
Low power standby mode measured with fixed on-hook voltage of 28 V (incl. hook detection)	32 mW / ch
Active on-hook (active line feed mode without load)	316 mW / ch
Active off-hook (feeding 23 mA, 300 Ω)	683 mW / ch
Ringing 60 V_{RMS} open loop, 5 REN with ring current regulation	2224 mW / ch

5.5 POTS Transmission Characteristics

This section details the AC transmission characteristics and the DC and ringing characteristics.

5.5.1 AC Transmission Characteristics

The specifications given in this section are derived from the Q.552 linecard requirements **[21]** and are given for the complete DXS system and the specified external components (see **Figure 15**). The digital interface is assumed to be a PCM channel.

Test Conditions

T_A = -40 °C to 85 °C, unless otherwise stated

$V_{DD1V5} = V_{DD15P} = V_{DD15}$ = 1.5 V ±5%

$V_{DD3V3} = V_{DDP33} = V_{DD33}$ = 3.3 V ±5%

V_{GND} = 0 V

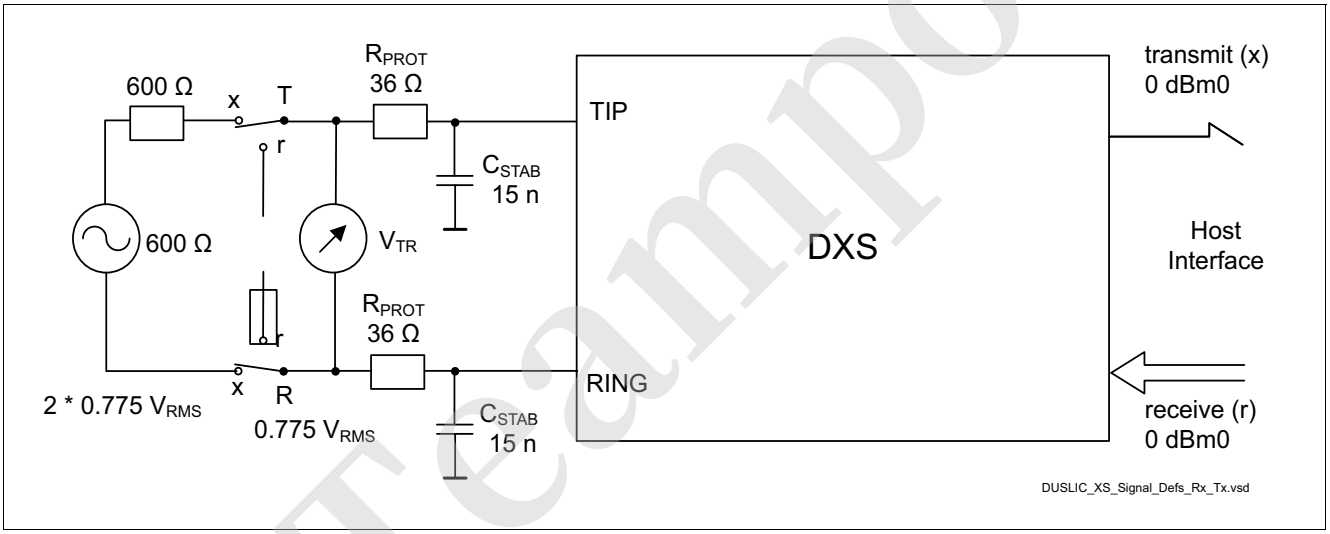


Figure 15 Signal Definitions Transmit, Receive

The following limits are valid for the 600 Ω impedance and for both A-Law and µ-Law.

A digital level of 0 dBm0 is defined as 3.14 dB below the full digital scale for A-Law (3.17 dB for µ-Law). The values in dBm are referred to 600 Ω (0 dBm corresponds to a voltage of 0.775 V_{RMS}).

L_R = -10 dBr means that a signal of 0 dBm0 at the digital input corresponds to -10 dBm at the analog interface.

L_X = +3 dBr means that a signal of 3 dBm at the analog interface corresponds to 0 dBm0 at the digital output.

Range: -12 dBr ≤ L_R ≤ 0.55 dBr (programmable using XTCOS, resolution < 0.1 dB).

Range: -4 dBr ≤ L_X ≤ 6 dBr (programmable using XTCOS, resolution < 0.1 dB).

The AC characteristics described in **Table 38** refer to 0 dBr for both L_R and L_X unless otherwise specified.

Table 38 AC Transmission

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Longitudinal current capability AC	I_{ll}	30	–	–	mA	Per active line
Overload level[1)]	V_{TR}	1.1	–	–	V_{RMS}	300 - 4000 Hz
Transmission Performance (2-wire/4-wire)						
Return loss	RL_2	23	–	–	dB	300 - 500Hz
		26	–	–	dB	500 - 3400 Hz
Balance return loss	RL_4	23	–	–	dB	300 - 3400 Hz
Gain Accuracy (2-wire to 4-wire and 4-wire to 2-wire)						
Gain accuracy – Transmit	G_X	-0.25	–	0.25	dB	1020 Hz
Gain accuracy – Receive	G_R	-0.25	–	0.25	dB	1020 Hz
Frequency Response (see Figure 16 and Figure 17)						
Receive loss Frequency variation	G_{RAF}					Reference frequency 1020 Hz, signal level 0 dBm0
		-0.3	–	–	dB	f = 0 - 300 Hz
		-0.3	–	1.0	dB	f = 300 - 400 Hz
		-0.3	–	0.75	dB	f = 400 - 600 Hz
		-0.3	–	0.35	dB	f = 600 - 2000 Hz
		-0.3	–	0.45	dB	f = 2000 - 2400 Hz
		-0.3	–	0.7	dB	f = 2400 - 3000 Hz
		-0.3	–	1.7	dB	f = 3000 - 3400 Hz
Transmit loss Frequency variation	G_{XAF}					Reference frequency 1020 Hz, signal level 0 dBm0
		0	–	–	dB	f = 0 - 200 Hz
		-0.3	–	–	dB	f = 200 - 300 Hz
		-0.3	–	1.0	dB	f = 300 - 400 Hz
		-0.3	–	0.75	dB	f = 400 - 600 Hz
		-0.3	–	0.35	dB	f = 600 - 2000 Hz
		-0.3	–	0.45	dB	f = 2000 - 2400 Hz
		-0.3	–	0.7	dB	f = 2400 - 3000 Hz
		-0.3	–	1.7	dB	f = 3000 - 3400 Hz
Gain Tracking (see Figure 20)						
Transmit gain Signal level variation	G_{XAL}					Sinusoidal test method f = 1020 Hz, reference level -10 dBm0
		-1.6	–	1.6	dB	Input level: -55 to -50 dBm0
		-0.6	–	0.6	dB	Input level: -50 to -40 dBm0
		-0.3	–	0.3	dB	Input level: -40 to 3 dBm0

Table 38 AC Transmission (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive gain Signal level variation	G_{RAL}					Sinusoidal test method f = 1020 Hz, reference level -10 dBm0
		-1.6	–	1.6	dB	Input level: -55 to -50 dBm0
		-0.6	–	0.6	dB	Input level: -50 to -40 dBm0
		-0.3	–	0.3	dB	Input level: -40 to 3 dBm0
Group Delay (see Figure 21)						
Transmit delay, absolute	D_{XA}	–	–	680	µs	f = 1792 Hz
Receive delay, absolute	D_{RA}	–	–	535	µs	f = 1000 Hz
Group delay distortion, receive and transmit, relative to 1500 Hz	D_{XR}	–	–	900	µs	f = 500 - 600 Hz
		–	–	450	µs	f = 600 - 1000 Hz
		–	–	150	µs	f = 1000 - 2600 Hz
		–	–	750	µs	f = 2600 - 2800 Hz
Longitudinal Balance						
Longitudinal to transversal rejection ratio	LTRR	57	63	–	dB	300 Hz < f < 1 kHz, ACTIVE
		57	63	–	dB	f = 3.4 kHz, ACTIVE
Transversal to longitudinal rejection ratio	TLRR	40	–	–	dB	300 Hz < f < 3.4 kHz, ACTIVE
Signal to Harmonic Distortion Ratio, 2nd Harmonic THD2, 3rd Harmonic THD3 (single test tone), A-Law						
Transmit A-law	THD2	47	–	–	dB	Out.ref.: -7 dBm0 300 - 3400 Hz
Receive A-law	THD2	47	–	–	dB	Inp.ref.: -7 dBm0 300 - 3400 Hz
Transmit A-law	THD3	47	–	–	dB	Out.ref.: -7 dBm0 300 - 3400 Hz
Receive A-law	THD3	47	–	–	dB	Inp.ref.: -7 dBm0 300 - 3400 Hz
Signal to Harmonic Distortion Ratio, 2nd Harmonic THD2, 3rd Harmonic THD3 (single test tone), µ-Law						
Transmit µ-law	THD2	47	–	–	dB	Out.ref.: -7 dBm0 300 - 3400 Hz
Receive µ-law	THD2	47	–	–	dB	Inp.ref.: -7 dBm0 300 - 3400 Hz
Transmit µ-law	THD3	47	–	–	dB	Out.ref.: -7 dBm0 300 - 3400 Hz
Receive µ-law	THD3	47	–	–	dB	Inp.ref.: -7 dBm0 300 - 3400 Hz
Idle Channel Noise						
2-wire port (receive) A-Law	N_{RP}	–	-76	-74	dBmp	Psophometric
µ-Law	N_{RC}	–	14	16	dBrnC	C message

Table 38 AC Transmission (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PCM side (transmit) A-Law	N_{TP}	–	-69	-67	dBm0p	Psophometric
µ-Law	N_{TC}	–	16	19	dBrnC	C message
Total Distortion with A-Law (Sinusoidal Test Method)[2)]						
Signal to total distortion Transmit	STD_X					Output connection: L_X = 0 dBr f = 1020 Hz, psophometrically weighted
		20	–	–	dB	-45 dBm0
		25	–	–	dB	-40 dBm0
		33	–	–	dB	-30 dBm0
		35	–	–	dB	-20 dBm0
		35	–	–	dB	-10 dBm0
		35	–	–	dB	3 dBm0
Signal to total distortion Receive	STD_R					Input connection: L_R = -7 dBr f = 1020 Hz, psophometrically weighted
		14.5	–	–	dB	-45 dBm0
		19.5	–	–	dB	-40 dBm0
		29	–	–	dB	-30 dBm0
		34	–	–	dB	-20 dBm0
		35	–	–	dB	-10 dBm0
		35	–	–	dB	3 dBm0
Signal to total distortion Receive	STD_R					Input connection: L_R = 0 dBr f = 1020 Hz, psophometrically weighted
		25	–	–	dB	-45 dBm0
		29	–	–	dB	-40 dBm0
		35	–	–	dB	-30 dBm0
		35	–	–	dB	-20 dBm0
		35	–	–	dB	-10 dBm0
		35	–	–	dB	3 dBm0

Table 38 AC Transmission (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Total Distortion with µ-Law (Sinusoidal Test Method)[2)]						
Signal to total distortion Transmit	STD_X					Output connection: L_X = 0 dBr f = 1020 Hz, C message-weighted
		20	–	–	dB	-45 dBm0
		25	–	–	dB	-40 dBm0
		33	–	–	dB	-30 dBm0
		35	–	–	dB	-20 dBm0
		35	–	–	dB	-10 dBm0
		35	–	–	dB	3 dBm0
Signal to total distortion Receive	STD_R					Input connection: L_R = -7 dBr f = 1020 Hz C message-weighted
		14.5	–	–	dB	-45 dBm0
		19.5	–	–	dB	-40 dBm0
		29	–	–	dB	-30 dBm0
		34	–	–	dB	-20 dBm0
		35	–	–	dB	-10 dBm0
		35	–	–	dB	3 dBm0
Signal to total distortion Receive	STD_R					Input connection: L_R = 0 dBr f = 1020 Hz, C message-weighted
		20	–	–	dB	-45 dBm0
		25	–	–	dB	-40 dBm0
		33	–	–	dB	-30 dBm0
		35	–	–	dB	-20 dBm0
		35	–	–	dB	-10 dBm0
		35	–	–	dB	3 dBm0

Table 38 AC Transmission (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Crosstalk						
NE crosstalk[3] in TX (TX to TX)	NE_{TX}	–	–	-75	dBm0	Analog input frequency 1020 Hz amplitude 0 dBm0
FE crosstalk[4] in TX (TX to RX)	FE_{TX}	–	–	-75	dBm0	Analog input frequency 1020 Hz amplitude 0 dBm0
NE crosstalk[3] in RX (RX to TX)	NE_{RX}	–	–	-75	dBm0	Analog input frequency 1020 Hz amplitude 0 dBm0
FE crosstalk[4] in RX (RX to RX)	FE_{RX}	–	–	-75	dBm0	Analog input frequency 1020 Hz amplitude 0 dBm0
Power Supply Rejection Ratio[5]						
V_{DD33}/V_{TR} (V_{DD33}: all 3.3 V supplies)	PSR_{R3V3}	– –	38 32	– –	dB dB	300 Hz to 3.4 kHz 4.6 kHz to 100 kHz ACTIVE mode
V_{DD15}/V_{TR} (V_{DD15}: all 1.5 V supplies)	PSR_{R1V5}	– –	45 40	– –	dB dB	300 Hz to 3.4 kHz 4.6 kHz to 100 kHz

1) In ACTIVE mode $L_X = L_R = 0$ dBr
2) For the min. values see also **Figure 23**, **Figure 24** and **Figure 25**
3) Near-end crosstalk according to **[21]**
4) Far-end crosstalk according to **[21]**
5) 20 mV_{RMS} test signal

5.5.1.1 Frequency Response

This section describes the frequency response for narrowband and wideband audio.

5.5.1.1.1 Narrowband Audio

Figure 16 and **Figure 17** show the frequency response for transmit and receive.

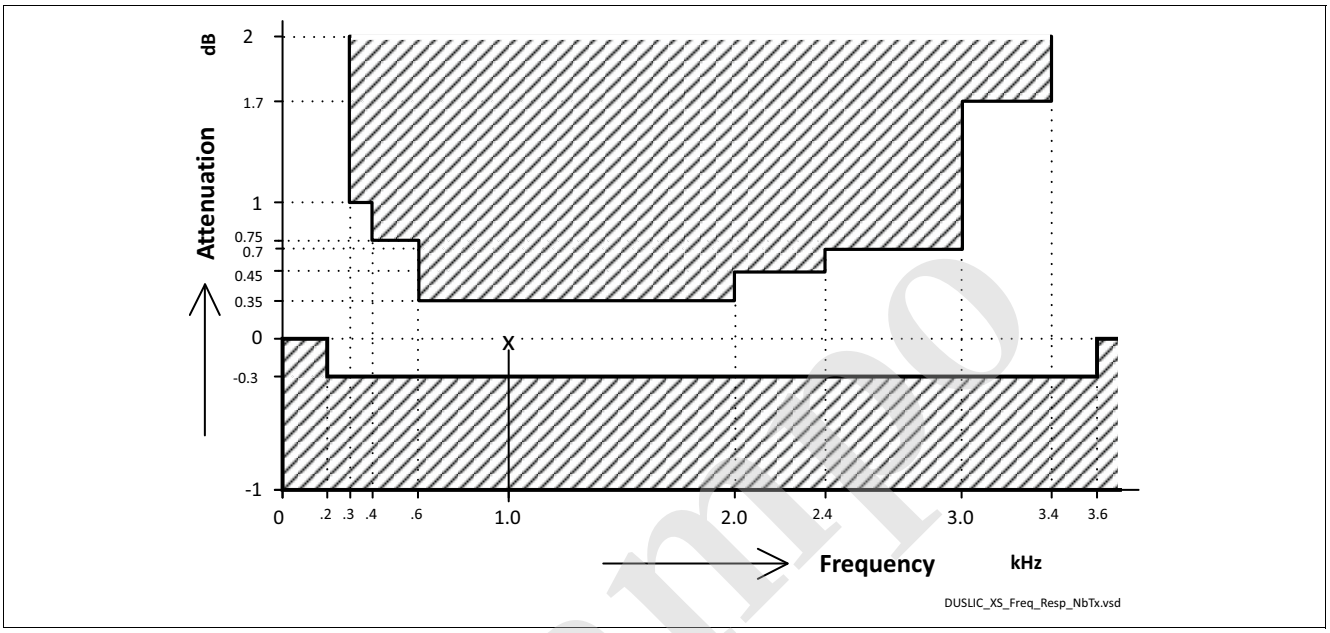


Figure 16 Frequency Response Transmit

Reference frequency 1 kHz, signal level 0 dBm0

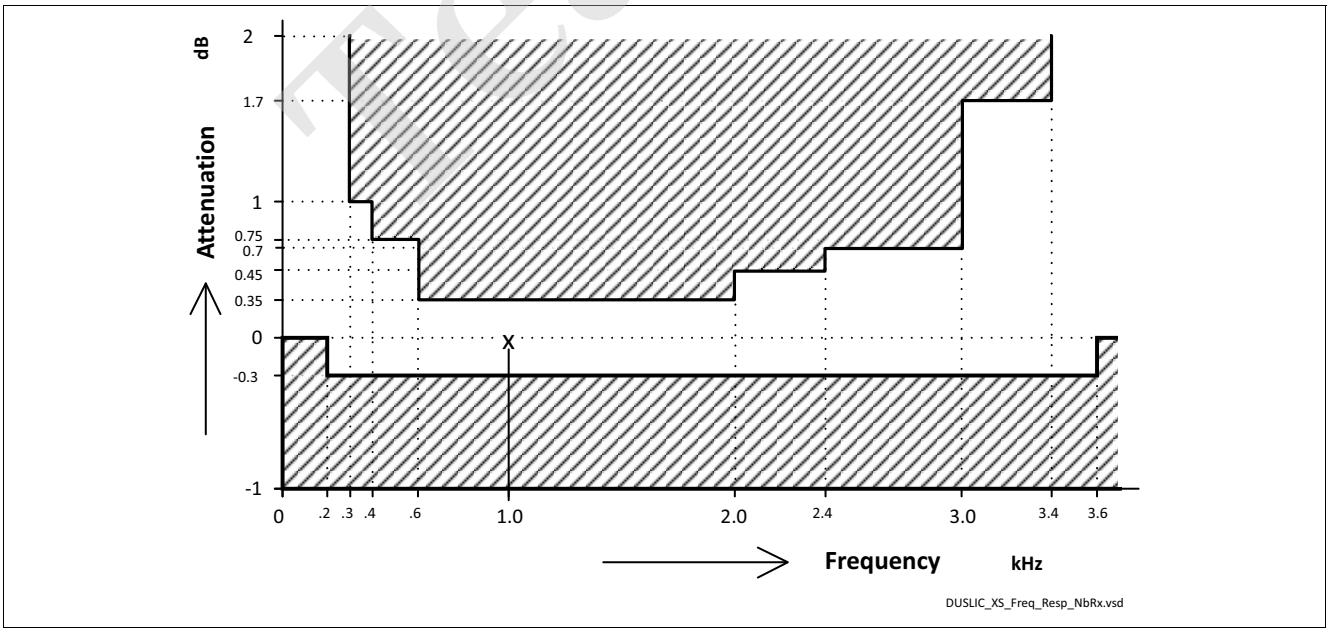


Figure 17 Frequency Response Receive

Reference frequency 1 kHz, signal level 0 dBm0

5.5.1.1.2 Wideband Audio

Figure 18 and **Figure 19** show the frequency response for transmit and receive.

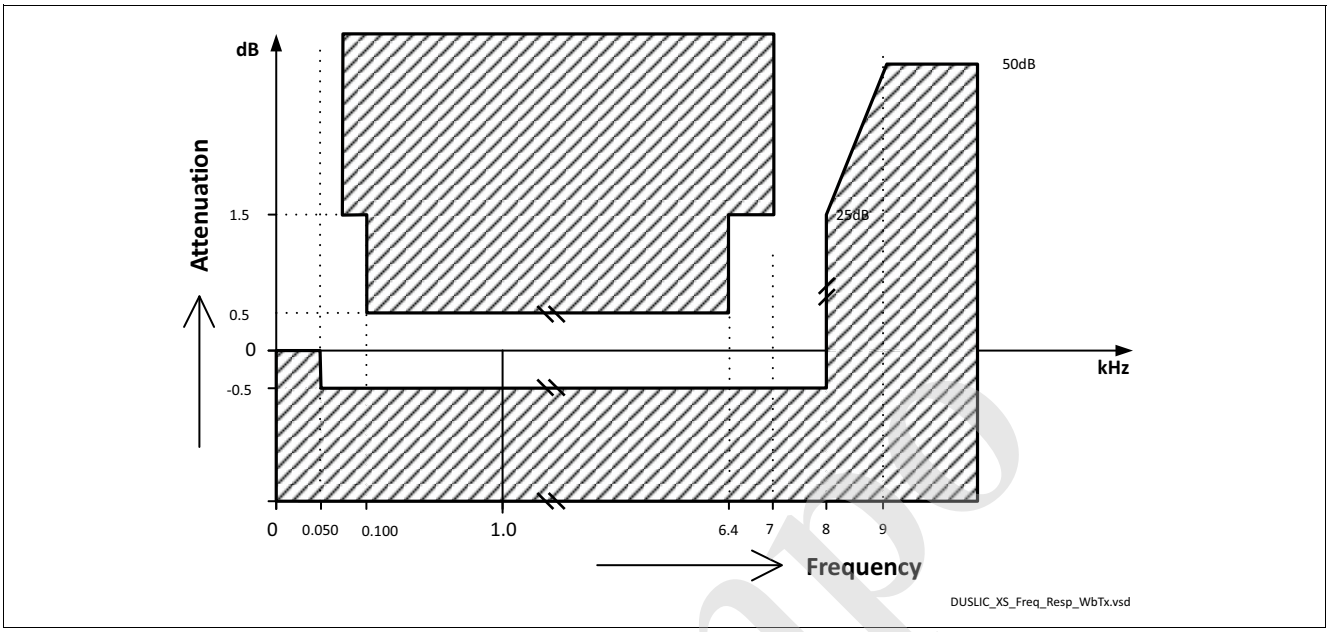


Figure 18 Frequency Response Transmit

Reference frequency 1 kHz, signal level -10 dBm0

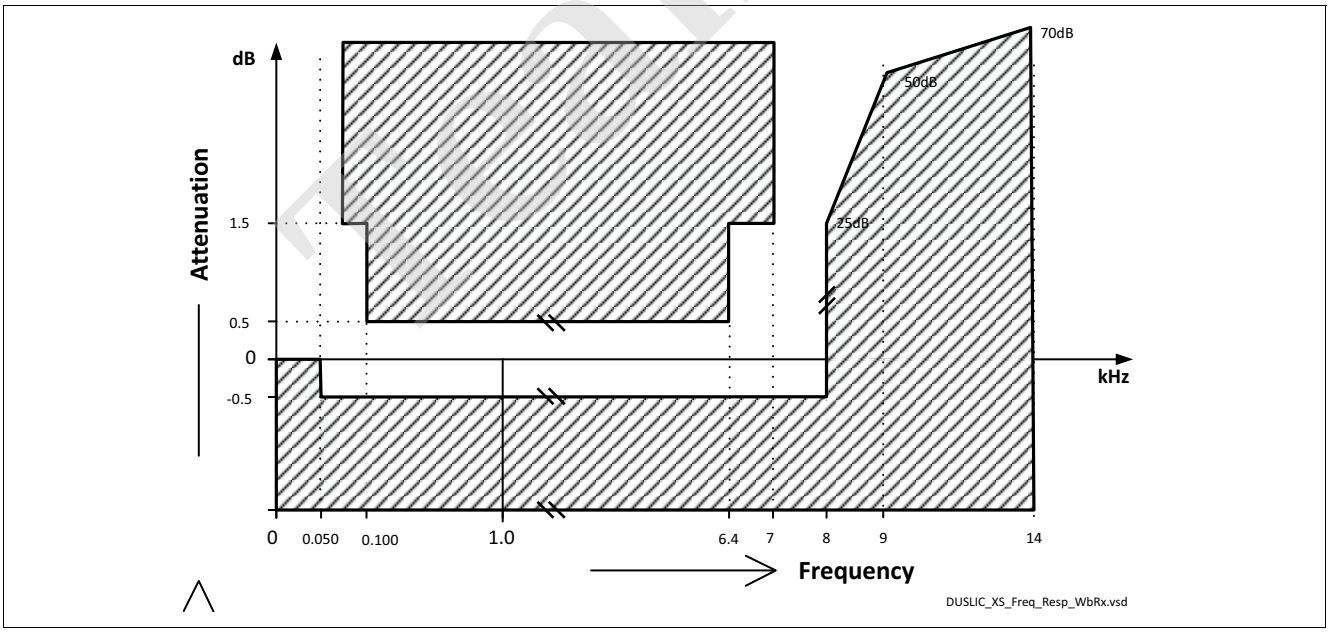


Figure 19 Frequency Response Receive

Reference frequency 1 kHz, signal level -10 dBm0

5.5.1.2 Gain Tracking (Receive or Transmit)

Measured with a sine wave of f = 1020 Hz, reference level is -10 dBm0. In **Figure 20** the gain deviations lie within the limits for T_A = 25 °C.

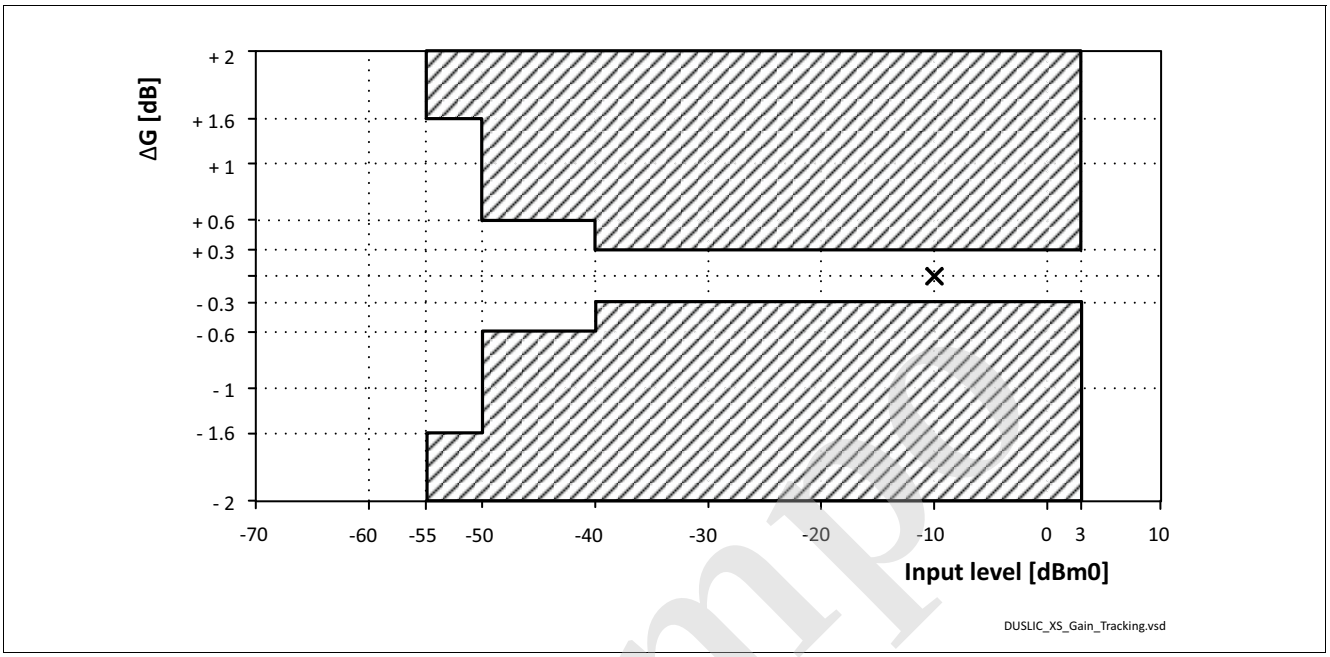


Figure 20 Gain Tracking

5.5.1.3 Group Delay

Group delays depend on internal Frequency Response Receive and Transmit filters and on the delay through A/D and D/A converters. Programmed time slots are also included for PCM transmissions.

5.5.1.3.1 Narrowband

Figure 21 shows the narrowband group distortion.

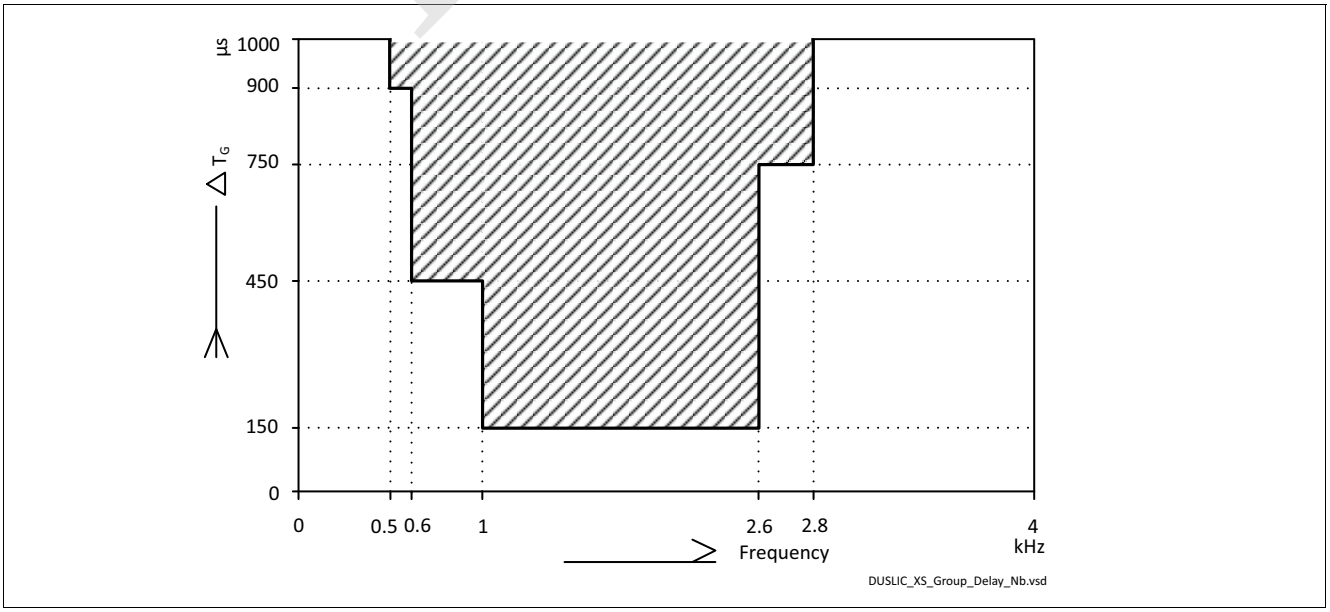


Figure 21 Group Delay Distortion Receive and Transmit, Signal Level is 0 dBm0

5.5.1.3.2 Wideband

Figure 22 shows the wideband group distortion.

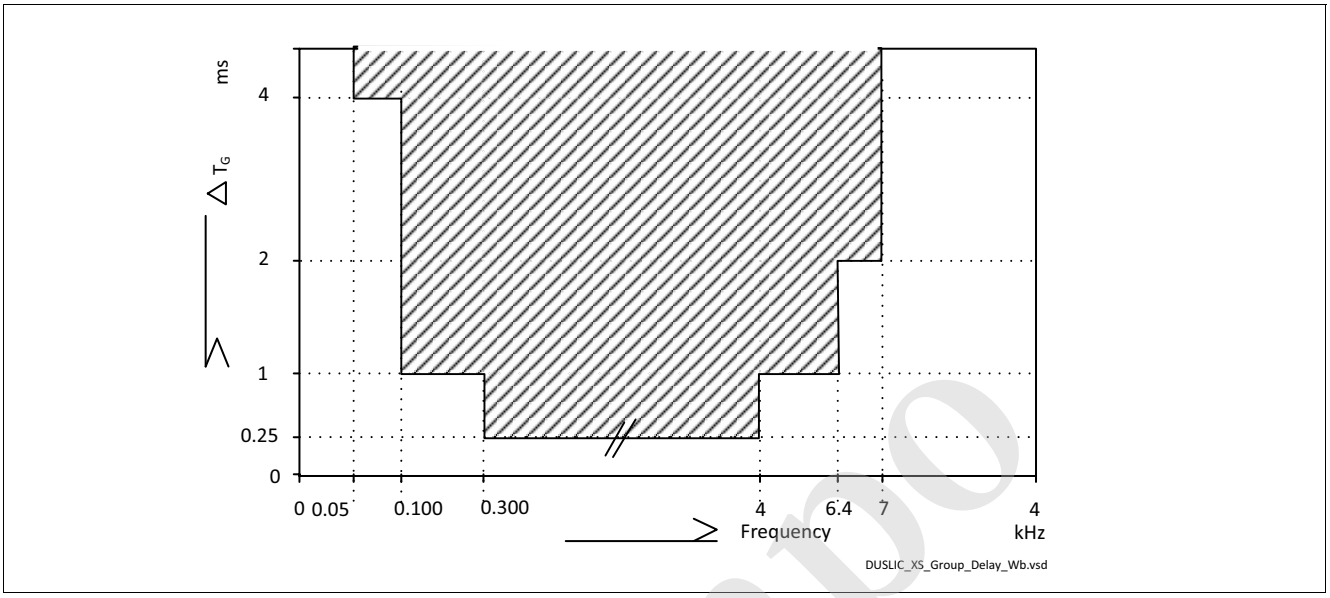


Figure 22 Group Delay Distortion Receive and Transmit, Signal Level is -10 dBm0

5.5.1.4 Out-of-Band Frequency Response (Receive)

With a 0 dBm0 sine wave with a frequency of f (300 Hz to 3400 Hz) applied at the PCM interface, the level of any spurious out-of-band image signal measured selectively at the TIP-RING interface is at least -28 dBm0.

5.5.1.5 Out-of-Band Frequency Response (Transmit)

With a -25 dBm0 sine wave with a frequency of f (4.6 kHz ≤ f ≤ 72 kHz) applied to the TIP-RING wires, the level of any image frequency produced at the PCM interface in the selected time slot is at least 25 dB below the level of the test signal.

5.5.1.6 Total Distortion Measured with Sine Wave

In **Figure 23** the signal to total distortion ratio exceeds the limits.

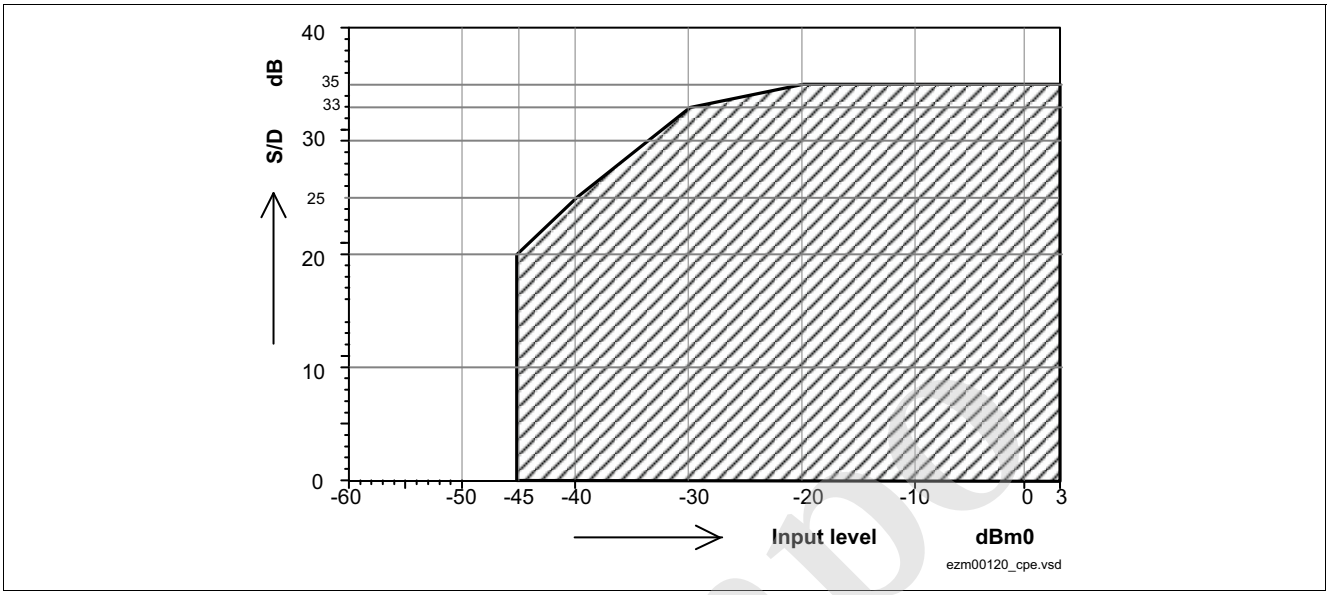


Figure 23 Total Distortion - Transmit (L_X = 0 dBr)

Measured with a sine wave of f = 1020 Hz (C message weighted for µ-Law, psophometrically weighted for A-Law).

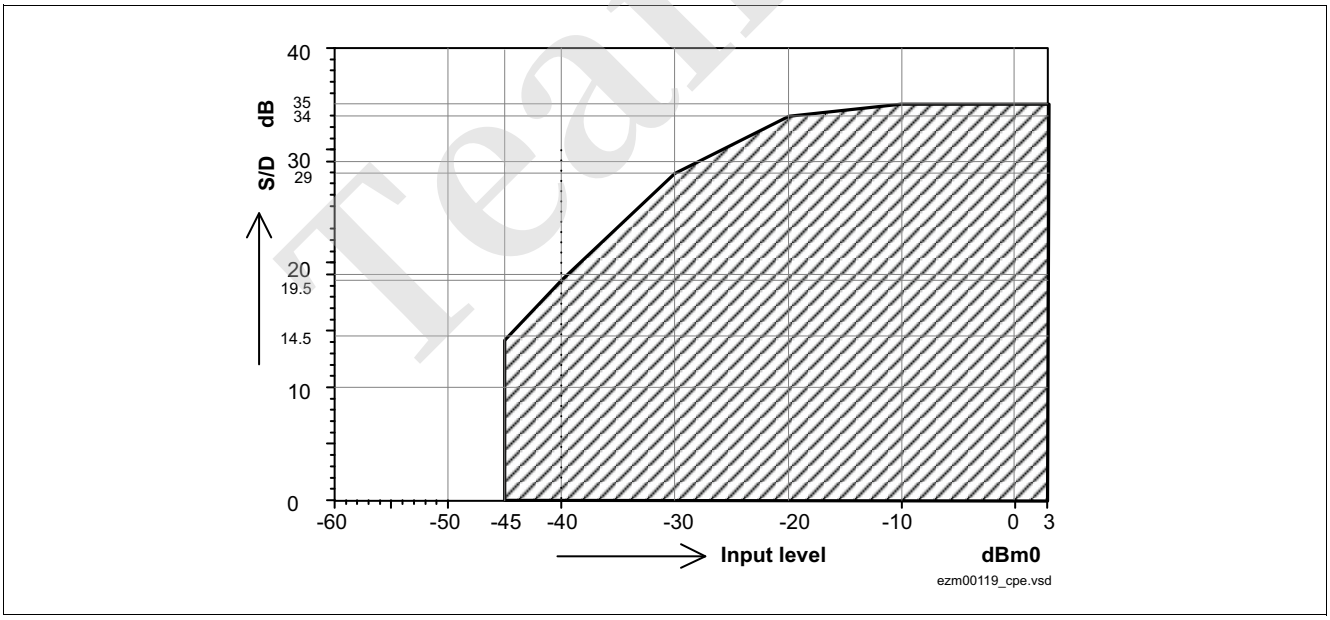


Figure 24 Total Distortion - Receive (L_R = -7 dBr)

Measured with a sine wave of f = 1020 Hz (C message-weighted for µ-Law, psophometrically weighted for A-Law)

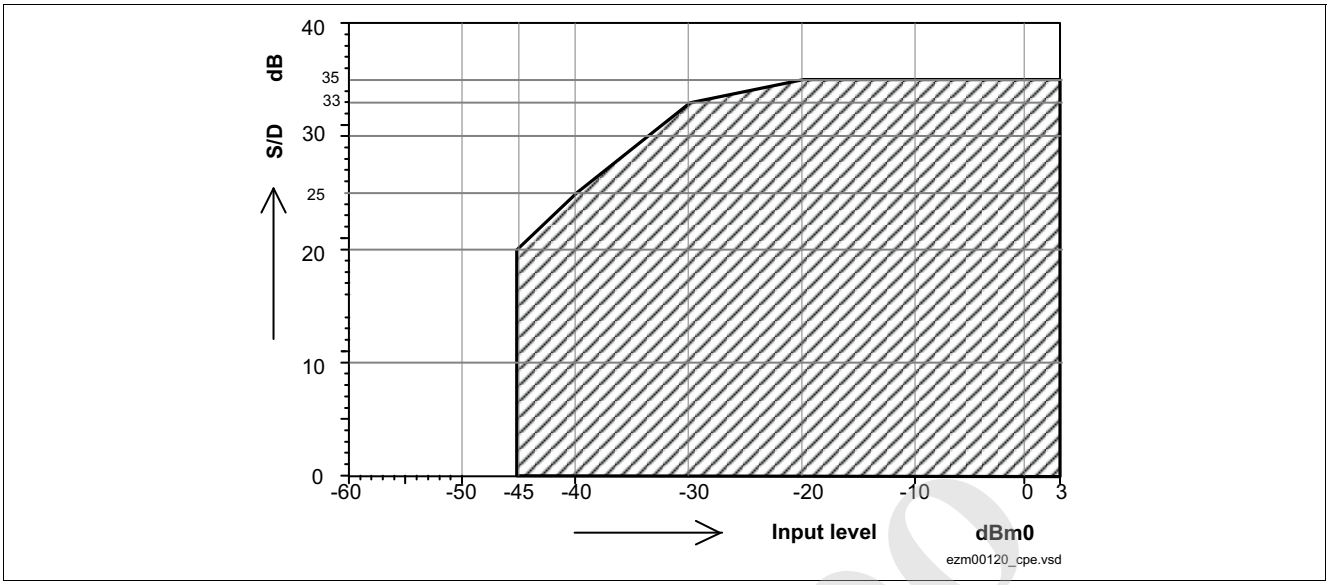


Figure 25 Total Distortion - Receive (L_R = 0 dBr)

Measured with a sine wave of f = 1020 Hz (C message weighted for µ-Law, psophometrically weighted for A-Law).

5.5.2 DC and Ringing Characteristics

The DC and ringing characteristics given in **Table 39** only apply if the channel has been calibrated.

T_A = -40 °C to 85 °C unless otherwise stated.

Table 39 DC Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line Termination Tip, Ring						
DC line voltage drop (see **Figure 26**)	$-V_N - V_{TR,\,max}$	–	2.5	3	V	$I_{Trans,DC}$ = 20 mA T_A = 25°C[1] Mode: **ACTIVE**, **RINGING**
Output resistance SLIC at tip, ring	$R_{Int,Tip}$ $R_{Int,Ring}$	17	20	23	Ω	T_A = 25°C[2]
Output current limitation of SLIC	$\|I_{R,\,max.}\|$, $\|I_{T,\,max.}\|$	70 80	85 100	100 120	mA mA	V_T, V_R = 0 (sinking) V_T, V_R = V_{Nx} (sourcing) Temp = 25°C[3]
Sinusoidal Ringing						
Maximum balanced ringing voltage	V_{RNG0}	80	85	90	V_{RMS}	Ring amplitude set to 85 V_{RMS} + 22 V_{DC} offset, sinusoidal ringing signal.
Harmonic distortion (sinusoidal ringing)	THD	–	–	5	%	–
Ringing voltage tolerance (max. deviation from the programmed value)	V_{RNG0}	–	–	5	%	Range: 15 - 50 Hz
Ringing frequency tolerance (max. deviation from the programmed value)		–	–	0.15	Hz	Range: 15 - 50 Hz
DC ring trip detection	$I_{RTD,DC}$	3.5	5	6.5	mA	DC ring trip threshold = 5 mA
Ring trip detection time	–	–	–	2	cycles	AC or DC RTD
Ring trip detection time	–	–	–	1	cycle	Fast RTD
DC Loop						
TIP-RING open-loop voltage	–	45	48	51	V	ACTIVE mode, V_{LIM} = 48 V
Loop current	I_{TRANS}	23.5	25	26.5	mA	I_{CONST} = 25 mA
Off-hook threshold	I_{OFF}	9.5	10	10.5	mA	ACTIVE mode, hook threshold set to 10 mA
Ground key threshold	I_{GNDKL}	7.5	9.4	11.3	mA	–
Ground fault threshold	I_{GNDKH}	23.9	27.6	31.3	mA	–

1) The systematic temperature dependence is appr. +7 mV / °C
2) The systematic temperature dependence is appr. +0.1% / °C.
3) The systematic temperature dependence is approximately -0.3% / °C

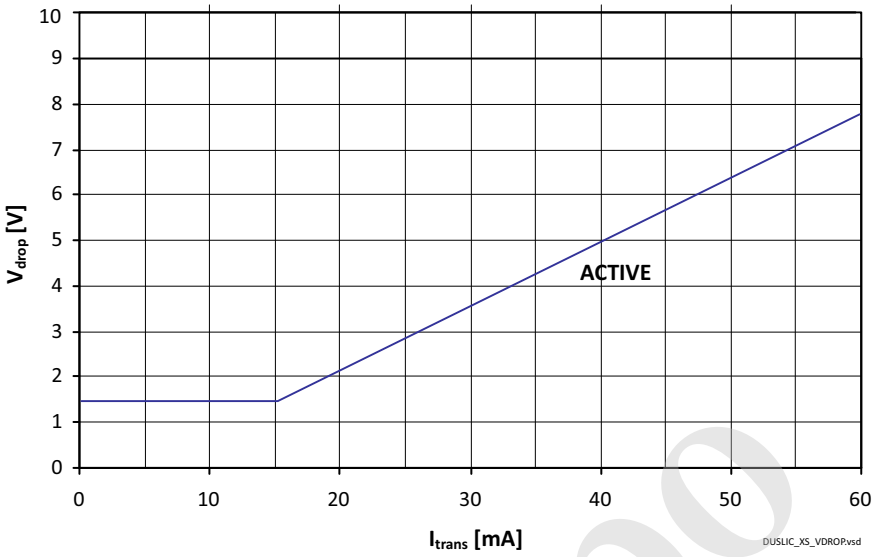


Figure 26 Typical Voltage Drop on Tip and Ring Buffers in ACTIVE and RINGING Operating Modes

5.6 DC/DC Converter Characteristics

Table 40 DC/DC Converter Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching frequency **ACTIVE**	$f_{SW,ACT}$	60	–	1024	kHz	The actual frequency depends on the load and the DC/DC converter topology used.
Switching frequency **STANDBY**	$f_{SW,STBY}$	20	–	512	kHz	–
Switch driver output slew rate	SR	–	50	–	V/µs	C_{Load} = 1 nF

Table 41 DC/DC Converter Output Voltage V_N

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_N range	–	-150	–	0	V	Mode: **RINGING**
Signal headroom	V_{OVH}	5	–	12	V	Mode: **ACTIVE**, **RINGING**
DC/DC converter output voltage	V_N	-24	-22	-20	V	V_{LIM} = 17 V; V_{OVH} = 5 V V_N= V_{LIM} [1] + V_{OVH} = 17 + 5 = 22 V Mode: **ACTIVE**
		-47.5	-45	-42.5	V	V_{LIM} = 40 V; V_{OVH} = 5 V V_N= V_{LIM} + V_{OVH} = 40 + 5 = 45 V Mode: **ACTIVE**
		–	28	–	V	Use fixed voltage instead of DC/DC DAC, V_{STBY} set to 28 V Mode: **STANDBY**
		–	45	–	V	Use fixed voltage instead of DC/DC DAC, V_{STBY} set to 45 V Mode: **STANDBY**

1) In **ACTIVE** off-hook mode, V_{LIM} is the regulated SLIC output voltage. See **Equation (9)**.

$$V_{LIM} = I_{L,DC} (R_{Int,Tip} + R_{Int,Ring} + 2*R_{PROT} + R_{LINE}) \quad (9)$$

6 Application Circuit

Figure 27 shows a typical application circuit for the DXS101.

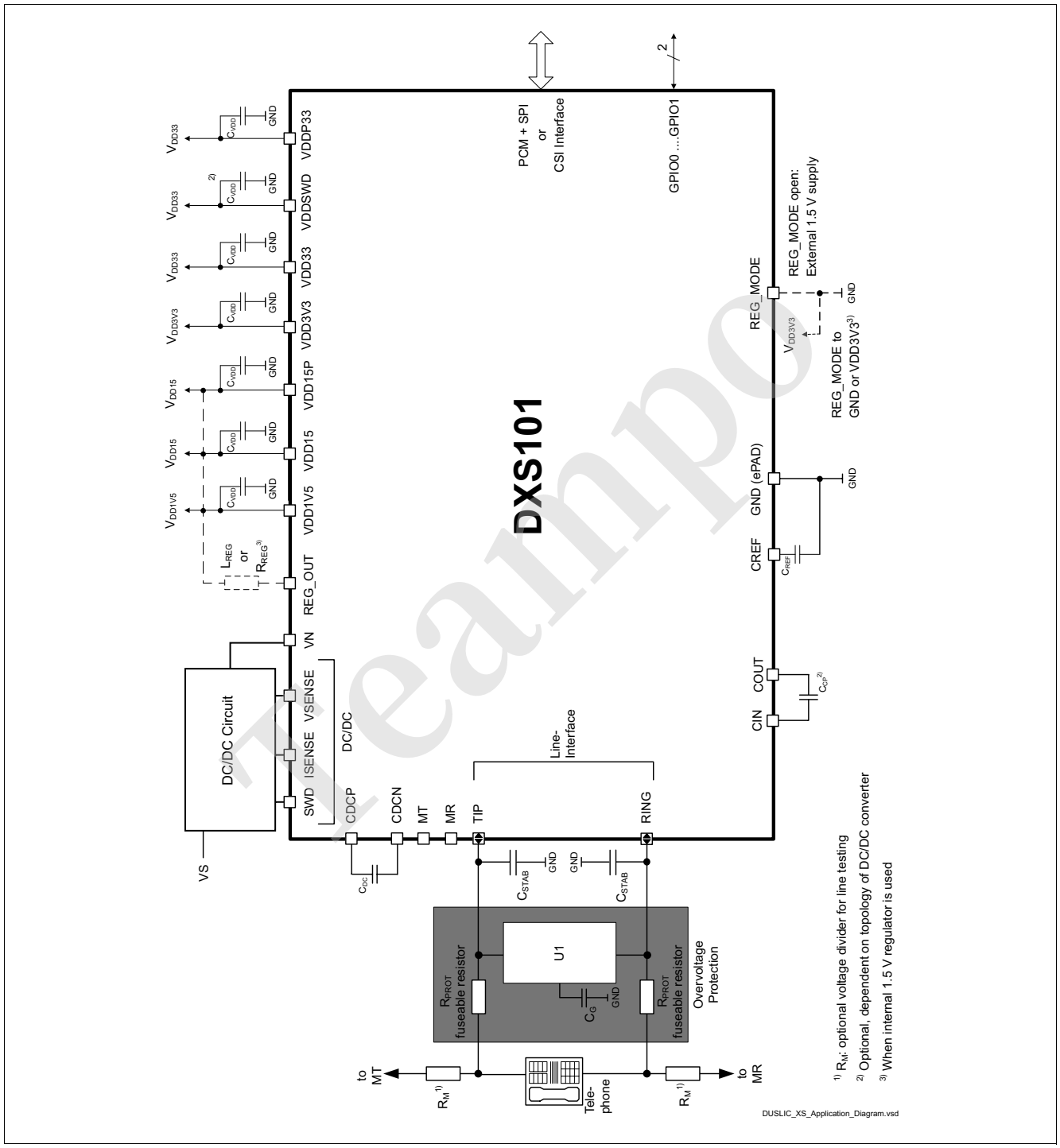
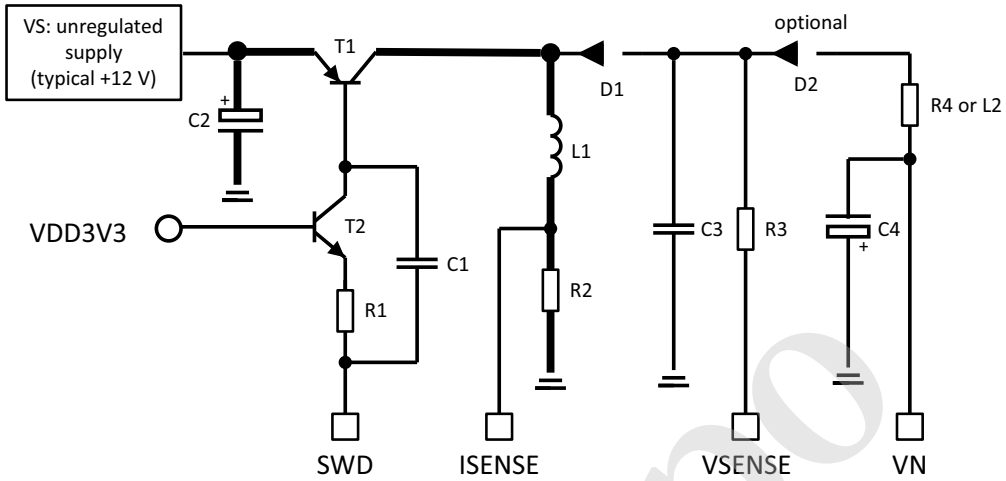


Figure 27 Application Circuit

It is possible to equip the application circuit in **Figure 27** with a DC/DC converter as presented in this section.

- **Inverting buck-boost DC/DC converter with input voltage +12 V (IBB12)**, see **Figure 28**
  This is the recommended default circuit.



Component D2 only has to be used when the gate triggered negative polarity protector for ITU-T K.21 basic requirements is used (refer to the protection requirements application note).

For improved ripple rejection or if diode D2 is used, replace resistor R4 with inductor L2.

DXS_DCDC_converter_bipolar_dedicated.vsd

Figure 28 Inverting Buck-Boost Converter Circuit for 12 V (IBB12)

6.1 Bill of Materials

Table 42 shows the external passive components required for a DXS101 solution with protection. For more details see Figure 27 and Figure 28. The supply input is 12 V and the ringing voltage is 65 V_{RMS} with no DC offset for ringer loads of up to 3 REN or up to 5 REN with ring current regulation.

Depending on the ringing voltages used in the application, some of the device ratings may be reduced. See footnote [1] below Table 42.

For more details on the circuits, please refer to the available documentation and schematics in the reference design package [10].

Table 42 External Components in Application Circuit

Quantity	Symbol	Component Type	Value	Unit	Tolerance	Rating / Comments
DXS101 External Components incl. Protection, see Figure 27						
2	C_{STAB}	Capacitor	15	nF	10%	150 V[1]
2	R_M[2]	Resistor	1.5	MΩ	1%	0.25 W, 200 V[3]
1	C_{DC}	Capacitor	330	nF	10%	10 V
2	R_{PROT}	Resistor	36	Ω	1%	0.25 W (depending on protection requirements, refer to [12])
1	C_{REF}	Capacitor	220	nF	10%	10 V
1	*U1*	Protection element	–	–	–	Overvoltage protection, e.g. Bourns* TISP 6NTP2C[4] or STMicroelectronics* LCDP1521S[4], refer to [12]
2	C_G	Capacitor	100	nF	20%	150 V[1], capacitor on gate of protection thyristor (refer to data sheet of protection element used)
7	C_{VDD}	Capacitor	Typ. 10[5]	µF	20%	10 V
1 optional	C_{CP}	Capacitor	100	nF	10%	50 V
1.5 V Supply Regulation, see Figure 3 and Figure 27						
1 optional[6]	R_{REG}	Resistor	1.5	Ω	–	If internal 1.5 V regulator is used in linear mode (low cost option)
	L_{REG}	Inductor	3.3	µH	5%	Murata* LQH31MN3R3J03, Idc = 130 mA max If internal 1.5 V regulator is used in step-down mode (low power option)
Inverting Buck-Boost Converter Circuit T0.2 for 12 V, see Figure 28						
1	*C1*	Capacitor	47	nF	10%	10 V
1	*C2*	Capacitor	22	µF	20%	16 V, electrolytic type (low ESR)
1	*C3*	Capacitor	220	nF	10%	150 V[1], ceramic capacitor
1	*C4*	Capacitor	2.2	µF	10%	160 V[1], ECA2CM2R2 from Panasonic* (electrolytic capacitor, low ESR)
1	*D1*	Diode	–	–	–	150 V, 1 A, needs to be of “fast” or “ultra-fast” type, e.g. ES1C, MURS120 or equivalent

Table 42 External Components in Application Circuit (cont'd)

Quantity	Symbol	Component Type	Value	Unit	Tolerance	Rating / Comments
1	*L1*	Inductor	47	µH	20%	I_{PEAK} = 1.55 A, e.g. EPCOS B82464G4473
1	*R1*	Resistor	160	Ω	5%	0.1 W
1	*R2*	Resistor	82	mΩ	5%	0.25 W
1	*R3*	Resistor	1	MΩ	1%	150 V, 0.125 W
1	*R4*[7)]	Resistor	20	Ω	5%	0.25 W
	L2	Inductor	220	µH	10%	0.1 A, TDK NLCV32T-221K
1 optional	*D2*	Diode	–	–	–	200 V, 0.2 A, BAS21 or equivalent; optional, depending on used protection
1	*T1*	Transistor	–	–	–	Zetex* DXT2014P5, PNP switching transistor; an alternative type is NXP PBHV9215Z (about 3% less efficiency)
1	*T2*	Transistor	–	–	–	SMBT3904S, NPN silicon transistor or equivalent

1) Depending on the maximum required voltage; for 65 V_{RMS} ringing, a device rating of 100 V is sufficient.
2) Voltage divider for line testing.
3) Depending on the protection requirements, resistor R_M may be split into more than one component (see to **Chapter 7.2.2**).
4) In the case of the dual overvoltage protectors TISP 6NTP2C and ST LCDP1521S, only one element is necessary.
5) Depends on layout considerations and the application. The sum of the capacitance of all C_{VDD} capacitors per voltage rail on the PCB must be of about 10 µF.
6) If the internal 1.5 V regulator is used. However, neither optional component (R_{REG} nor L_{REG}) is required if an external 1.5 V supply is used. Refer to **Chapter 3.2.1** for further details.
7) For improved ripple rejection or if diode *D2* is used, replace resistor *R4* with inductor *L2*.

For more information on the list of components, including different DC/DC converter topologies, refer to **[11]** and the available schematics in the evaluation package documentation.

7 Hardware Design Guidelines

The guidelines in this section serve as a reference for the design of applications using the DXS101. They are intended to help the reader become familiar with the DXS101 devices and to accelerate the development process. These design and layout guidelines aim at achieving optimum performance for a POTS application. Adhering to these guidelines helps to ensure a reliable design.

7.1 Power Supply and Grounding

This section gives guidelines for the power supply and grounding design.

7.1.1 DXS101 Codec Part Supply

The codec part of the DXS101 chip requires two supply voltages: +3.3 V and +1.5 V[1)]. The tolerance of these supply voltages is ±5%.

These supply voltages are used to supply digital sections of the DXS101:

- VDDP33: Digital supply for I/O pads (+3.3 V)
  2.5 V or 1.8 V is optional for the I/O pads
- VDD33: Digital supply for DC/DC converter (+3.3 V)
- VDD15: Power supply for digital parts (+1.5 V)

These supply voltages are used to supply analog sections of the DXS101:

- VDD3V3: Analog supply voltage (+3.3 V)
- VDD1V5: Analog supply voltage (+1.5 V)
- VDD15P: PLL supply voltage (+1.5 V)

The analog supply voltages must be kept separate from the digital supply and only connected at a central point in the design. When the Enhanced Idle Channel Noise requirements must be met, the digital and analog supplies must be connected via LC filters or ferrite beads (140 Ω @ 100 MHz, 0.55 Ω DC, 200 mA). It is not mandatory for the analog supply voltages to be generated locally.

The power supply pins of the PLL are described in **Chapter 7.1.3.3**.

For a calculation of the maximum power consumption of the DXS101, see **Chapter 5.4**.

7.1.2 DXS101 SLIC Part Supply

The SLIC requires a V_N voltage that depends on the line feeding conditions and operating modes. This supply voltage is within the range -12 V down to -150 V, and is generated by a DC/DC converter where the PWM controller is located at the DXS101. The DC/DC converter itself requires an unregulated power supply that depends on the DC/DC converter topology. Typical VS voltages are +12 V, +3.3 V and -48 V. In the case of a 12 V supply, the power supply needs to be blocked with at least 22 µF. Refer to the reference schematics and the DC/DC Converter Externals Application Note **[11]** for details on other DC/DC converter topologies.

The highest power consumption occurs during ring trip. In the case of DC ring trip, it may take up to two ring periods for off-hook to be detected, resulting in an extended period of high power consumption. Use the fast ring trip feature of the DXS101 to reduce this high power consumption period, and consequently reduce the cost of the power supply.

1) 1.5 V is either supplied from an external source or from the integrated 1.5 V regulator.

7.1.3 Supply Filtering

This section gives guidelines for the supply filtering design.

7.1.3.1 DXS101 Supply Concept

The parasitic capacitances to digital ground (GND) must be minimized for analog pins. **Figure 29** shows the principle of this power supply concept. Also refer to **Figure 3** in **Chapter 3.2.1** when using internal 1.5 V regulation, and to **Chapter 7.1.3.4** when using a charge pump.

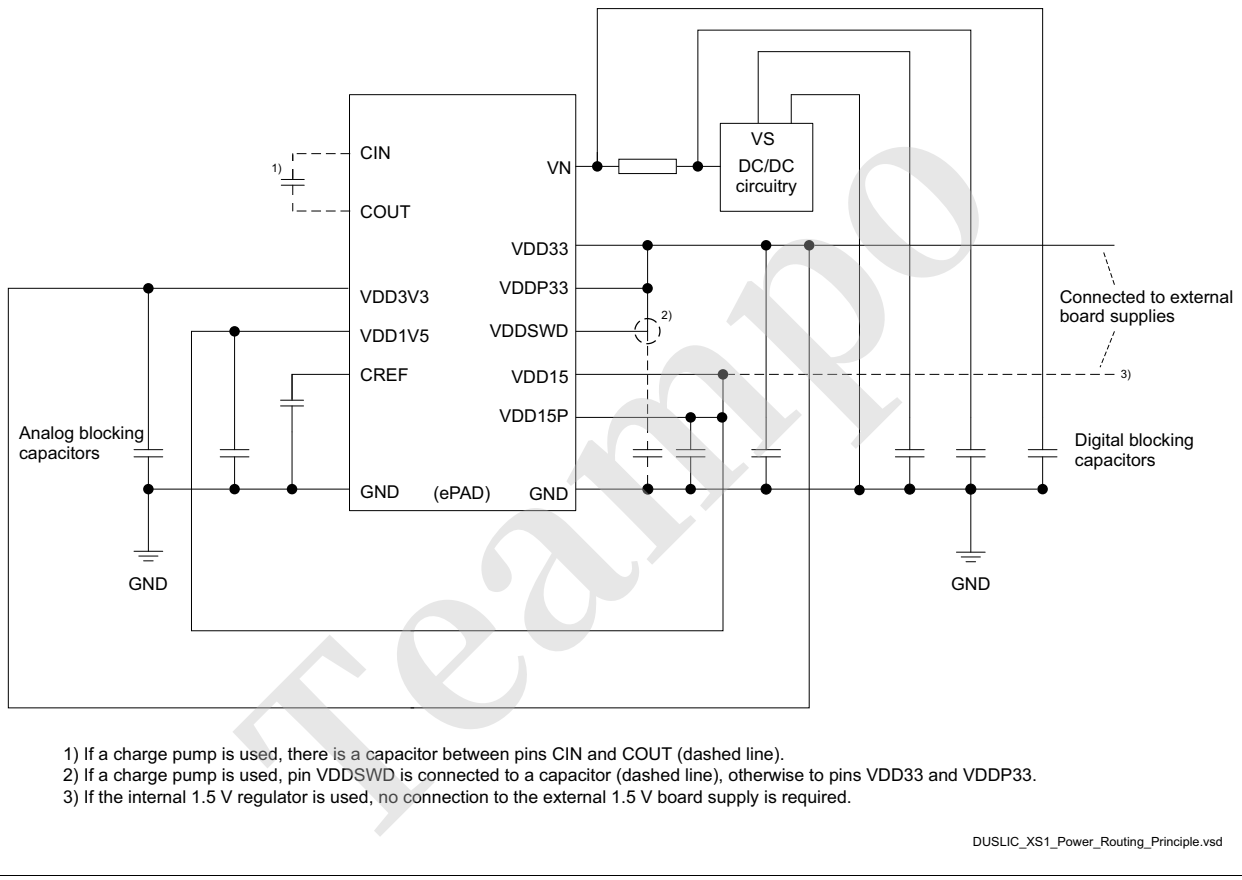


Figure 29 Supply Concept

7.1.3.2 Decoupling the DXS101 Supply Voltages

Table 43 lists the capacitors recommended for the DXS101 device.

Table 43 Required Decoupling Capacitors

Supply Pin Group	Decoupling Capacitor
Core supply pins (VDD15)	100 nF ceramic capacitors on each supply pin
Digital interface supply pins (VDDP33)	
Digital supply voltage (VDD33)	2.2 µF and 100 nF in parallel on the supply pin referred to GND
Analog +1.5 V supply pins (VDD1V5)	2.2 µF on each supply pin referred to ground
Analog +3.3 V supply pins (VDD3V3)	2.2 µF and 100 nF (ceramic) in parallel on each supply pin referred to ground
PLL supply pin (VDD15P)	100 nF directly at the pin
DC/DC converter supply (VS)	At least 22 µF (placed near the power pins)
SLIC supply (VN)	2*2.2 µF, low ESR
Charge pump (optional)	2*100 nF ceramic capacitor (between pin VDDSWD and GND, and between pins CIN and COUT)

7.1.3.3 PLL Supply Voltage (VDD15P)

VDD15P supplies an analog section of the codec, but is filtered against the digital ground to avoid disturbance of the other analog supplies. A blocking capacitor of 100 nF referred to digital ground (GND) must be placed directly on the pin VDD15P to filter high frequency power supply noise. VDD15P is directly connected to the +1.5 V digital power supply rail.

7.1.3.4 Charge Pump Function (VDDSWD)

The charge pump function allows the support of high level MOS transistors with no external driver stage. The internal charge pump is connected to three pins CIN, COUT and VDDSWD. When no charge pump is used, VDDSWD must be connected to VDD33 and CIN, COUT must be left unconnected.

When the charge pump is used, a 100 nF capacitor is connected between VDDSWD and GND, and a second 100 nF capacitor must be connected between CIN and COUT.

7.2 Layout Recommendations

All the figures in this section show the analog channel decoupling capacitors, but not the decoupling capacitors for the digital power supplies.

7.2.1 Placement

This section gives placement recommendations for the digital and analog parts of the design.

7.2.1.1 Placement Recommendations for the Digital Part

These are the placement recommendations for the digital part of the design:

- Place decoupling capacitors as close as possible to the supply pins of the DXS101 and each associated ground pin.
- The decoupling capacitor of the PLL must be placed as close as possible to the device.
- To reduce reflections, consider these mounting options for the PCM highway, especially for long or branching lines.
  - For the FSC and PCLK signals, an AC termination to ground is recommended on the DXS101 (receive side) to avoid distortion.
  - A serial termination is recommended on the transmitter side.
- The pull-up resistors must only be placed once in the system for the interrupt signals (INT), PCM data lines (TXD and RXD).
- When GPIO pins operate as outputs, leave them open. When a GPIO signal is programmed to be an input, a pull-up/down is required when it is not possible to guarantee a stable signal at all times.

7.2.1.2 Placement Recommendations for Analog Part

This section refers to the typical external components shown in **Figure 27** and the recommended DC/DC converter application circuit shown in **Figure 28**. These are the placement recommendations for the analog part of the design:

- C_{REF} must be placed as close as possible to the CREF pin since this filters the on-chip reference voltage.
- The voltage sense resistor for the DC/DC converter must be placed as close as possible to the VSENSE input pin. A maximum wire length of 5 mm is allowed, and the wire must not be close to the ground plane.
- The blocking capacitors must be placed as close as possible to the respective pins of the device.
- C_{DC} must be placed close to the DXS101.
- Place the resistors R_{PROT} and capacitors C_{STAB} (see **Figure 27**) near to the SLIC or near to the protection components. The wires (tip and ring) must be routed in parallel, as differential lines, between the protection components and the SLIC.
- A 22 µF (minimum value) blocking capacitor must be placed close to the input pins of the DC/DC converter circuitry, see $C2$ in **Figure 28**.
- The components of the DC/DC converter circuit must be placed close together. The area must be as small as possible to avoid disturbances.
- The switching transistor needs a heat sink of at least 100 mm^2.
- The value for the sense resistor $R2$ in the recommended default schematic (see **Figure 28**) depends on the DC/DC converter type used. A value of 0.082 Ω must be used for the standard application with dedicated DC/DC converter control.
- The traces of the circuitry between pin VNx and the inductor $L1$ (including the capacitors $C3$ and $C4$) must have a width of min. 1.5 mm.

- The 2.2 µF capacitor at the VN supply may be of type X7R or electrolytic. The voltage rating must be chosen according to the application needs and the 2.2 µF capacitor must be of low ESR type to minimize voltage ripples on VN.
- The parts and traces of the DC/DC converter must not be placed near the tip and ring lines, or must be routed in a separate layer.

7.2.2 Routing

These are the general recommendations for routing:

- The ground of the DC/DC converter circuitry is referred to the digital ground (GND). It is possible to route this signal as a trace. No plane is required.
- The digital tracks must not cross or be placed parallel to the analog tracks of the DXS101. This especially includes the PCM interface signals and clock signals. Host controller interfaces including the control signals must not to be routed through the analog section. It is recommended that these tracks are routed out of the package on the digital side in an inner layer or on the bottom layer to avoid crosstalk to sensitive analog circuitry.
- The digital host interface and clock signals must be routed on the component and solder side and kept far away from the analog signals.
- The control lines must be routed on the component side (top side).
- The connection to GND, the battery voltages, and all the connections to the protection devices must be low impedance to prevent ground bouncing due to the high impulse currents in the case of an overvoltage strike - wide tracks or planes are required.

These are the recommendations for the line side:

- Depending on the protection requirements, the track width from the TIP/RING interface to the external overvoltage protector (if used) must be chosen appropriately. In practice, a trace width of 1.6 mm is sufficient to meet most surge requirements.
- When a layer change is necessary between the line connector and protection device (for example, a TISP element), three vias must be used, as one is not sufficient. This is not necessary between the tip and ring lines and the R_M resistors or to the 15 nF capacitors.
- The connections between the C_{STAB} capacitors and ground must be low impedance.
- Depending on the protection requirements, the resistance R_M may need to be split into more than one component in order to satisfy the maximum voltage rating specification of the components used. In certain cases, two (2 x 750 kΩ) or three (3 x 499 kΩ) resistors in series are recommended.

These are the recommendations for the DC/DC converter are:

- The traces for the input voltage of the DC/DC converter must be routed separately and must be connected near to the power supply at a blocking capacitor (star point).
- The power supplies are placed in the two inner layers on a multi-layer board or in large traces (0.2 mm - 0.3 mm width) on a 2-layer board.
- The components of the DC/DC converters must be placed on the smallest possible area, the traces must have a minimum width and coupling to the analog part must be minimized to avoid noise (**Figure 30**).
  The main current loops for the DC/DC converter during the two switching periods are:
  – Switch on-time: VS blocking capacitor - switch - coil - current sense resistor - VS blocking capacitor
  – Switch off-time: coil - diode - VN filter capacitor - current sense resistor - coil
  The four components $L1$, $R2$, $D1$ and $C3$ must be placed close together on one side of the PCB in order to minimize the current loop.

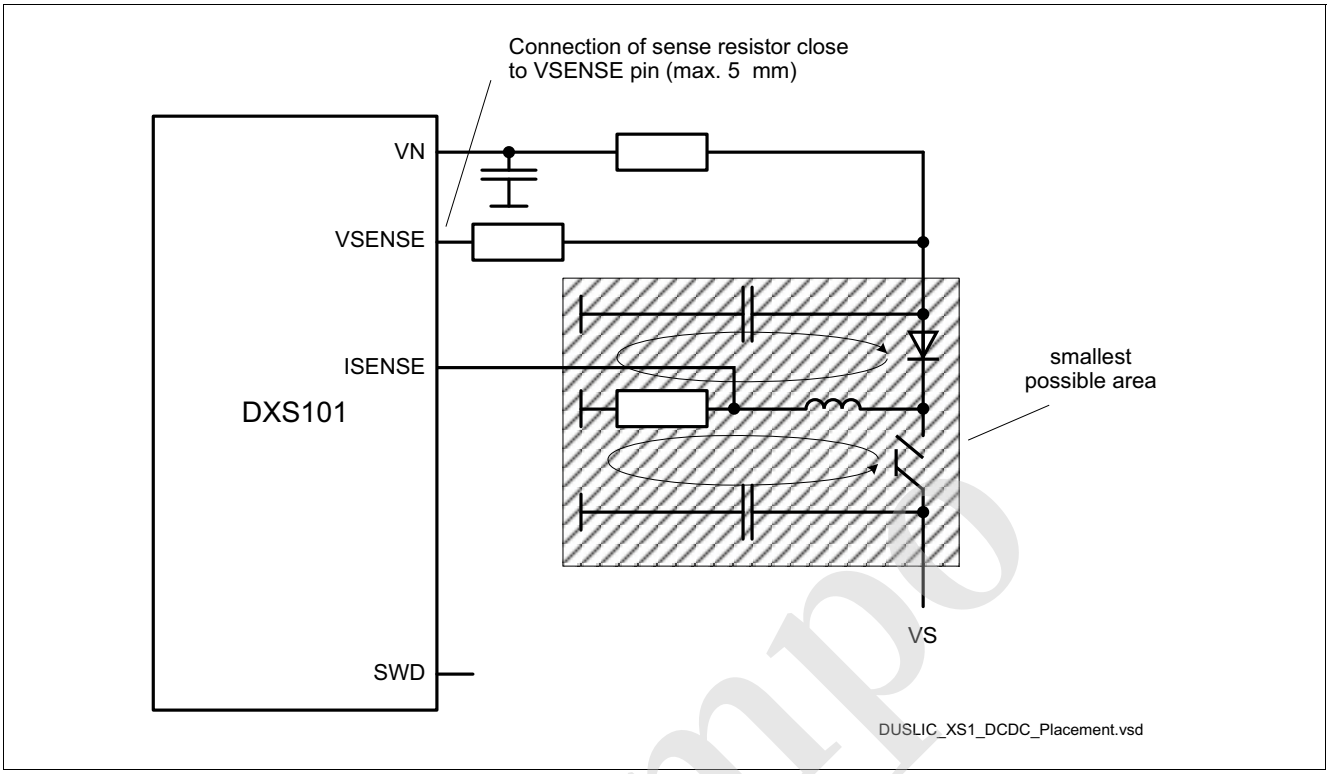


Figure 30 DC/DC Converter Component Placement

7.3 Unused Pins

Unused pins must be left open (not connected).

8 Package Outlines

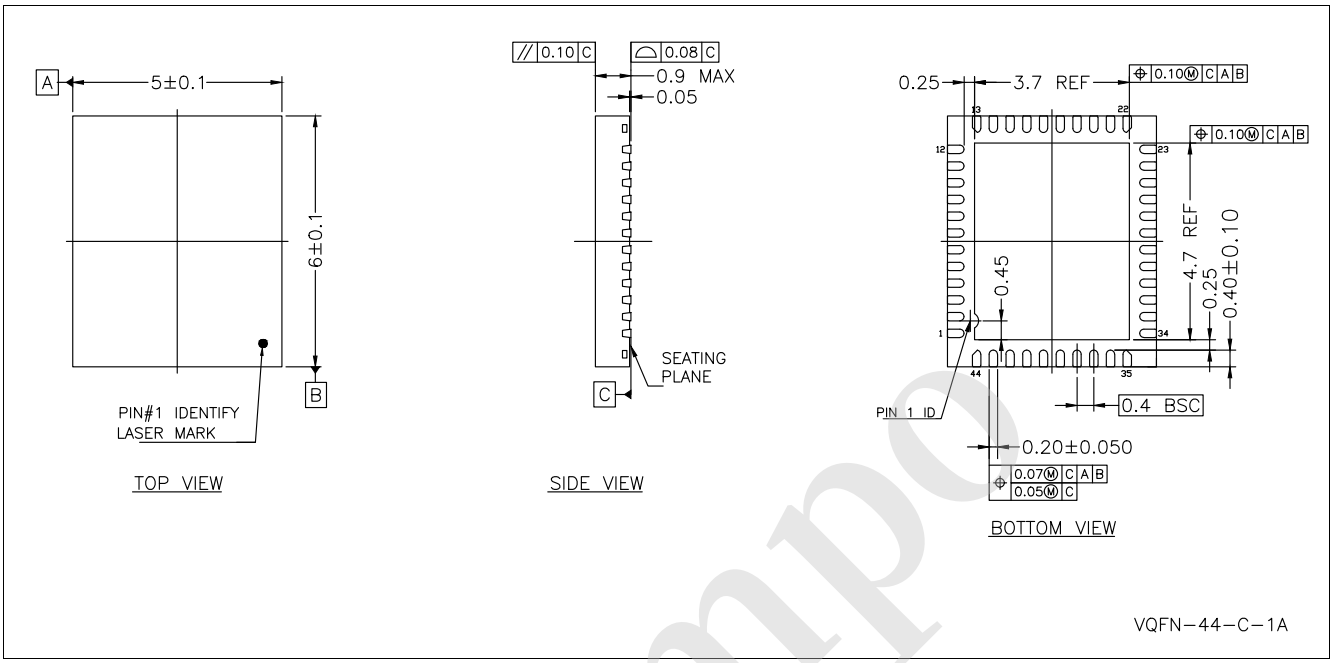


Figure 31 PG-VQFN-44 (Plastic Green Very Thin Quad Flat Non-leaded)

Dimensions are in mm.

Package description, package handling, PCB and board assembly information is available on request (refer to **[13]**).

9 Chip Identification and Ordering Information

Figure 32 shows an example of the marking pattern on a DXS101 device. The actual chip marking may differ slightly from the illustration.

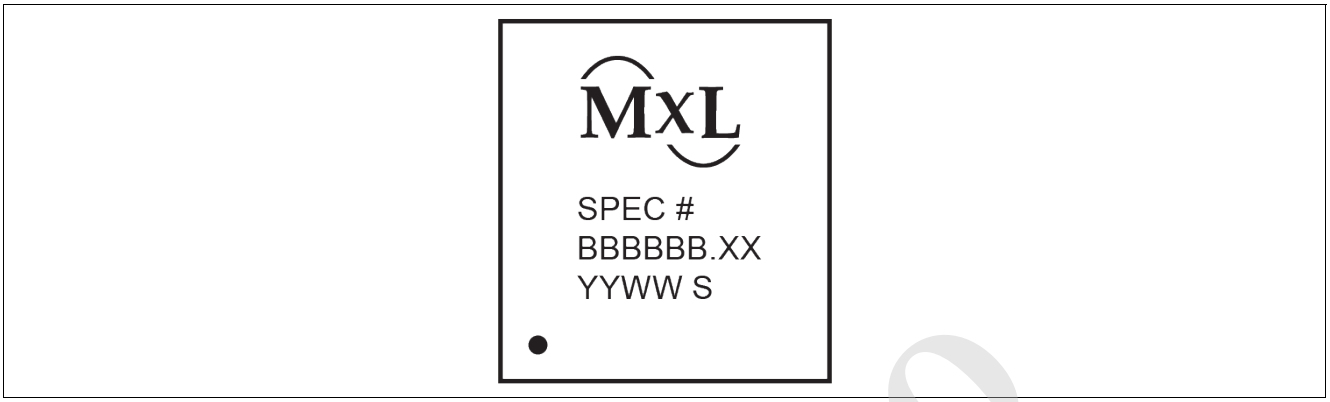


Figure 32 Example of Chip Marking

Table 44 explains the chip marking information and Table 45 provides chip ordering information.

Table 44 Chip Marking Pattern

Marking	Description
Text Line 1	MaxLinear Logo
Text Line 2	Spec. Number - Refer to Table 45
Text Line 3	Wafer Lot Number
Text Line 4	Date Code (YYWW) and Assembly Site Code (S)

Table 45 Product and Package Naming

Product Name	Ordering Code	S-Spec#	Package
DXS101	PEF32001VSV13	SLLX3	PG-VQFN-44
DXS101	PEF32001VSV12	SLLU3	PG-VQFN-44

Literature References

[1] Telephony Chipset for CPE DXS Series Product Brief Rev. 2.0

[2] DXS API Device Driver Programmer’s Reference Rev. 3.0

[3] DXS User's Manual System Description Rev. 2.2

[4] DXS102/DXS101 V1.2/V1.3 Data Sheet Rev. 2.0

[5] DXS System Package Release Notes

[6] DXS Series Tool Brief

[7] EASY 3200x/3100x DXS/DXC Evaluation Package Getting Started Rev. 5.0

[8] EASY 3200x/3200x DXS Evaluation Package Latest Information

[9] DXS Reference Board/Evaluation Board Documentation

[10] DXS Reference Design V1.2/V1.3 Release Note Rev. 2.0, including Reference Design Package

[11] DXS102/DXS101 V1.1/V1.2/V1.3 DC/DC Converter Externals Application Note Rev. 2.0

[12] DXS/DXC V1.2/V1.3 Protection Requirements Application Note Rev. 2.0

[13] P(G)-VQFN Packages PCB Assembly Recommendations Solution Guide Rev. 1.5

Attention: Please refer to the latest revision of these documents.

Standards References

[14] ANSI T1.401-2000, November 15, 2000, Network to Customer Installation Interfaces – Analog Voicegrade Switched Access Lines Using Loop-Start and Ground-Start Signaling.

[15] Bellcore, TR-TSY-000231-Generic Automated Loop Test Systems

[16] BT SIN 227, Issue 3.7, September 2015, Suppliers' Information Note: CALLING LINE IDENTIFICATION SERVICE, SERVICE DESCRIPTION

[17] ETSI EN 300 659-1, V1.3.1 (2001-01), European Standard (Telecommunications series), Access and Terminals (AT); Analogue access to the Public Switched Telephone Network (PSTN); Subscriber line protocol over the local loop for display (and related) services; Part 1: On-hook data transmission

[18] ITU-T Recommendation G.711, 1988, 1993, PULSE CODE MODULATION (PCM) OF VOICE FREQUENCIES: GENERAL ASPECTS OF DIGITAL TRANSMISSION SYSTEMS TERMINAL EQUIPMENTS

[19] ITU-T Recommendation Q.23, 1993, INTERNATIONAL AUTOMATIC AND SEMI-AUTOMATIC WORKING TECHNICAL FEATURES OF PUSH-BUTTON TELEPHONE SETS

[20] ITU-T Recommendation Q.24, 1988, 1993, INTERNATIONAL AUTOMATIC AND SEMI-AUTOMATIC WORKING MULTIFREQUENCY PUSH-BUTTON SIGNAL RECEPTION

[21] ITU-T Recommendation Q.552, (11/2001), Transmission characteristics at 2-wire analogue interfaces of digital exchanges

[22] ITU-T Recommendation V.23, 1993, 600/1200-BAUD MODEM STANDARDIZED FOR USE IN THE GENERAL SWITCHED TELEPHONE NETWORK

[23] NTT Technical Reference, TELEPHONE SERVICE INTERFACES Edition 5

[24] Telcordia Technologies Generic Requirements GR-30-CORE, Issue 2 December 1998, LSSGR: Voiceband Data Transmission Interface (FSD 05-01-0100) (A Module of LSSGR, FR-64)

[25] Telcordia Technologies GR-909-CORE Issue 2 December 2004, Generic Criteria for Fiber in the Loop Systems

[26] ESDA/JEDEC JDS-001-2012, ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level, January 2012

[27] JEDEC Standard JESD22-C101D, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components, December 2009