1. DESCRIPTION

The XL1000/XD1000 serves as a standalone CAN controller, designed for area network control in mobile applications as well as general industrial environments. Furthermore, it introduces a novel operational mode known as PeliCAN, which supports the CAN 2.0B protocol equipped with numerous enhanced features.

2. FEATURES

The XL1000/XD1000 CAN controller boasts a comprehensive feature set, including:

- Compatibility with the default BasicCAN mode
- An expanded 64-byte receive buffer (FIFO)
- Full compatibility with the CAN 2.0B protocol
- Support for both 11-bit and 29-bit identifiers
- Bit rates reaching up to 1Mbits/s

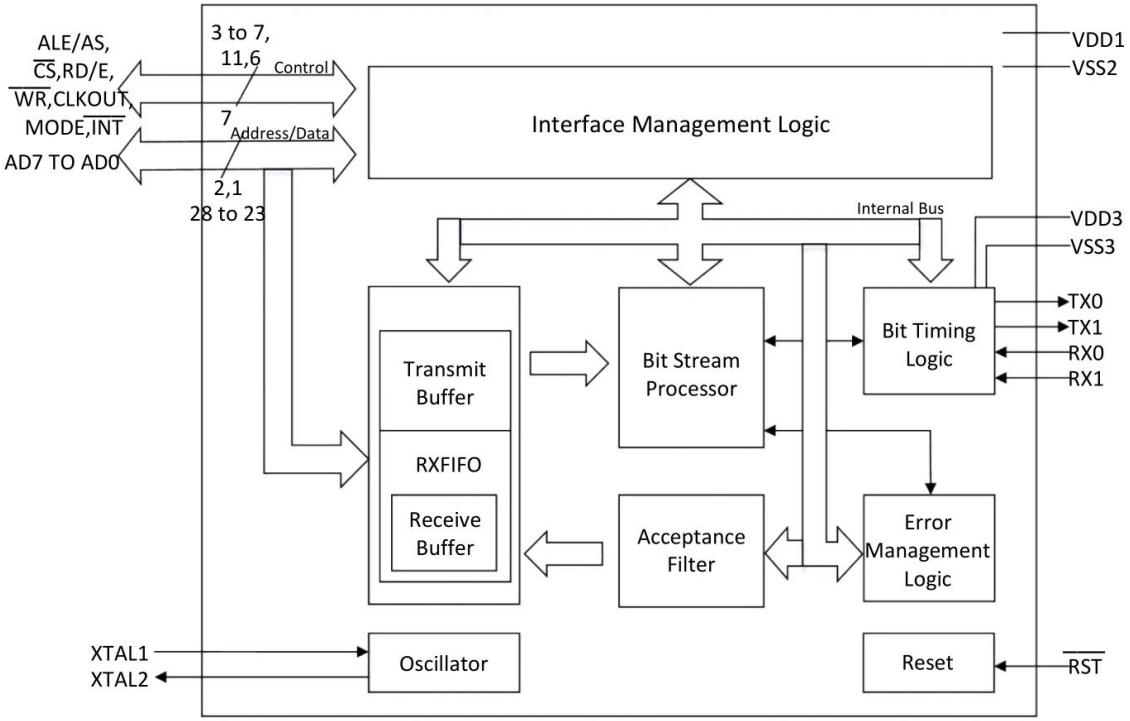
In its PeliCAN mode, it further extends its capabilities with:

- Read/write access to error counters
- Programmable error warning limits
- A register for the most recent error code
- Interrupts for every CAN bus error
- Detailed arbitration lost interrupt control through specific control bits
- Single shot transmission (without retransmission)
- Silent mode (no acknowledgment errors)
- Support for hot-plugging (software bit-rate detection)
- Expanded acceptance filter capabilities (4-byte code and 4-byte mask)
- Self-message reception (self-reception request)

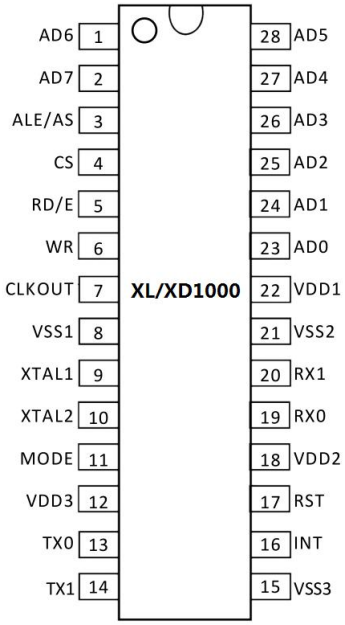
Additional features include:

- A 24MHz clock frequency
- Interfaces for multiple types of microprocessors
- Programmable CAN output driver configuration
- An operating temperature range of -40°C to +125°C

3. FUNCTIONAL BLOCK DIAGRAM



4. PIN CONFIGURATIONS AND FUNCTION



(TOP VIEW)

pin configuration		
Symbol	**Pin**	**Description**
AD7-AD0	2, 1, 28-23	Multiplexed Address/Data Bus
ALE/AS	3	ALE Input Signal (Intel Mode), AS Input Signal (Motorola Mode)
/CS	4	Chip Select Input, Low Level Enables Access to XL1000/XD1000
/RD /E	5	Microcontroller's /RD Signal (Intel Mode) or E Enable Signal (Motorola Mode)
/WR	6	Microcontroller's /WR Signal (Intel Mode) or (R/WR) Signal (Motorola Mode)
CLKOUT	7	Clock Output Signal Generated by XL1000/XD1000 for Microcontroller, Derived from Internal Oscillator and Programmable, Can Be Disabled by Clock Control Register's Clock Off Bit
VSS1	8	Ground
XTAL1	9	Input to Oscillator Amplifier Circuit, External Oscillator Signal Input (Note 1)
XTAL2	10	Oscillator Amplifier Circuit Output, Left Open Circuit Output When Using External Oscillator Signal (Note 1)
MODE	11	Mode Select Input 1 = Intel Mode 0 = Motorola Mode
VDD3	12	5V Voltage Source for Output Drivers
TX0	13	Output from CAN Output Driver 0 to Physical Line
TX1	14	Output from CAN Output Driver 1 to Physical Line
VSS3	15	Ground for Output Drivers
/INT	16	Interrupt Output for interrupting the microcontroller. /INT is active low when any of the internal interrupt register bits are set. /INT is an open-drain output and wired-OR with other /INTs in the system. A low level on this pin can activate the IC from sleep mode.
/RST	17	Reset Input for resetting the CAN interface (active low). Connect /RST pin to VSS through a capacitor and to VDD through a resistor for automatic power-on reset (e.g., C=1nF; R=50K).
VDD2	18	5V Voltage Source for Input Comparators
RX0 RX1	19,20	The input to the input comparator of XL1000/XD1000 from the physical CAN bus determines the control level, which will wake up XL1000/XD1000 from its sleep mode. If the level of RX1 is higher than that of RX0, the dominant control level is read. Conversely, if RX0 is higher, the recessive level is read. If the CBP bit in the Clock Prescaler Register is set, the CAN input comparator is bypassed to reduce internal delay, assuming an external transceiver circuitry is connected. In this scenario, only RX0 is active; the recessive level is considered high, while the dominant level is considered low.
VSS2	21	Ground for Input Comparators
VDD1	22	5V Voltage Source for Logic Circuits

Notes:1.The XTAL1 and XTAL2 pins must be connected to the VSS 1 through a capacitance of 15 pF.

5. LIMIT VALUE

Symbol	Parameter	Condition	Min	Max	Unit
VDD	Power Supply		-0.5	+6.5	V
II,IO	Input/Output Current of All Pins Except TX0 and TX1		-	±4	mA
IOT(sink)	Total Current Consumption by TX0 and TX1	Note1	-	30	mA
IOT(source)	Combined Source Current of TX0 and TX1	Note1	-	-20	mA
Tamb	Operating Ambient Temperature		-40	+125	℃
Tstg	Storage Temperature		-65	+150	℃
Ptot	Total Power Consumption		-	1.0	W
Vesd	Discharge of Each Pin	Note2	-1500	+1500	V
		Note4	-200	+200	V

Notes

1.During operation, IOT is a peak current with a width of t<100ms. The average output current of each TX does not exceed 10mA.
2.This value is based on the allowable maximum temperature and package thermal resistance, rather than the device power consumption.
3.Human Body Model: Equivalent to discharging a 100pF capacitor through a 1.5kΩ resistor.
4.Machine Model: Equivalent to discharging a 200pF capacitor through an RL circuit of 25Ω and positive 2.5μH.

6. DC CHARACTERISTICS

VDD = 5V (±10%); VSS = 0V; Tamb = -40°C to +125°C; All voltages are referenced to VSS unless otherwise specified.

Symbol	Parameter	Condition	Min	Max	Unit
Power Supply					
VDD	Voltage Source		4.5	5.5	V
IDD	Operating Current	fOSC=24MHz ;note 1		15	mA
Ism	Sleep Mode Current	Non-active state of oscillator note2		40	uA
Input					
VIL1	Low-Level Input on Pins ALE/AS/CS, (/RD)/E/WR, and MODE		-0.5	+0.8	V
VIL2	Low-Level Input Voltage on Pins XTAL1 and /INT			0.3 VDD	V
VIL3	Low-Level Input Voltage on Pins /RST, AD0-AD7, and RX0		-0.5	+0.6	V
VIH1	High-Level Input Voltage on Pins ALE/AS,/CS, (/RD)/E/WR, and MODE		2.0	VDD+0.5	V
VIH2	High-Level Input Voltage on Pins XTAL1 and /INT		0.7VDD		V
VIH3	High-Level Input Voltage on Pins /RST, AD0-AD7, and RX0		2.4	VDD+0.5	V
hy sRST	Input Hysteresis on Pins /RST, AD0-AD7, and RX0		500	-	mA
ILI	Leakage Current on Pins Except XTAL1, RX0, and RX1	0.45V<VI(D)<VDD;note3	-	±2	uA
Output					
VOL	Low-Level Output Voltage on Pins AD0-AD7, CLKOUT, and /INT	IOL=4Ma		0.4	V
VOH	High-Level Output Voltage on Pins AD0-AD7, CLKOUT, and /INT	IOH=-4mA	VDD-0.4		V
CAN Input Comparator					
Vth(I) (diff)	Differential Input Threshold Voltage	VDD=5V±10% ; 1.4V<VI(RX)<VDD-1.4V note 4 , 6		32	mV
Vhys	Hysteresis Voltage		8	30	mV
II	Input Current			±400	nA
CAN Output Driver					

VOL(TX)	Low-Level Input Voltage on Pins TX0 and TX1	VDD=5V 10% IO=1.2mA; note6 IO=10mA		0.05 0.4	V
VOH(TX)	High-Level Input Voltage on Pins TX0 and TX1	VDD=5V 10% IO=1.2mA; note6 IO=10mA	VDD-0.05 VDD-0.4		V

NOTES

1.AD0-AD7 = ALE = /RD = /WR = /CS = VDD; /RST = MODE = VSS; RX0 = 2.7V; RX1 = 2.3V; XTAL1 = 0.5V or VDD - 0.5V; All outputs are unloaded.
2.AD0-AD7 = ALE = /RD = /WR = /INT = /RST = /CS = MODE = RX0 = VDD; RX1 = XTAL1 = VSS; All outputs are unloaded.
3.VID = Input voltage at the data input pins.
4.VIRX = Input voltage at RX0 and RX1 pins.
5.Applies only when the comparator bypass mode is enabled.
6.Not tested during production.

7. AC CHARACTERISTIC

VDD = 5 V ± 10%; VSS = 0 V; CL = 50 pF (output pin); Tamb = -40~ + 125; unless otherwise noted; Note 1

Symbol	Parameter	Condition	Min	Max	Unit
fOSC	Oscillator Frequency			24	MHz
tSU(A-AL)	Address Setup Time for ALE/AS Low Level		8		ns
th(A-LA)	Hold Time with ALE Low		2		ns
tW(AL)	Pulse Width of ALE/AS		8		ns
tRLQV	/RD Low for Valid Output Data	Intel		50	ns
tEHQV	E High for Valid Output Data	Motorola		50	ns
tRHDZ	/RD High for Data Tri-state	Intel		30	ns
tELDZ	E Low for Data Tri-state	Motorola		30	ns
tDVWH	/WR High for Valid Input Data	Intel	8		ns
tWHDX	Data Hold Time after /WR High	Intel	8		ns
tWHLH	/WR High to Next ALE High		15		ns
tELAH	E Low to Next AS High	Motorola	15		ns
tsu(I)(D-EL)	Input Data Setup Time with E Low	Motorola	8		ns
th(I)(EL-D)	Input Data Hold Time with E Low	Motorola	8		ns
tLLWL	ALE Low to /WR Low	Intel	10		ns
tLLRL	ALE Low to /RD Low	Intel	10		ns
tLLEH	AS Low to E High	Motorola	10		ns
tsu(R-EH)	RD/(/WR) to E High Setup Time	Motorola	5		ns
tW(W)	/WR Pulse Width	Intel	20		ns
tW(R)	/RD Pulse Width	Intel	40		ns
tW(E)	E Pulse Width	Motorola	40		ns
tCLWL	/CS Low to /WR Low	Intel	0		ns
tCLRL	/CS Low to /RD Low	Intel	0		ns
tCLEH	/CS Low to E High	Motorola	0		ns
tWHCH	/WR High to /CS High	Intel	0		ns
tRHCH	/RD High to /CS High	Intel	0		ns
tELCH	E Low to /CS High	Motorola	0		ns
tW(RST)	/RST Pulse Width		100		ns
Input Comparator / Output Driver					
tSD	Sum of Input and Output Delays			40	ns

Notes

1. AC characteristics are not tested during production.
2. If an external transmit-receive circuit is used, the analog input comparator can be internally bypassed by setting the CBP bit in the clock prescaler register. This will reduce the delay (<26ns) for the input voltage VI(RX) at RX0 and RX1 pins.

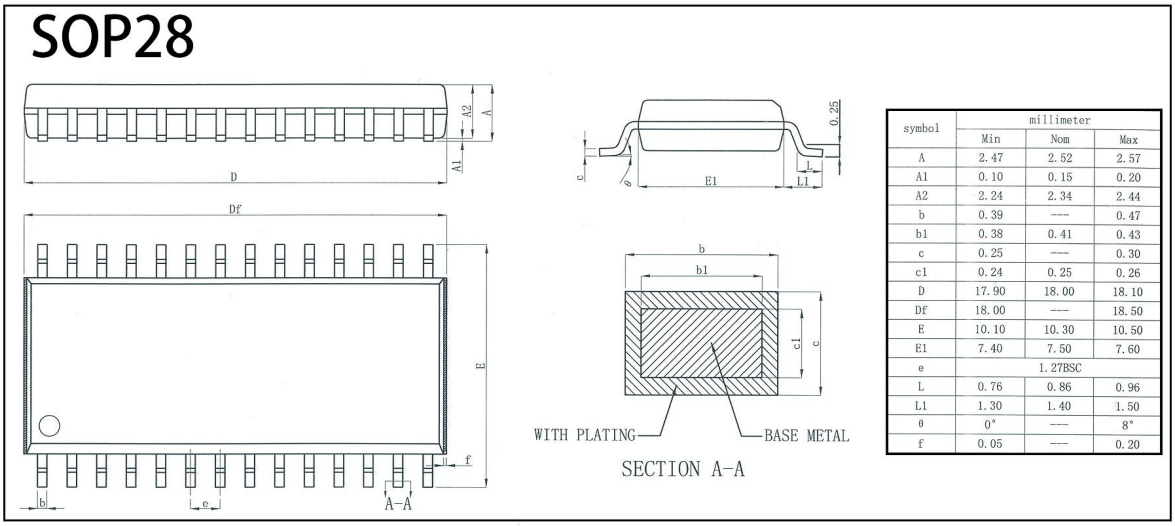
8. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL1000	XL1000	SOP28	18.25 * 7.50	- 0 to +70	MSL3	T&R	1000
XD1000	XD1000	DIP28	37.01 * 13.84	- 0 to +70	MSL3	T&R	260

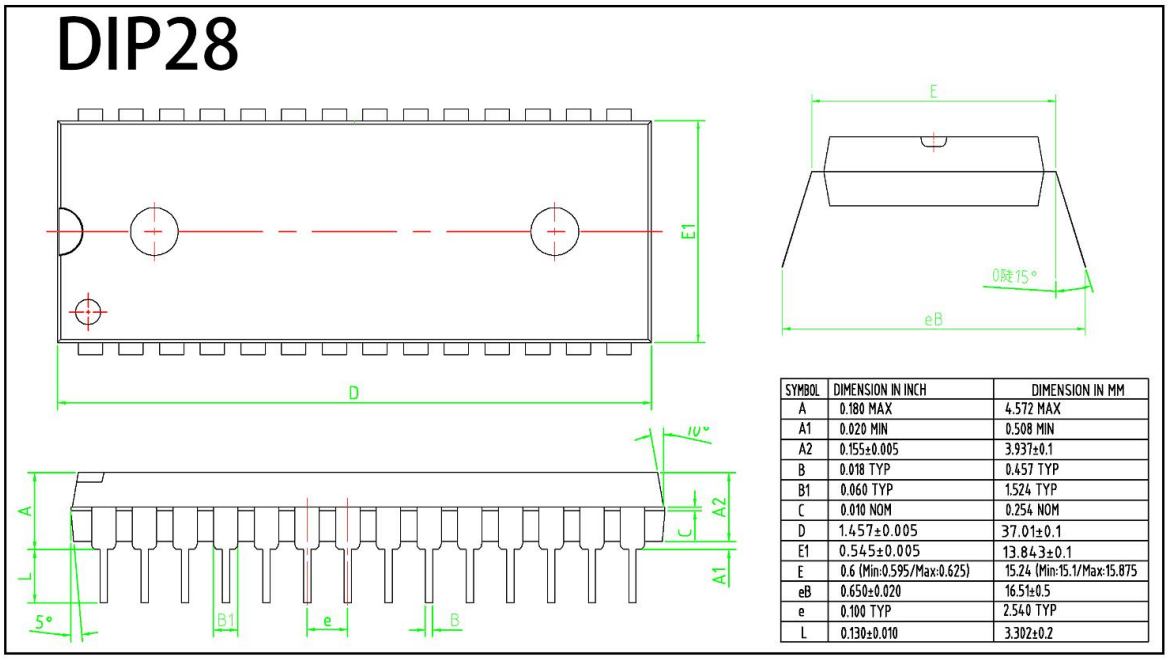
9. DIMENSIONAL DRAWINGS

SOP28



symbol	millimeter		
	Min	Nom	Max
A	2.47	2.52	2.57
A1	0.10	0.15	0.20
A2	2.24	2.34	2.44
b	0.39	---	0.47
b1	0.38	0.41	0.43
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	17.90	18.00	18.10
Df	18.00	---	18.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.76	0.86	0.96
L1	1.30	1.40	1.50
θ	0°	---	8°
f	0.05	---	0.20

DIP28



SYMBOL	DIMENSION IN INCH	DIMENSION IN MM
A	0.180 MAX	4.572 MAX
A1	0.020 MIN	0.508 MIN
A2	0.155±0.005	3.937±0.1
B	0.018 TYP	0.457 TYP
B1	0.060 TYP	1.524 TYP
C	0.010 NOM	0.254 NOM
D	1.457±0.005	37.01±0.1
E1	0.545±0.005	13.843±0.1
E	0.6 (Min:0.595/Max:0.625)	15.24 (Min:15.1/Max:15.875
eB	0.650±0.020	16.51±0.5
e	0.100 TYP	2.540 TYP
L	0.130±0.010	3.302±0.2