

# CAT24M01 M24M01 EEPROM Serial 1-Mb I<sup>2</sup>C Product Overview

Better Future.

For complete documentation, see the data sheet.

The M24M01/CAT24M01 is a EEPROM Serial 1-Mb I<sup>2</sup>C, internally organized as 131,072 words of 8 bits each.

It features a 256-byte page write buffer and supports the Standard (100 kHz), Fast (400 kHz) and Fast-Plus (1 MHz) I<sup>2</sup>C protocol.

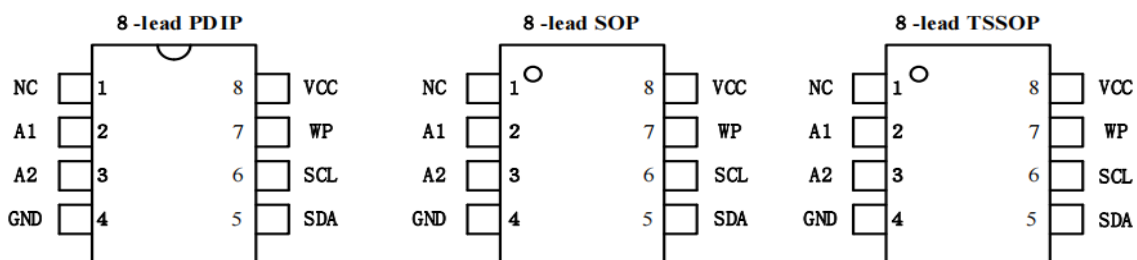
(this protects the entire memory).

External address pins make it possible to address up to four TDM24M01 devices on the same bus.

On-Chip ECC (Error Correction Code) makes the device suitable for high reliability applications.

## Features

- Supports Standard, Fast and Fast-Plus I<sup>2</sup>C Protocol
- 1.8 V to 5.5 V Supply Voltage Range
- 256-Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- 8-lead SOIC and TSSOP and 8-pad UDFN packages
- For more features, see the data sheet



## Pin Descriptions

Pin Name	Type	Functions
A1-A2	I	Address Inputs
SDA	I/O	Serial Data
SCL	I	Serial Clock Input
WP	I	Write Protect
GND	P	Ground
VCC	P	Power Supply

Table 1

M24M01/CAT24M01 1M bits (131,072x8)

## Examples

型号	封装	私印	工作电压	兼容电压
M24M01-RMN6TP-TUDI	SOP8	24M01R	1.8to 5.5	1.7V
CAT24M01WI-GT3-TUDI	SOP8	24M01WI	1.8to 5.5	
CAT24M01YI-GT3-TUDI	TSSOP8	24M01	1.8to 5.5	

Position	A	B	C
1	VCC	-	SDA
2	-	SCL	-
3	WP	-	A2
4	-	A1	-
5	NC	-	GND

Table 2

## Block Diagram

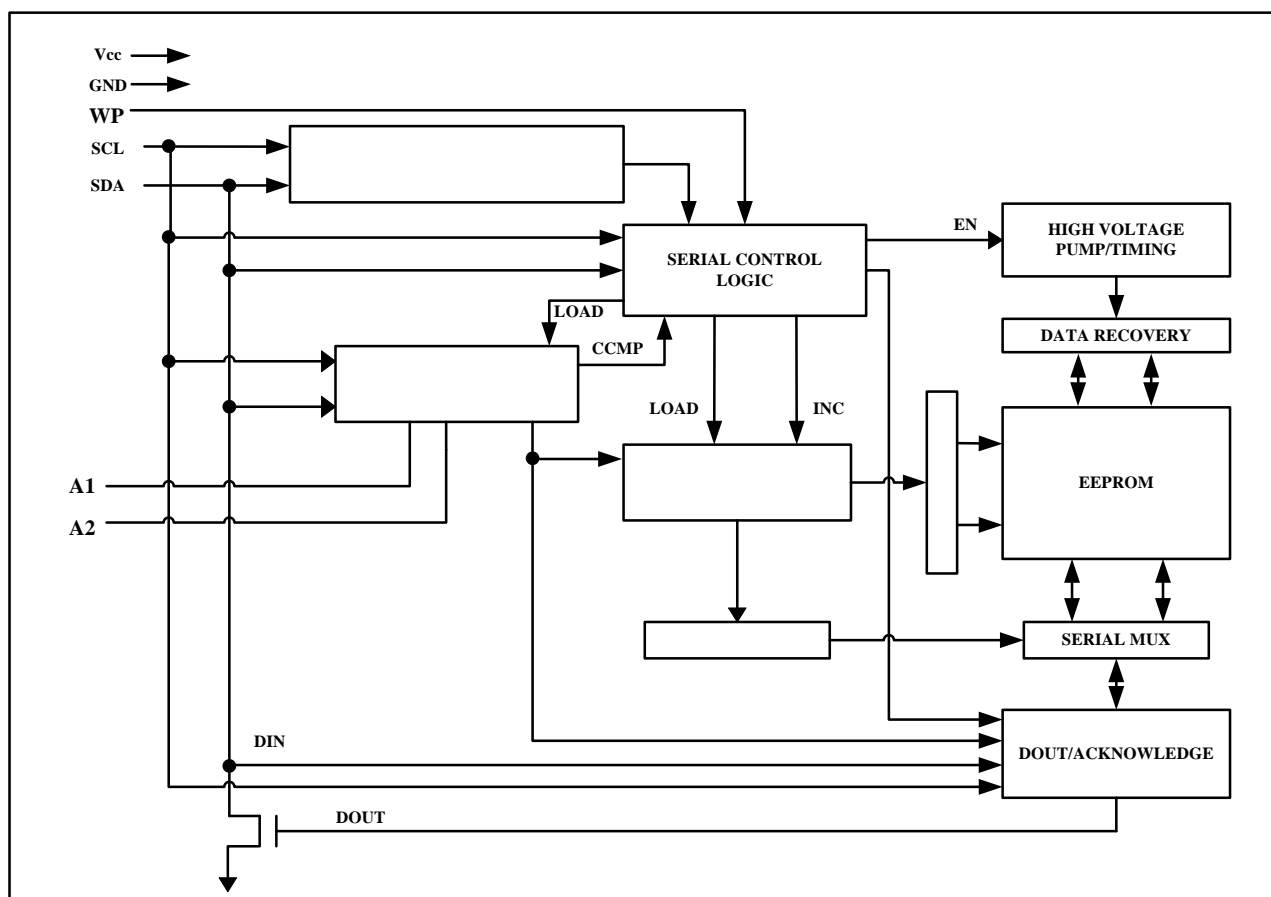


Figure 1

M24M01/CAT24M01 1M bits (131,072x8)

**DEVICE/PAGE ADDRESSES (A2 and A1):** The A2 and A1 pins are device address inputs that are hard wire for the 24M01. Four 1M devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

**SERIAL DATA (SDA):** The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

**SERIAL CLOCK (SCL):** The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

**WRITE PROTECT (WP):** The 24M01 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protection pin is connected to Vcc, the write protection feature is enabled and operates as shown in the following **Table 2**.

WP Pin Status	24M01
At VCC	Full(1024K)Array
At GND	Normal Read/Write Operations

Table 3

## Functional Description

### 1. Memory Organization

24M01, 1M SERIAL EEPROM: Internally organized with 512 pages of 256 bytes each, the 1M requires a 17-bit data word address for random word addressing.

### 2. Device Operation

**CLOCK and DATA TRANSITIONS:** The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see **Figure 2**). Data changes during SCL high periods will indicate a start or stop condition as defined below.

**START CONDITION:** A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see **Figure 3**).

**STOP CONDITION:** A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see **Figure 3**).

**ACKNOWLEDGE:** All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

**STANDBY MODE:** The 24M01 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

**MEMORY RESET:** After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Lock SDA high in each cycle while SCL is high.
3. Create a start condition and a stop condition.

M24M01/CAT24M01 1M bits (131,072x8)

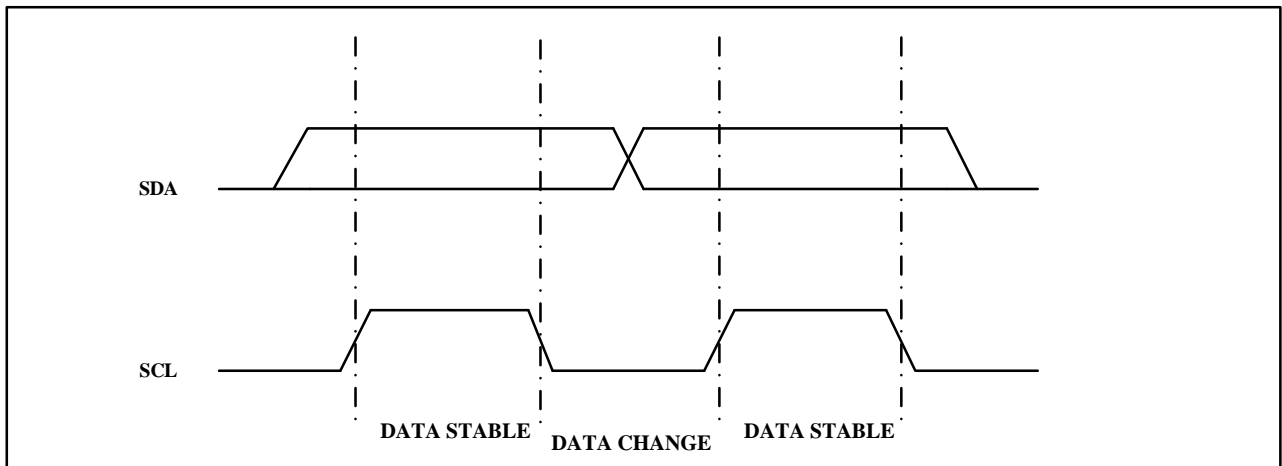


Figure 2. Data Validity

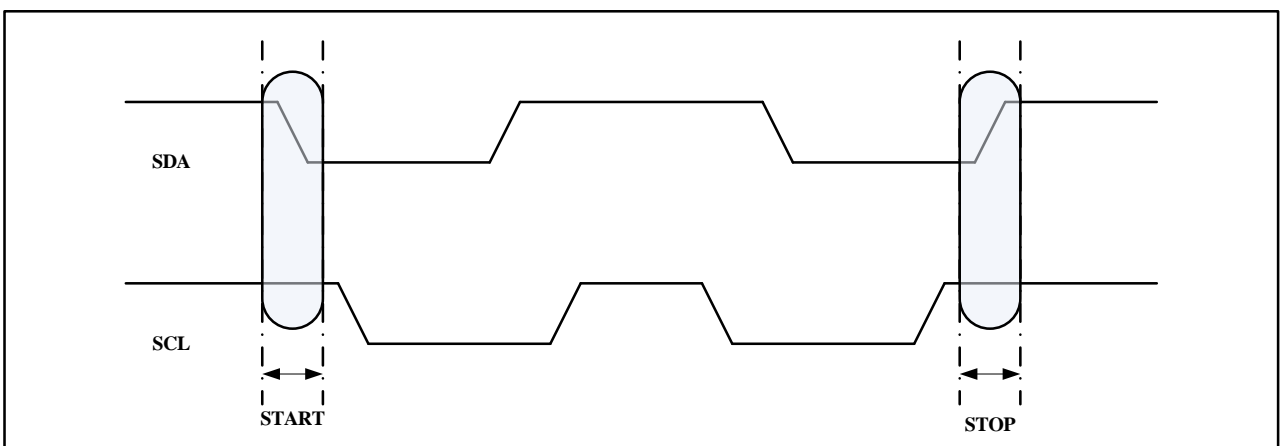


Figure 3. Start and Stop Definition

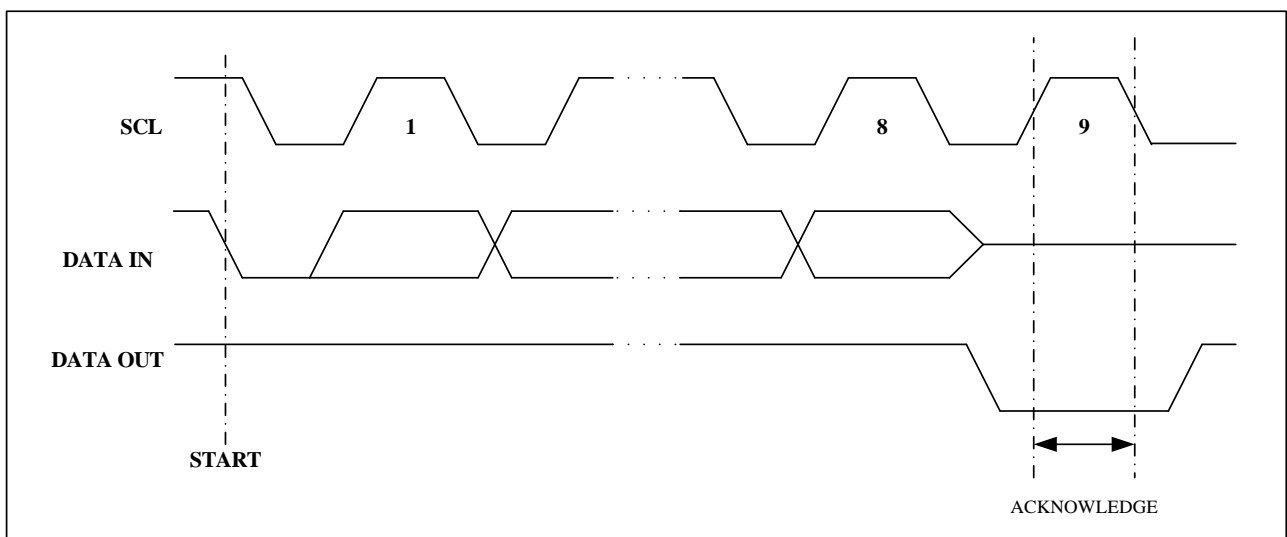


Figure 4. Output Acknowledge

M24M01/CAT24M01 1M bits (131,072x8)

### 3. Device Addressing

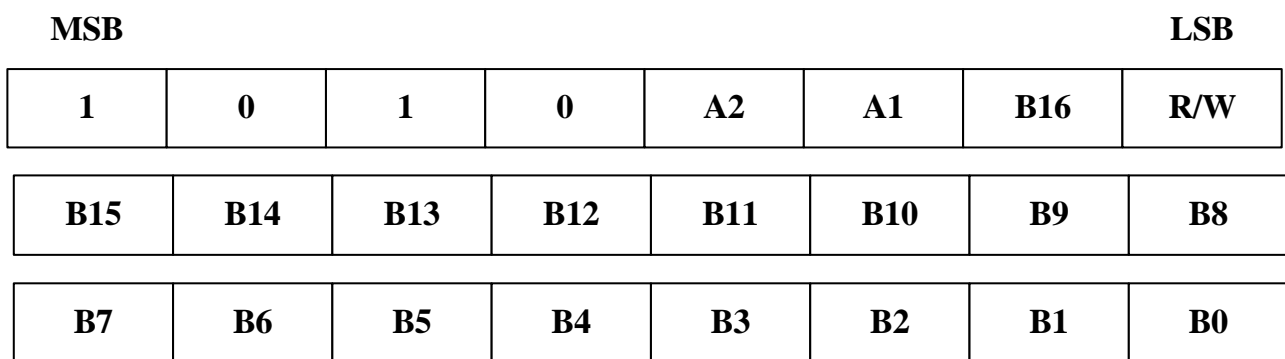
The 1M EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see **Figure 5**)

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 1M EEPROM uses A2 and A1 device address bits and one word address bit to allow as much as four devices on the same bus. These 2 device address bits must be compared to their corresponding hardwired input pins. The A2 and A1 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.



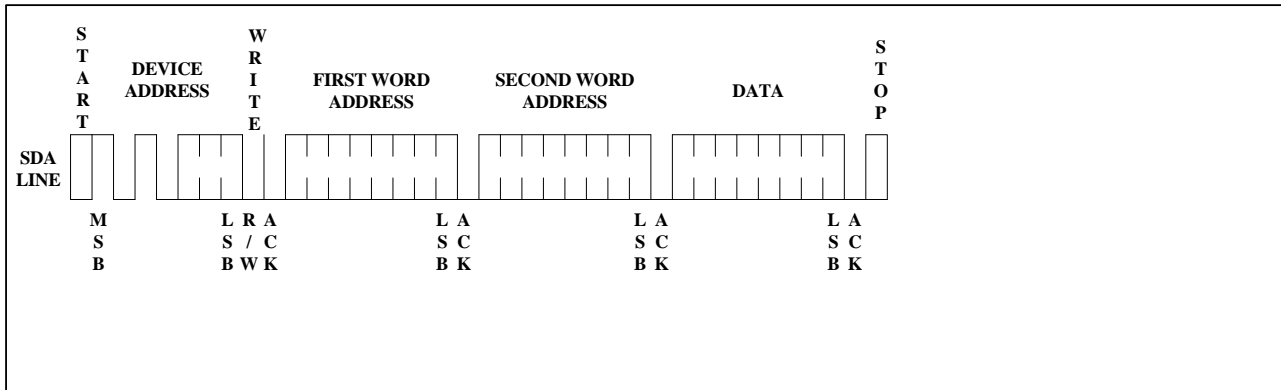
**Figure 5. Device Address and two 8-bit data word address**

**DATA SECURITY:** The 24M01 has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at VCC.

M24M01/CAT24M01 1M bits (131,072x8)

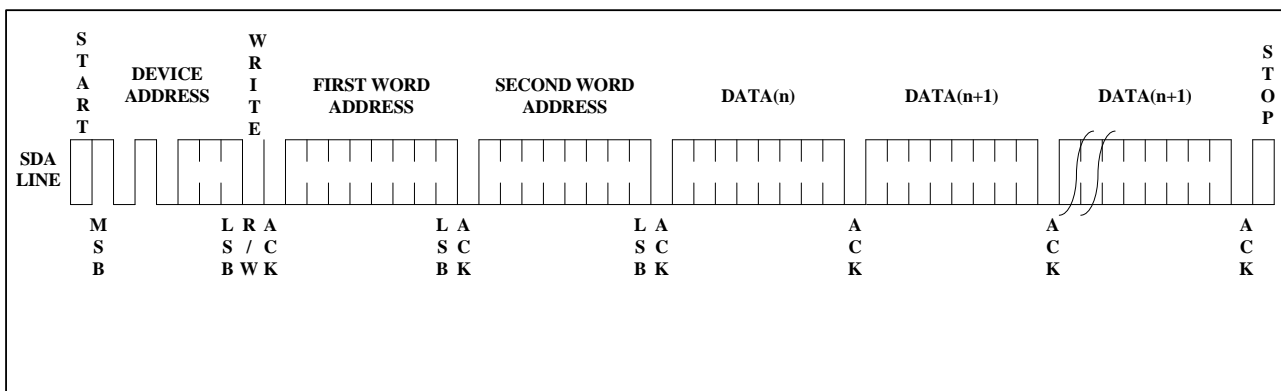
#### 4. Write Operations

**BYTE WRITE:** A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle,  $t_{WR}$ , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see **Figure 6**).



**Figure 6. Byte Write**

**PAGE WRITE:** The Page Write mode allows up to 256 bytes to be written in a single Write cycle. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 255 more data words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see **Figure 7**).



**Figure 7. Page Write**

The data word address lower eight bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 256 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

**WRITE IDENTIFICATION PAGE:** The Identification Page (256 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- MSB address bits B16/B8 are don't care except for address bit B10 which must be "0".  
LSB address bits B7/B0 define the byte address inside the Identification page.

M24M01/CAT24M01 1M bits (131,072x8)

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

**ACKNOWLEDGE POLLING:** Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

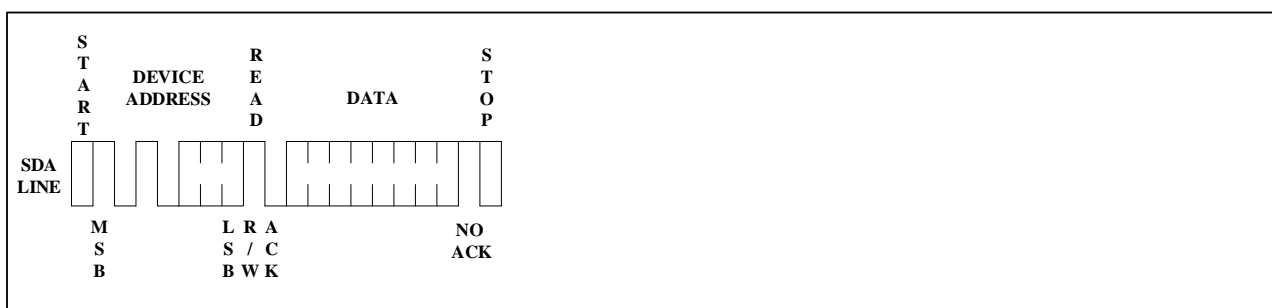
M24M01/CAT24M01 1M bits (131,072x8)

## 5. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

### CURRENT ADDRESS READ:

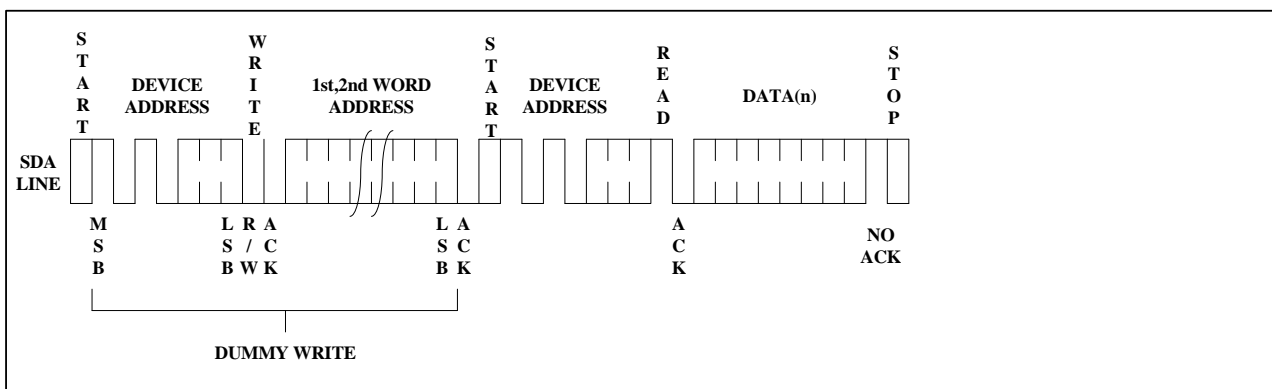
The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see **Figure 8**).



**Figure 8. Current Address Read**

### RANDOM READ:

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 9**).

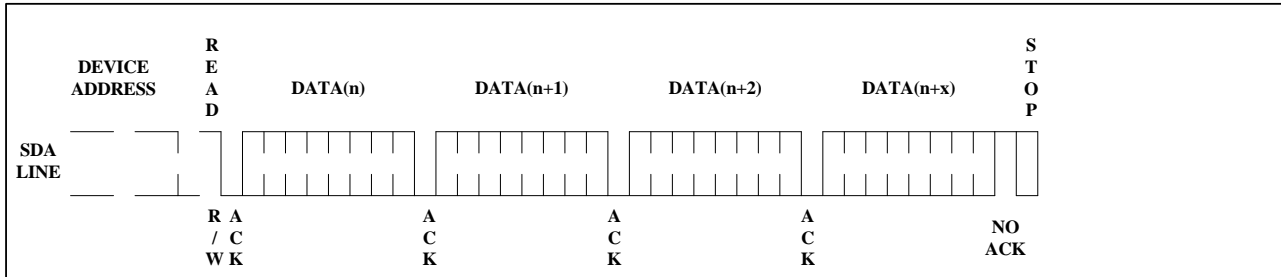


**Figure 9. Random Read**



M24M01/CAT24M01 1M bits (131,072x8)

**SEQUENTIAL READ:** Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 10**).



**Figure 10. Sequential Read**

**READ IDENTIFICATION PAGE:** The Identification Page (256 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

The Identification Page can be read by issuing an Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits B16/B8 are don't care, the LSB address bits B7/B0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g.: when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 246, as the ID page boundary is 256 bytes)

**LOCK IDENTIFICATION PAGE:** The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

Device type identifier = 1011b

Address bit B10 must be '1'; all other address bits are don't care

The data byte must be equal to the binary value xxxx xx1x, where x is don't care

M24M01/CAT24M01 1M bits (131,072x8)

## Electrical Characteristics

Absolute Maximum Stress Ratings:

- DC Supply Voltage . . . . . -0.3V to +6.5V
- Input / Output Voltage . . . . . GND-0.3V to VCC+0.3V
- Storage Temperature . . . . . -65°C to +150°C
- Electrostatic pulse (Human Body model) . . . . . 8000V

Comments:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

### DC Electrical Characteristics

Applicable over recommended operating range from (unless otherwise noted):

Parameter	Symbol	Min	Typ	Max	Unit	Condition
24M01	TA =-40°C to +85°C	VCC = +1.7V to +5.5V CL=100 pF				
24M01E1	TA =-40°C to +105°C					
24M01E0	TA =-40°C to +125°C					
Supply Voltage	VCC1	1.7	-	5.5	V	-
Supply Current VCC=5.0V	ICC1	-	0.26	0.5	mA	READ at 400KHZ
Supply Current VCC=5.0V	ICC2	-	0.28	0.5	mA	WRITE at 400KHZ
Supply Current VCC=5.0V	ISB1	-	0.03	0.5	μA	VIN=VCC or VSS
Input Leakage Current	IL1	-	0.10	1.0	μA	VIN=VCC or VSS
Output Leakage Current	ILO	-	0.05	1.0	μA	VOUT=VCC or VSS
Input Low Level	VIL1	-0.3	-	VCCx0.3	V	VCC=1.7V to 5.5V
Input High Level	VIH1	VCCx0.7	-	VCC+0.3	V	VCC=1.7V to 5.5V
Output Low Level VCC=1.7V	VOL1	-	-	0.2	V	IOL=2.1mA
Output Low Level VCC=5.0V	VOL2	-	-	0.4	V	IOL=3.0mA

Table 4

### Pin Capacitance

Applicable over recommended operating range from TA = 25°C, f =1MHz, VCC = +5.0V

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input/Output Capacitance(SDA)	C <sub>IO</sub>	-	-	8	pF	V <sub>IO</sub> =0V
Input Capacitance(A1,A2,SCL)	C <sub>IN</sub>	-	-	6	pF	V <sub>IN</sub> =0V

Table 5

M24M01/CAT24M01 1M bits (131,072x8)

### AC Electrical Characteristics

Applicable over recommended operating range from (unless otherwise noted):

Parameter	Symbol	1.7V ≤ VCC < 2.5V			2.5V ≤ VCC < 5.5V			Units
		Min	Typ	Max	Min	Typ	Max	
24M01	TA = -40°C to +85°C	VCC = +1.7V to +5.5V CL=100 pF						
24M01E1	TA = -40°C to +105°C							
24M01E0	TA = -40°C to +125°C							
Clock Frequency, SCL	fSCL	-	-	400	-	-	1000	kHZ
Clock Pulse Width Low	tLOW	1.3	-	-	0.5	-	-	μs
Clock Pulse Width High	tHIGH	0.6	-	-	0.26	-	-	μs
Noise Suppression Time	tl	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	tAA	-	-	0.9	-	-	0.45	μs
Time the bus must be free before a new transmission can start	tBUF	1.3	-	-	0.5	-	-	μs
Start Hold Time	tHD:STA	0.6	-	-	0.25	-	-	μs
Start Setup Time	tSU:STA	0.6	-	-	0.25	-	-	μs
Data In Hold Time	tHD:DAT	0	-	-	0	-	-	μs
Data in Setup Time	tSU:DAT	100	-	-	100	-	-	ns
Input Rise Time(1)	tR	-	-	0.3	-	-	0.12	μs
Input Fall Time(1)	tF	-	-	0.3	-	-	0.12	μs
Stop Setup Time	tSu:STO	0.6	-	-	0.25	-	-	μs
Data Out Hold Time	tDH	50	-	-	50	-	-	ns
Write Cycle Time	tWR	-	3.5	5	-	3.5	5	ms
5.0V, 25°C, Byte Mode(1)	Endurance	4M	-	-	4M	-	-	Write Cycle

Table 6

Notes:

1. This parameter is characterized and is not 100% tested.
2. AC measurement conditions:  
 RL (connects to VCC): 1.3 k  
 Input pulse voltages: 0.3 VCC to 0.7 VCC  
 Input rise and fall time: 50 ns  
 Input and output timing reference voltages: 0.5 VCC  
 The value of RL should be concerned according to the actual loading on the user's system.

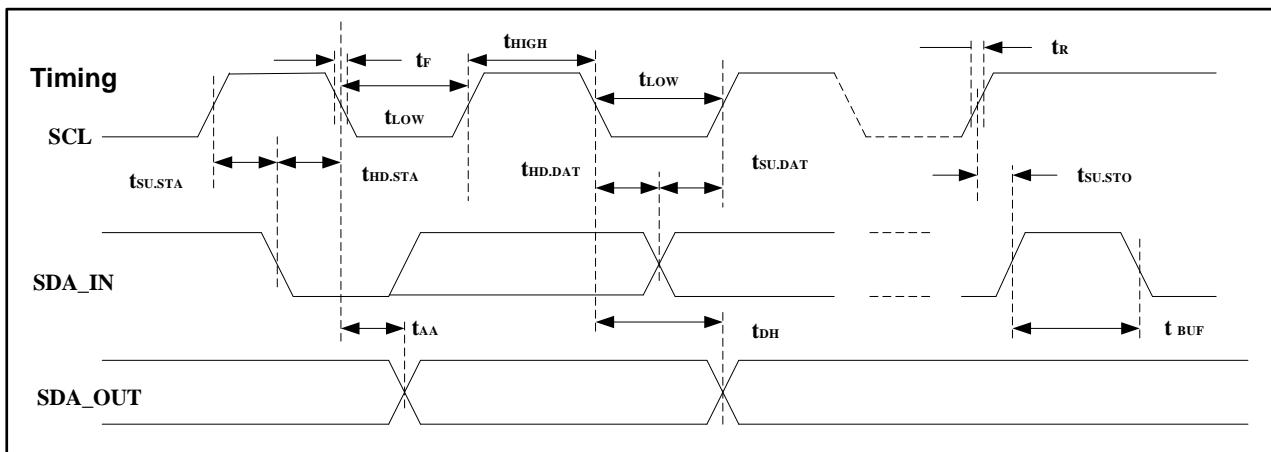


Figure 11. SCL: Serial Clock, SDA: Serial Data I/O

Write Cycle Timing

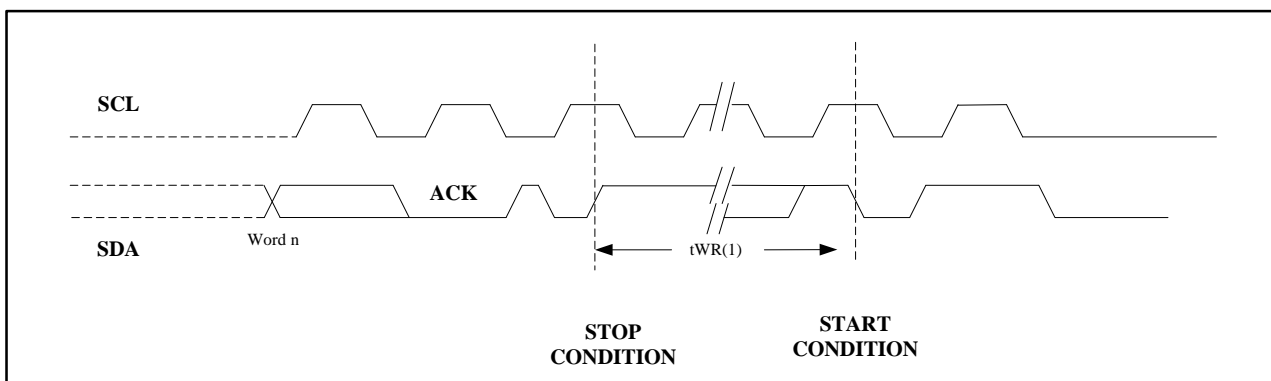
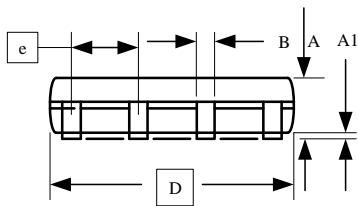
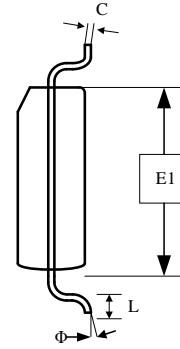
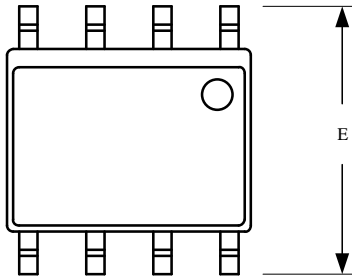


Figure 12. SCL: Serial Clock, SDA: Serial Data I/O

Notes:

The write cycle time  $t_{WR}$  is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

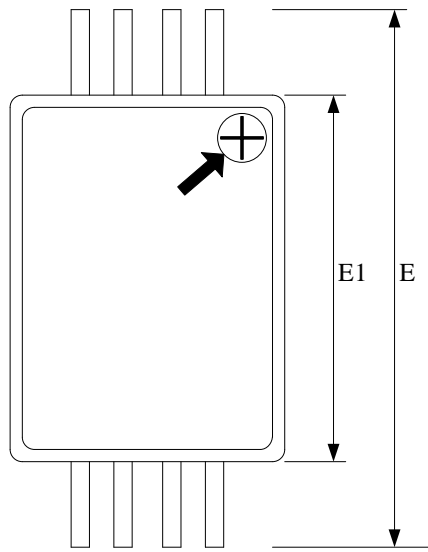
**Information**



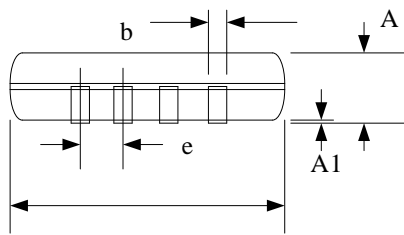
**COMMON DIMENSIONS**  
 (Unit of Measure=mm)

SYMBOL	MIN	NOM	MAX
A	1.35	-	1.75
A1	0.10	-	0.23
B	0.39	-	0.48
C	0.21	-	0.26
D	4.70	4.90	5.10
E1	3.70	3.90	4.10
E	5.80	6.00	6.20
e	1.27BSC		
L	0.50	-	0.80
Φ	0"	-	8"

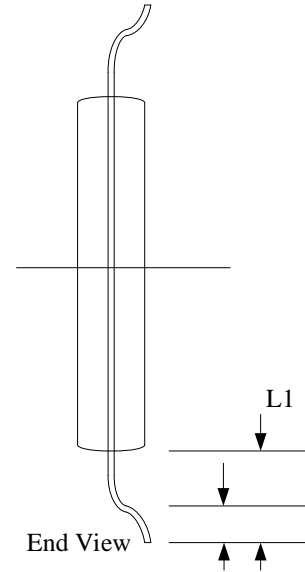
24M01 1M bits 131,072×8

**TSSOP**


Top View



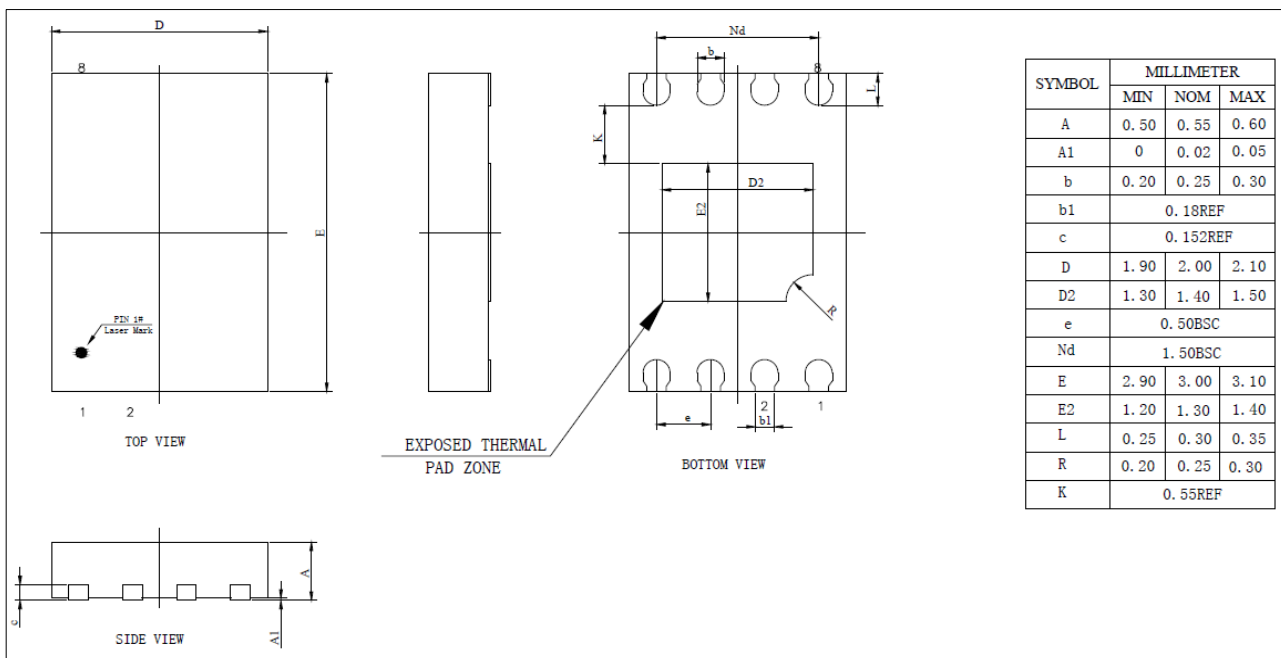
Side View



End View

**COMMON DIMENSIONS**  
Unit of Measure=mm

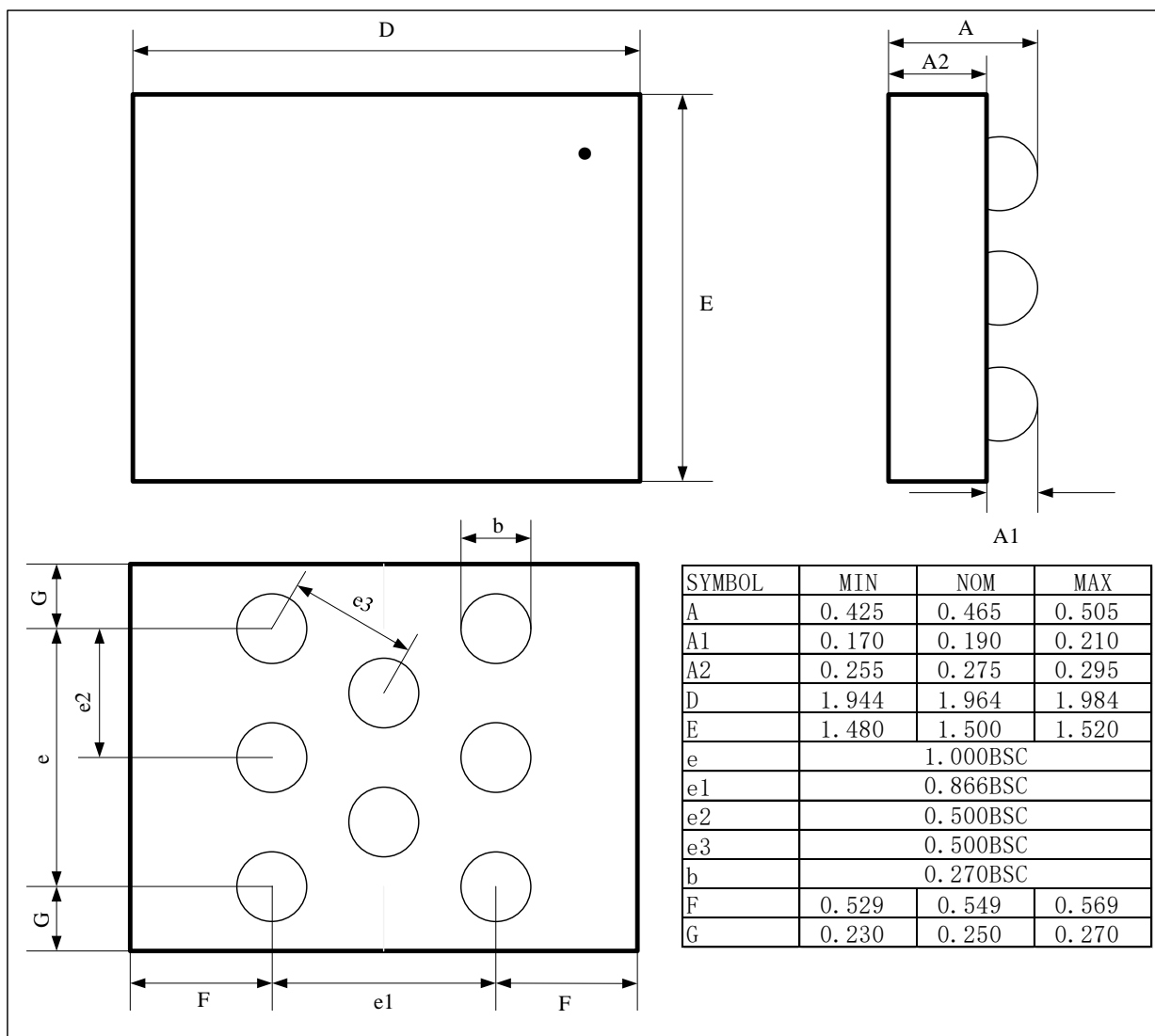
SYMBOL	MIN	NOM	MAX
D	2.90	3.00	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
A	-	-	1.20
A1	0.05	-	0.15
b	0.21	-	0.30
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		

**M24M01/CAT24M01**  
**1M bits (131,072x8)**  
**UDFN**

**重要通知与免责声明**

深圳市钲地半导体有限公司将准确可靠地提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、WEB工具、安全信息和其他资源，但不保证任何缺陷，一切以实物测试为准，并且不作任何明示或暗示的保证，包括但不限于对适销性的暗示保证、对特定目的适用的暗示保证或不侵犯任何第三方知识产权的暗示保证。

这些资源旨在为使用钲地产品的熟练开发人员提供支持：（1）为您的应用程序选择合适的产品；（2）设计、验证和测试您的应用程序；（3）确保您的应用程序符合适用的标准和任何其他安全、安保或其他要求；（4）钲地和钲地标志是钲地半导体的注册商标。所有商标均为其各自所有者的财产；（5）有关更改详情，请查阅任何修订文件中包含的修订历史记录。资源可能会在不通知的情况下更改。我公司将不对使用此产品及其使用而导致的专利或第三方知识产权的侵权负责。

## WLCSP



## WLCSP

### 重要通知与免责声明

深圳市钰地半导体有限公司将准确可靠地提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、WEB工具、安全信息和其他资源，但不保证任何缺陷，一切以实物测试为准，并且不作任何明示或暗示的保证，包括但不限于对适销性的暗示保证、对特定目的适用的暗示保证或不侵犯任何第三方知识产权的暗示保证。

这些资源旨在为使用钰地产品的熟练开发人员提供支持：（1）为您的应用程序选择合适的产品；（2）设计、验证和测试您的应用程序；（3）确保您的应用程序符合适用的标准和任何其他安全、安保或其他要求；（4）钰地和钰地标志是钰地半导体的注册商标。所有商标均为其各自所有者的财产；（5）有关更改详情，请查阅任何修订文件中包含的修订历史记录。资源可能会在不通知的情况下更改。我公司将不对使用此产品及其使用而导致的专利或第三方知识产权的侵权负责。