MSKSEMI 美森科







TVC



TSS



MOV



GDT



PIFF

ET3157-MS

Product specification





General Description

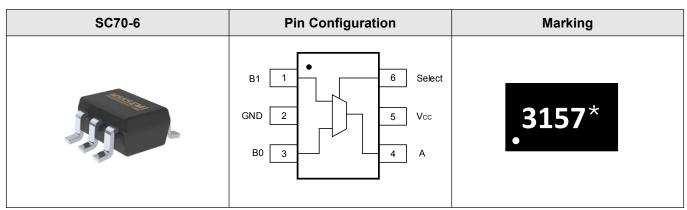
The ET3157-MS is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. It achieves very low propagation delay while maintaining CMOS low power dissipation. Analog and digital voltages that may vary across the full power–supply range (from Vcc to GND).

The Select pin has over voltage protection that allows voltages above Vcc, up to 7.0 V to be present on the pin without damage or disruption of operation of the part, regardless of the operating voltage.

Features

- Low power dissipation
- High speed
- Standard CMOS logic levels
- High bandwidth, improved linearity
- Switches Standard NTSC/PAL Video, Audio, SPDIF and HDTV
- be used for Clock Switching, Data Mux'ing,etc.
- Low RDSON
- Break Before Make Circuitry, Prevents Inadvertent Shorts
- Operating temperature -55 ℃~ +125 ℃
- package : SC70-6

Pinning and Marking



Pin Description

Pin	I/O	Pin Function
A, B ₀ , B ₁	I/O	Data port
Select	I	Controlling choice
Vcc	1	Power supply port
GND	1	Ground

FUNCTIONS DESCRIPTION

Select input port	Function
L	B ₀ Connected to A
Н	B ₁ Connected to A



Order information

Orderable Device	Package	Packing Option
ET3157-MS	SC70-6	3000PCS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V _{cc}	-0.5 -+7.0	V
DC Switch Voltage (1)	Vs	-0.5-V _{CC} +0.5	V
DC Input Voltage (1)	V _{IN}	-0.5 -+7.0	V
DC Input Diode Current @ V _{IN} < 0 V	I _{IK}	-50	mA
DC Output Current	lout	128	mA
DC V _{CC} or Ground Current	Icc/I _{GND}	100	mA
Storage Temperature Range	Tstg	-65 -+150	°C
Junction Temperature Under Bias	TJ	150	°C
Junction Lead Temperature (Soldering, 10 Seconds)	TL	260	°C
Power Dissipation @ +85°C	P _D	180	mW

NOTE:

Stresses beyond those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. QCSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

QCSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact sales office to get the latest datasheet.

RECOMMENDED OPERATING CONDITIONS (2)

Cha	Symbol	Min	Max	Unit		
Supply Voltage Operating	V _{cc}	1.65	5.5	V		
Select Input Voltage	V _{IN}	0	Vcc	٧		
Switch Input Voltage	V _{IN}	0	V _{CC}	V		
Output Voltage	V _{OUT}	0	V _{CC}	V		
Operating Temperature		T _A	-55	+125	$^{\circ}\!\mathbb{C}$	
Input Rise and Fall Time	Control Input V _{CC} = 2.3 V ~ 3.6 V	tr tf	0	10	A /	
	Control Input V _{CC} = 4.5 V ~ 5.5 V	tr,tf	0	5.0	ns/V	

Note:

2. Select input must be held HIGH or LOW, it must not float



ELECTRICAL CHARACTERISTICS

				-	Γ _A = 25°	<u> </u>	T _A = -40°	℃ ~ +85℃		
Symbol	Parameter	Test Conditions	V _{cc}	Min	Тур	Max	Min	Max	Unit	
DC ELECTRICAL CHARACTERISTICS										
			1.65 ~ 1.95				0.75Vcc			
V_{IH}	High Level Input		2.3 ~ 2.8				1.5		V	
▼ IH	Voltage		3 ~ 4.2				2.4			
			4.5 ~ 5.5				0.6Vcc			
	l and anal band		1.65 ~ 1.95					0.25V _{CC}		
V_{IL}	Low Level Input Voltage		2.3 ~ 2.8					0.4	V	
	3.		3 ~ 5.5					0.3Vcc		
I _{IN}	Input Leakage Current	0 < V _{IN} < 5.5 V	0 ~ 5.5		±0.05	±0.1		±1	μA	
I _{OFF}	OFF State Leakage Current	0 < A, B < Vcc	1.65 ~ 5.5		±0.05	±0.1		±1	μA	
I _{cc}	Quiescent Supply	V _{IN} = Vcc or GND I _{OUT} = 0	5.5			1.0		10	μA	
	Analog Signal Range		V _{cc}	0		V _{CC}	0	V _{CC}	V	
		V _{IN} = 0 V, I _O = 30 mA			3.0			7.0	Ω	
		$V_{IN} = 2.4 \text{ V},$ $I_{O} = -30 \text{ mA}$	4.5		5.0			12	Ω	
		$V_{IN} = 4.5 \text{ V},$ $I_{O} = -30 \text{ mA}$			7.0			15	Ω	
		$V_{IN} = 0 \text{ V},$ $I_{O} = 24 \text{ mA}$	3.0		4.0			9.0	Ω	
R_{ON}	Switch On Resistance ⁽³⁾	$V_{IN} = 3 V$, $I_{O} = -24 \text{ mA}$	3.0		10			20	Ω	
		$V_{IN} = 0 V$, $I_O = 8 \text{ mA}$	2.3		5.0			12	Ω	
		$V_{IN} = 2.3 \text{ V},$ $I_{O} = -8 \text{ mA}$	2.0		13			30	Ω	
		V _{IN} =0V, I _O =4 mA			6.5			20	Ω	
		V _{IN} = 1.65 V, I _O = -4 mA	1.65		17			50	Ω	
Б	On Resistance		4.5					25	Ω	
R _{RANGE}	Over Signal Range ⁽³⁾⁽⁷⁾	$I_A = -24 \text{ mA}$ $0 \le V_{Bn} \le V_{CC}$	3					50	Ω	



ELECTRICAL CHARACTERISTICS (continued)

Or made al	Damamatan	Took Constitions	V	•	T _A = 25°	С	T _A = -40°	℃ ~ +85℃	Unit
Symbol	Parameter	Test Conditions	V _{cc}	Min	Тур	Max	Min	Max	
R _{RANGE}	On Resistance RANGE Over Signal	$I_A = -8 \text{ mA}$ $0 \le V_{Bn} \le V_{CC}$	2.3					100	Ω
RANGE	Range ⁽³⁾⁽⁷⁾	$I_{A} = -4 \text{ mA}$ $0 \le V_{Bn} \le V_{CC}$	1.65					300	Ω
		I _A = -30 mA V _{Bn} = 3.15	4.5		0.15				Ω
ΔR_{ON}	On Resistance	I _A = -24 mA V _{Bn} = 2.1	3		0.2				Ω
ΔΙΚΟΝ	Match Between Channels (3)(4)(5)	I _A = -8 mA V _{Bn} = 1.6	2.3		0.5				Ω
		I _A = -4 mA V _{Bn} = 1.15	1.65		0.5				Ω
		$I_A = -30 \text{ mA}$ $0 \le V_{Bn} \le V_{CC}$	5		6.0				Ω
B	On Resistance	$I_A = -24 \text{ mA}$ $0 \le V_{Bn} \le V_{CC}$	3.3		12				Ω
R _{FLAT}	Flatness ⁽³⁾⁽⁴⁾⁽⁶⁾	$I_A = -8 \text{ mA}$ $0 \le V_{Bn} \le V_{CC}$	2.5		28				Ω
		$I_A = -4 \text{ mA}$ $0 \le V_{Bn} \le V_{CC}$	1.8		125				Ω
AC ELECT	TRICAL CHARAC	TERISTICS							
			1.65 ~ 1.95						nS
t _{PHL}	Propagation	Figure 1	2.3 ~ 2.7					1.2	nS
t _{PLH}	Delay Bus to Bus (8)	V _I = OPEN	3.0 ~ 3.5					0.8	nS
			4.5 ~ 5.5					0.3	nS
	Output Enable	Figure 1	1.65 ~ 1.95			23	7.0	24	nS
t _{PZL}	Time,	$V_1 = 2*V_{CC}$ for	2.3 ~ 2.7			13	3.5	14	nS
t _{PZH}	Turn On Time (A to Bn)	$t_{PZL}, V_I = 0 V \text{ for}$	3.0 ~ 3.5			6.9	2.5	7.6	nS
	(A to Bil)	t _{PZH}	4.5 ~ 5.5			5.2	1.7	5.7	nS
	0.44.5:	Fig. 4	1.65 ~ 1.95			12.5	3.0	13	nS
t _{PLZ}	Output Disable Time, Turn Off	Figure 1 $V_1 = 2*V_{CC}$ for	2.3 ~ 2.7			7.0	2.0	7.5	nS
t _{PHZ}	Time (A Port	t_{PLZ} , $V_I = 0$ V for	3.0 ~ 3.5			5.0	1.5	5.3	nS
	to B Port)	t _{PHZ}	4.5 ~ 5.5			3.5	0.8	3.8	nS



ELECTRICAL CHARACTERISTICS (continued)

Camela a l	Donomatan	Toot Conditions	V	1	_ _A = 25°0	2	T _A = -40℃	~ +85℃	Unit
Symbol	Parameter	Test Conditions	V _{cc}	Min	Тур	Max	Min	Max	Offic
			1.65 ~ 1.95				0.5		nS
4	Break Before	Figure2 ,	2.3 ~ 2.7				0.5		nS
t _{B-M}	Make Time (7)	$C_L = 50 \text{ pF}$, $R_L = 600 \Omega$	3.0 ~ 3.5				0.5		nS
		R _L = 600 Ω	4.5 ~ 5.5				0.5		nS
	Charge Injection	Figure 3, $C_L = 0.1 \text{ nF}$,	5.0		7.0				рС
Q	(7)	$V_{GEN} = 0 V$, $R_{GEN} = 0 \Omega$	3.3		3.0				рС
OIRR	Off Isolation (9)	Figure 4, $R_L = 50 \Omega$, f = 10MHz	1.65 ~ 5.5		-57				dB
Xtalk	Crosstalk	Figure 5, R_L = 50 Ω , f = 10MHz	1.65 ~ 5.5		-54				dB
BW	-3 dB Bandwidth	Figure 8, $R_L = 50 \Omega$	1.65 ~ 5.5		350M				Hz
THD	Total Harmonic Distortion (7)	$R_L = 600 \Omega,$ $0.5V_{P-P}$ $f = 600 Hz \sim 20$ kHz	5.0		0.011				%
C_{IN}	Select Pin Input Capacitance (10)		0		2.3				pF
C _{IO-B}	B Port Off Capacitance (10)	Figure 6	5.0		5.0				pF
C _{IOA-ON}	A Port Capacitance when Switch is Enabled (10)	Figure 7	5.0		15.5				pF



Note:

- 3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).
- 4. Parameter is characterized but not tested in production.
- 5. $\Delta R_{ON} = R_{ON} \text{ max} R_{ON} \text{ min measured at identical } V_{CC}$, temperature and voltage levels.
- 6. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
- 7. Guaranteed by Design.
- 8. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).
- 9. Off Isolation = 20 log10 $[V_A/V_{Bn}]$.
- 10. $T_A = +25$ °C, f = 1 MHz, Capacitance is characterized but not tested in production.

TEST CIRCUITS

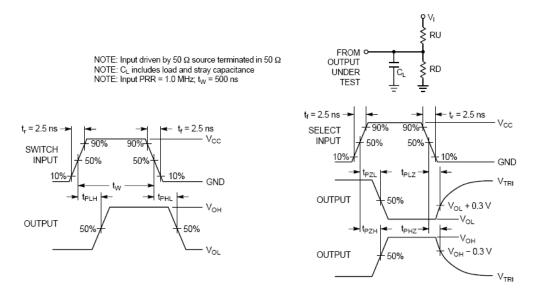


Figure 1. AC Test Circuit ,AC Waveforms



Figure 2. Break Before Make Interval Timing



TEST CIRCUITS (continued)

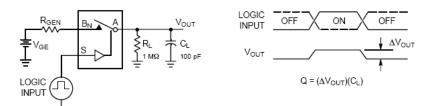


Figure 3. Charge Injection Test

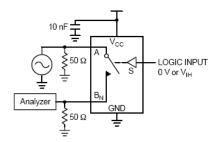


Figure 4. Off Isolation

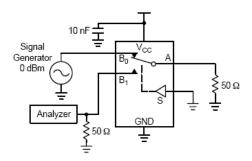


Figure 5.Crosstalk

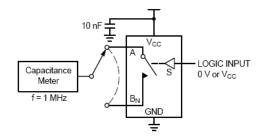


Figure 6. Channel Off Capacitance



TEST CIRCUITS (continued)

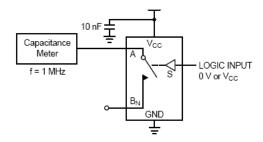


Figure 7. Channel On Capacitance

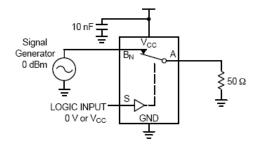
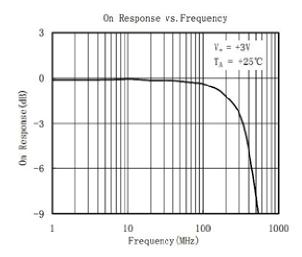
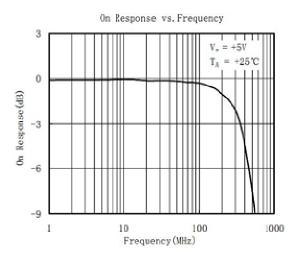


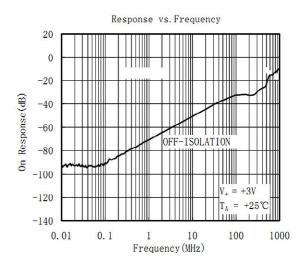
Figure 8. Bandwidth

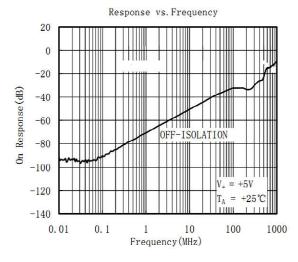


TYPICAL PERFORMANCE CHARACTERISTICS





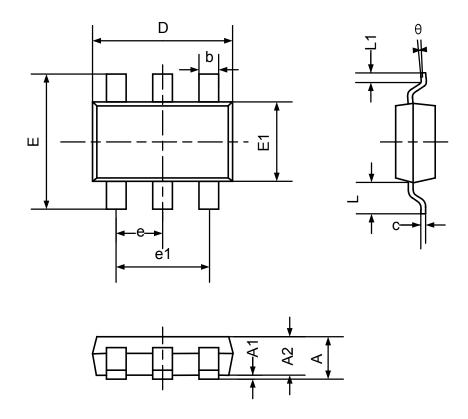






PACKAGE OUTLINE

SC70-6



Cumbal	Dimensions in Millimeters					
Symbol	Min	Max				
Α	0.85	1.05				
A1	0.00	0.10				
A2	0.80	1.00				
b	0.15	0.35				
С	0.08	0.22				
D	2.02	2.12				
E	2.20	2.40				
E1	1.25	1.35				
е	0.65BSC					
e1	1.30BSC					
L	0.50REF					
L1	0.28 0.38					
θ	0° 8°					



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