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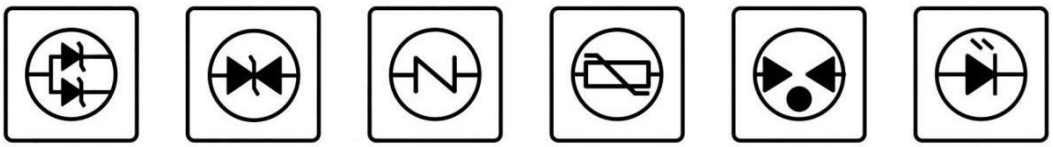


LMV721IDBVR-MS/LMV722IDR-MS

Product specification

GENERAL DESCRIPTION

The LMV721IDBVR-MS/LMV722IDR-MS families of products offer low voltage operation and rail-to-rail input and output, as well as excellent speed/power consumption ratio, providing an excellent bandwidth(11MHz), a slew rate of 10V/us, and a quiescent current of 150uA/amplifier at 2.2V. The op-amps are unity gain stable and feature an ultra-low input bias current.

The LMV721IDBVR-MS/LMV722IDR-MS are designed to provide optimal performance in low-voltage systems. They provide rail-to-rail I/O, and the maximum input offset voltage are 2mV for the devices. Their capacitive load capability is also good at low supply voltages. The operating range is from 2.2 V to 5.5 V.

The LMV72x families of operational amplifiers are specified at the full temperature range of - 40°C to +105 °C under single or dual power supplies of 2.2V to 5.5V.

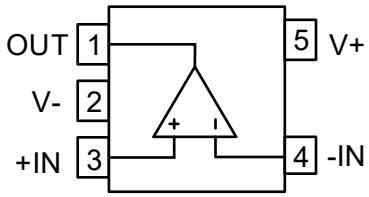
Features

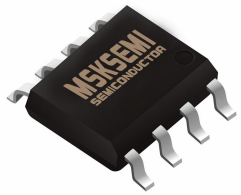
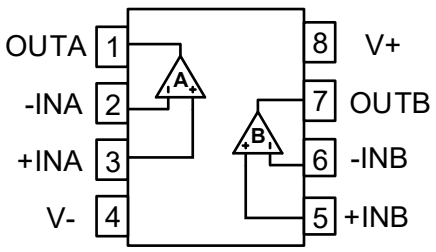
- Input Offset Voltage：2mV（MAX）
- Low Supply Current：150μA（Vs=2.2V）
- Supply Range：2.2V to 5.5V
- Gain Bandwidth：11MHz（Vs=5V）
- Slew rate: 10V/μs（Vs=5V）
- Rail-to-Rail Input and Output
- Low Cost
- Micro size Packages：
  LMV721IDBVR-MS：SOT23-5
  LMV722IDR-MS：SOP-8

Applications

- Photodiode Amplification
- Active Filter and Buffer
- Battery Powered Electronics
- Sensors
- Cellular and Cordless Phones
- Test Equipment
- Driving A/D Converters

Pin Description AND MARKING

SOT-23-5	Pin Description	Marking
		

SOP-8	Pin Description	Marking
		

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LMV721IDBVR-MS

PIN		I/O	DESCRIPTION
NAME	SOT-23-5		
+IN	3	I	Positive (noninverting) input
-IN	4	I	Negative (inverting) input
OUT	1	O	Output
V+	5	—	Positive (highest) power supply
V-	2	—	Negative (lowest) power supply

LMV722IDR-MS

PIN		I/O	DESCRIPTION
NAME	SOP-8		
+INA	3	I	Noninverting input, channel A
+INB	5	I	Noninverting input, channel B
-INA	2	I	Inverting input, channel A
-INB	6	I	Inverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
V-	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

Package/Order Information

ORDERING NUMBER	Op Temp(℃)	Package	Packing Option
LMV721IDBVR-MS	-40°C~105°C	SOT23-5	3000PCS
LMV722IDR-MS		SOP-8	2500PCS

TYPICAL APPLICATION

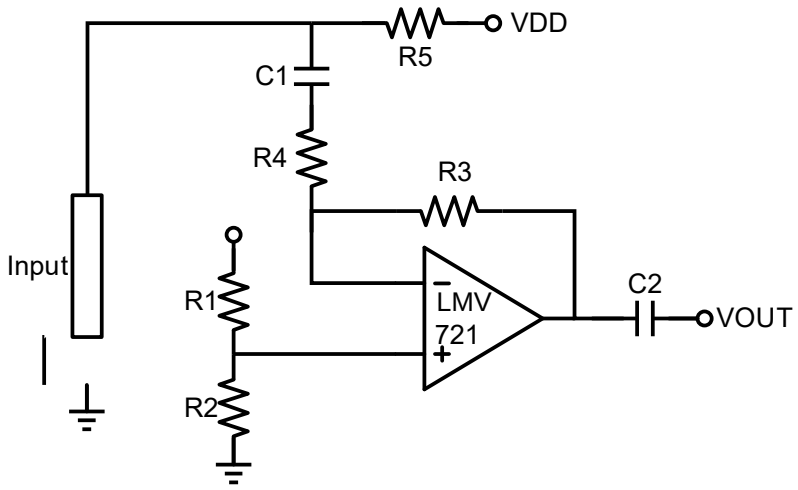

Figure 1. Typical Application

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SPECIFICATIONS

Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Voltage	Supply Voltage		6	V
	Signal Input Terminals Voltage(2)	(V-) - 0.5	(V+) + 0.5	V
	Signal Input Terminals Voltage(3)	(V-) - 0.5	(V+) + 0.5	V
Current	Signal Input Terminals Current(2)	-10	10	mA
	Signal output Terminals Current(3)	-200	200	mA
	Output Short-Circuit(4)	Continuous		
θ_{JA}	Operating Temperature Range	-40	105	°C
	Storage Temperature Range	-65	150	°C
	Junction Temperature	-40	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5V beyond the supply rails should be current-limited to ±200mA or less.

(4) Short-circuit to ground, one amplifier per package.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM)	±2000	V
		Charged-Device Model (CDM)	±500	V
		Machine Model	100	V

Recommended Operating Conditions

		MIN	MAX	UNIT
Supply voltage， Vs= (V+) - (V-)	Single-supply	2.2	5.5	V
	Dual-supply	±1.1	±2.75	V

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ELECTRICAL CHARACTERISTICS(V_S = +5V)

At T_A = 25°C, V_{IN}=V_{OUT}= V_S /2, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input Offset Voltage			0.2	2	mV
dV_{OS}/dT	Input Offset Voltage Average Drift	T_A = -40°C to 105°C		0.4	0.6	μV/°C
INPUT CURRENT						
I_B	Input Bias Current			400	1000	pA
		T_A = -40°C to 105°C		4		pA/°C
I_{OS}	Input Offset Current			30		pA
NOISE						
V_N	Input Voltage Noise	f=0.1Hz to 10Hz		15		μV_{PP}
	Input Voltage Noise PSD	f=1kHz		61		nV/√Hz
INPUT VOLTAGE						
V_{CM}	Common-Mode Voltage Range		(V_{S-})-0.1		(V_{S+})+0.1	V
CMRR	Common-Mode Rejection Ratio	ΔV_{IN}=2V		90	100	dB
FREQUENCY RESPONSE						
GBW	Gain-Bandwidth Product			11		MHz
SR	Slew Rate	G = +1, V_{IN}=2V Step		10		V/μs
Ts	Settling Time	G = +1, V_{IN}=2V Step		0.6		us
OUTPUT						
A_V	Open-Loop Voltage Gain	ΔV_{OUT}=4V	110	115		dB
$V_{OUT-SWING}$	Output Swing from Rail				5	mV
I_{SC}	Output Short-Circuit Current	Sourcing, V_{OUT}=0V $V_{IN(diff)}$=±0.5V		20		mA
		Sinking, V_{OUT}=2.5V $V_{IN(diff)}$=±0.5V		-70		mA

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C_L(1)	Capacitive Load Drive	G=+1,V_{IN}=2V Step			200	pF
POWER SUPPLY						
PSRR	Power-Supply Rejection Ratio	V_S=2.2V to 5.5V	90	110		dB
V_S	Operating Voltage Range	I_O=0A	2.2		5.5	V
I_Q	Quiescent Current/Amplifier	I_O=0A		250	288	μA

(1) Capacitive load drive means that above a given maximum value, the output waveform will oscillate under the step response.

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ELECTRICAL CHARACTERISTICS(V_S = +2.2V)

At T_A = 25°C, V_{IN}=V_{OUT}= V_S /2, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input Offset Voltage			0.18	2	mV
dV_{OS}/dT	Input Offset Voltage Average Drift	T_A = -40°C to 105°C		0.4	0.6	μV/°C
INPUT CURRENT						
I_B	Input Bias Current			200	700	pA
		T_A = -40°C to 105°C		4		pA/°C
I_{OS}	Input Offset Current			200		pA
NOISE						
V_N	Input Voltage Noise	f=0.1Hz to 10Hz		15		μV_{PP}
	Input Voltage Noise PSD	f=1kHz		61		nV/√Hz
INPUT VOLTAGE						
V_{CM}	Common-Mode Voltage Range		(VS-)-0.1		(VS+)+0.1	V
CMRR	Common-Mode Rejection Ratio	ΔV_{IN}=1V	80	90		dB
FREQUENCY RESPONSE						
GBW	Gain-Bandwidth Product			6.5		MHz
SR	Slew Rate			5		V/μs
Ts	Settling Time			0.8		us
OUTPUT						
A_V	Open-Loop Voltage Gain	ΔV_{OUT}=2V	105	110		dB
$V_{OUT-SWING}$	Output Swing from Rail				5	mV
I_{SC}	Output Short-Circuit Current	Sourcing, V_{OUT}=0V $V_{IN(diff)}$=±0.5V		11		mA
		Sinking, V_{OUT}=2.2V $V_{IN(diff)}$=±0.5V		-16.6		mA

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C_L(1)	Capacitive Load Drive	G = +1, V_{IN}=1V Step			100	pF
POWER SUPPLY						
PSRR	Power-Supply Rejection Ratio	V_S=2.2V to 5.5V	90	110		dB
V_S	Operating Voltage Range	I_O=0A	2.2		5.5	V
I_Q	Quiescent Current/Amplifier	I_O=0A		150	167	μA

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TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = +5V, G=+1, V_{IN}=V_{OUT}= V_S /2, unless otherwise noted.

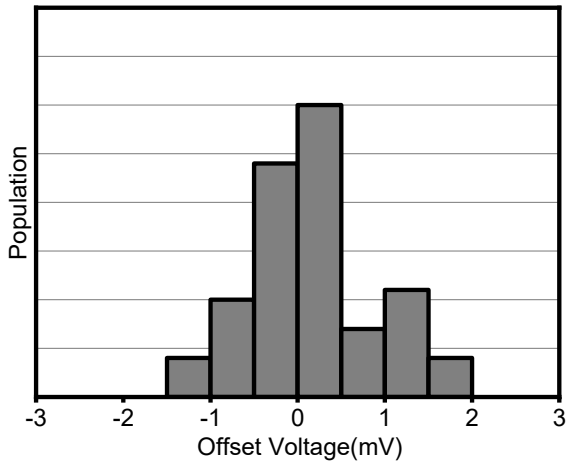

Figure 2. Offset Voltage Production Distribution

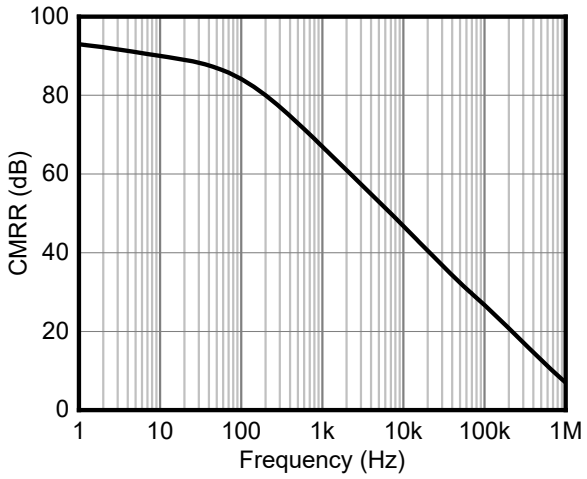

Figure 3. CMRR vs Frequency

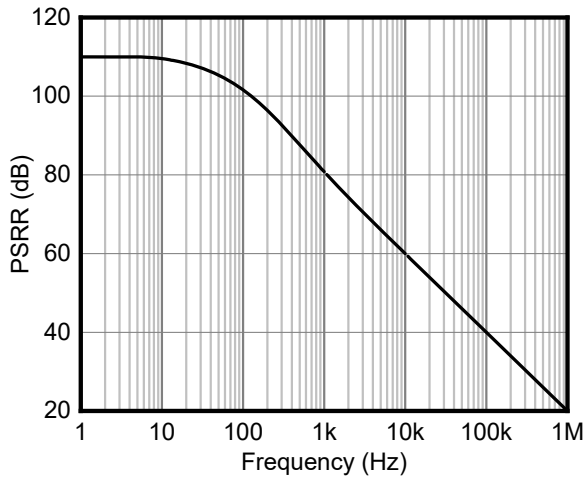

Figure 4. PSRR vs Frequency

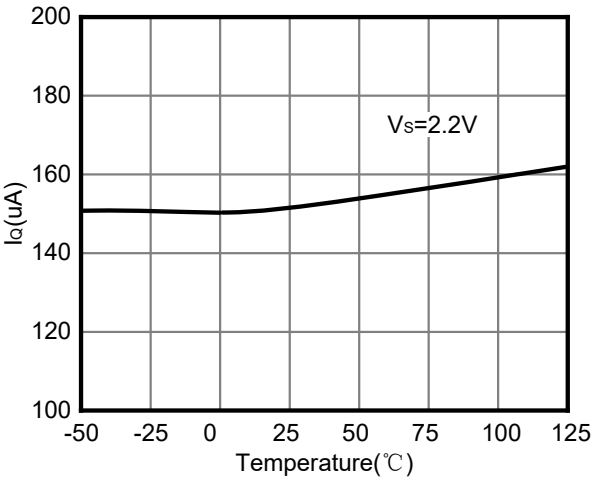

Figure 5. Quiescent Current vs Temperature

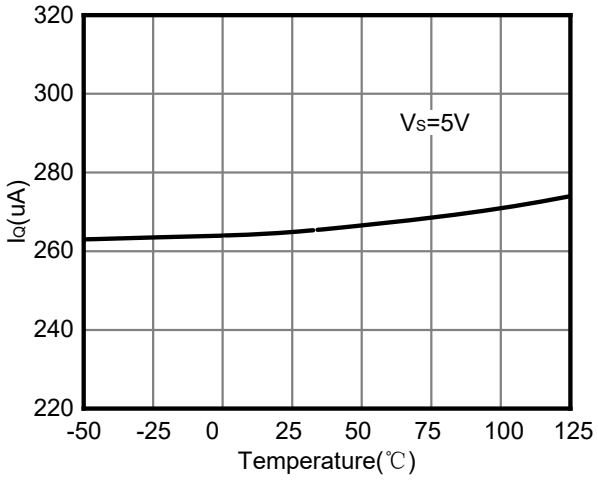

Figure 6. Quiescent Current vs Temperature

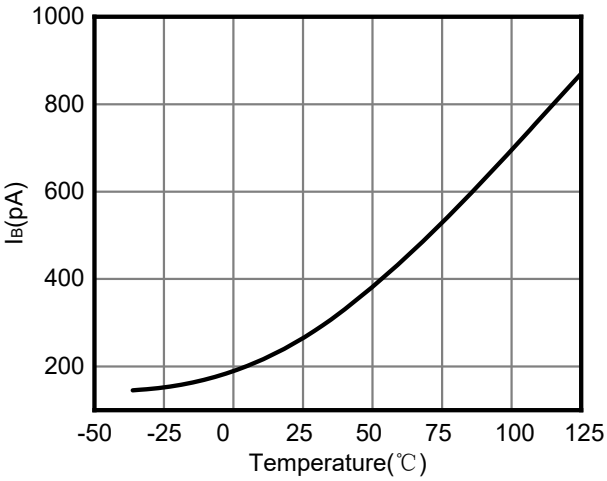

Figure 7. Input Bias Current vs Temperature

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TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = +5V, G=+1, V_{IN}=V_{OUT}= V_S /2, unless otherwise noted.

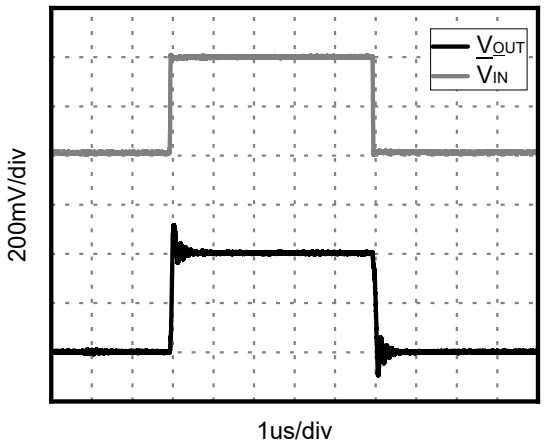

Figure 8. Small-Signal Step Response

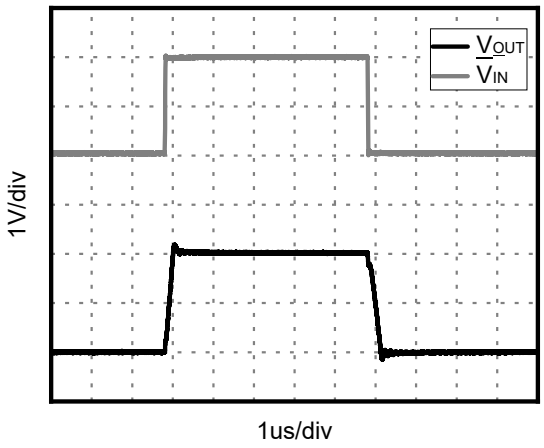

Figure 9. Large-Signal Step Response

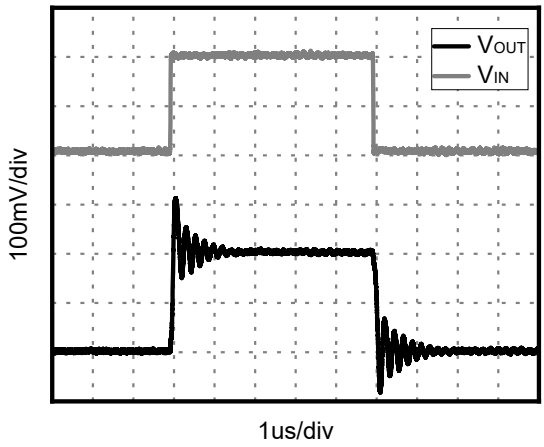

Figure 10. Small-Signal Step Response(V_S=2.2V)

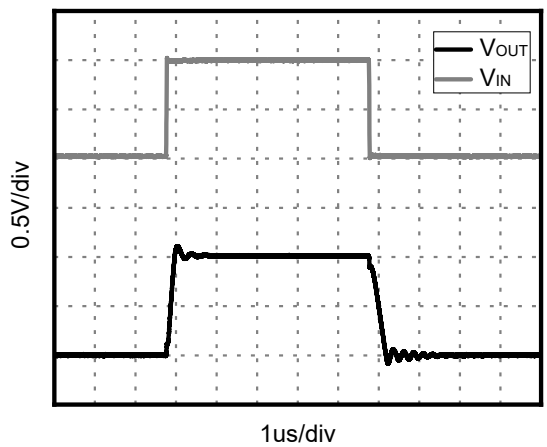

Figure 11. Large-Signal Step Response(V_S=2.2V)

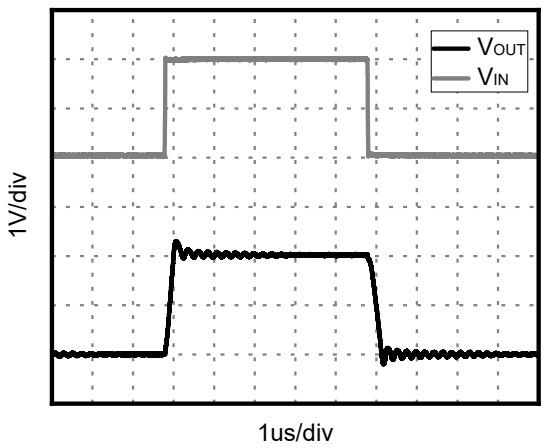

Figure 12. Capacitive Load Drive(C_L=200pF)

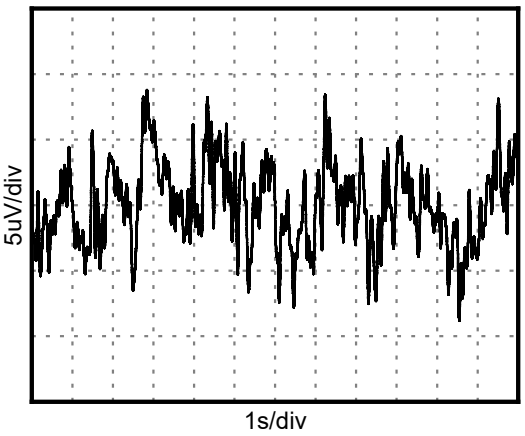

Figure 13. 0.1Hz to 10Hz Noise

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TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = +5V, G=+1, V_{IN}=V_{OUT}= V_S /2, unless otherwise noted.

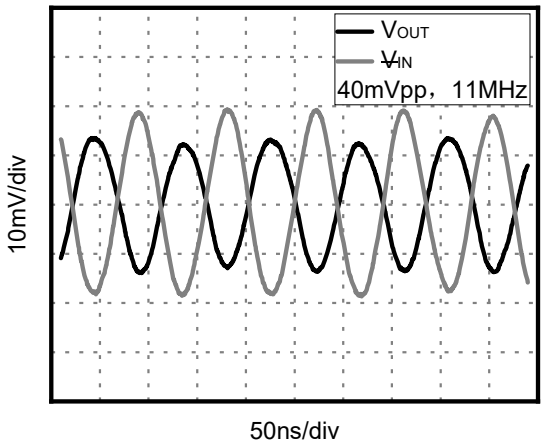

Figure 14. -3dB bandwidth

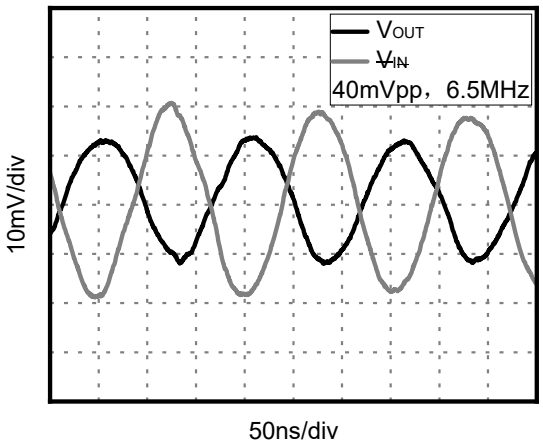

Figure 15. -3dB bandwidth (V_S=2.2V)

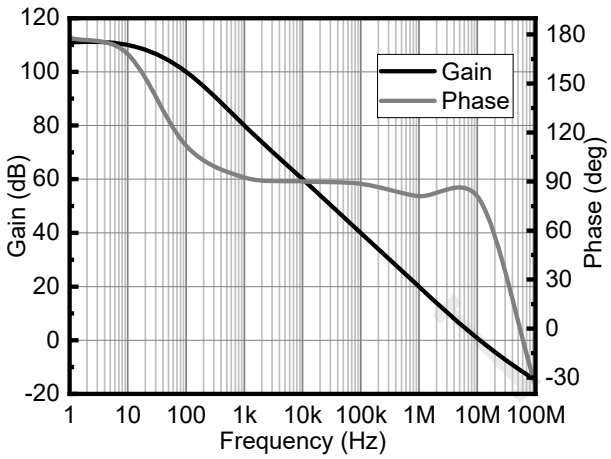

Figure 16. Open-Loop Gain and Phase vs Frequency

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Detailed Description

Overview

The LMV721IDBVR-MS/LMV722IDR-MS devices are a high-bandwidth, unity-gain stable, rail-to-rail operational amplifier available in single and dual-channel versions that operate in a single-supply voltage range of 2.2V to 5.5V(±1.1V to ±2.75V). A high supply voltage of 6V(absolute maximum) can permanently damage the amplifier. Rail-to-rail input and output wobbles significantly increase the dynamic range, especially in low-supply applications. Good layout practices require that a 0.1uF capacitor be used where it is tightly threaded through the power supply pin.

Phase Reversal Protection

The LMV721IDBVR-MS/LMV722IDR-MS devices have internal phase-reversal protection.
Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range,
causing the output to reverse into the opposite rail. The input of the LMV721IDBVR-MS/LMV722IDR-MS prevents phase reversal with excessive commonmode voltage. Instead, the appropriate rail limits the output voltage.

Typical Applications

1 Voltage Follower

As shown in Figure 17, the voltage gain is 1. With this circuit, the output voltage V_{OUT} is configured to be equal to the input voltage V_{IN}. Due to the high input impedance and low output impedance, the circuit can also stabilize the output voltage, the output voltage expression is

$$V_{OUT}=V_{IN} \quad (1)$$

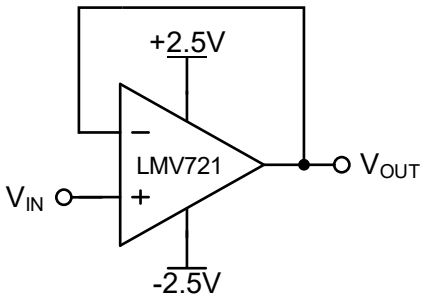

Figure 17. Voltage Follower

2 Inverting Proportional Amplifier

As shown in Figure 18, for a reverse-phase proportional amplifier, the input voltage V_{IN} is amplified by a voltage gain that depends on the ratio of R1 to R2. The output voltage V_{OUT} is inversely with the input voltage V_{IN}. The input impedance of the circuit is equal to R1, and the output voltage expression is

$$V_{OUT}=-\frac{R2}{R1}V_{IN} \quad (2)$$

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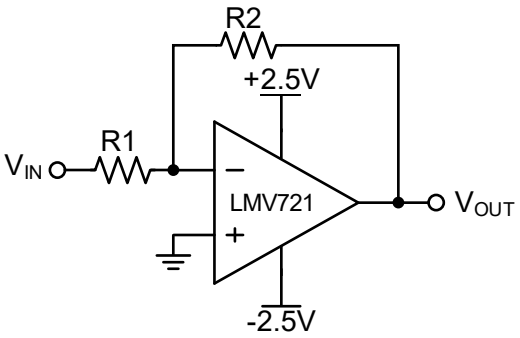

Figure 18. Inverting Proportional Amplifier

3 Noninverting Proportional Amplifier

As shown in Figure 19, for a noninverting amplifier, the input voltage V_{IN} is amplified by a voltage gain that depends on the ratio of R1 to R2. The output voltage V_{OUT} is in phase with the input voltage V_{IN}. In fact, this circuit has a high input impedance because its input side is the same as the input side of the operational amplifier. The output voltage expression is

$$V_{OUT}=(1+\frac{R2}{R1})V_{IN} \quad (3)$$

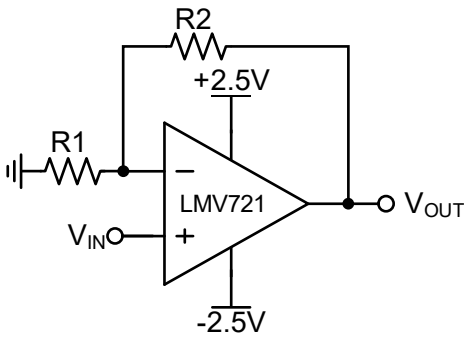

Figure 19. Noninverting Proportional Amplifier

Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1uF capacitor closely across the supply pins.

These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI susceptibility.

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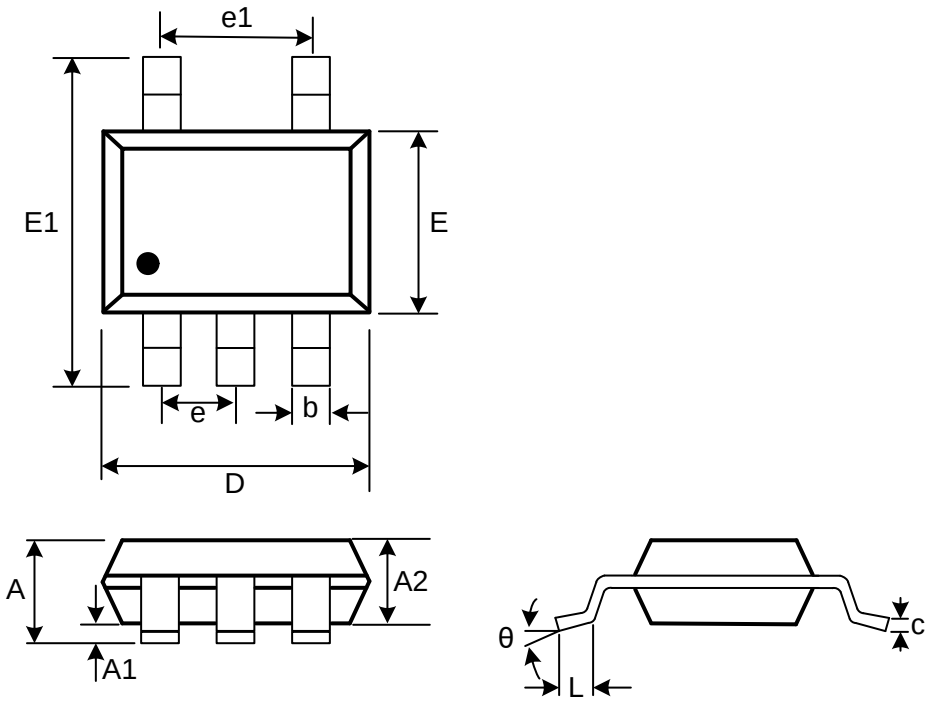
Package Description

SOT23-5



(Unit: mm)

Symbol	Min	Max
A	1.05	1.25
A1	0	0.1
A2	1.05	1.15
b	0.3	0.5
c	0.1	0.2
D	2.82	3.02
e	0.95(BSC)	
e1	1.9(BSC)	
E	1.5	1.7
E1	2.65	2.95
L	0.3	0.6
θ	0°	8°

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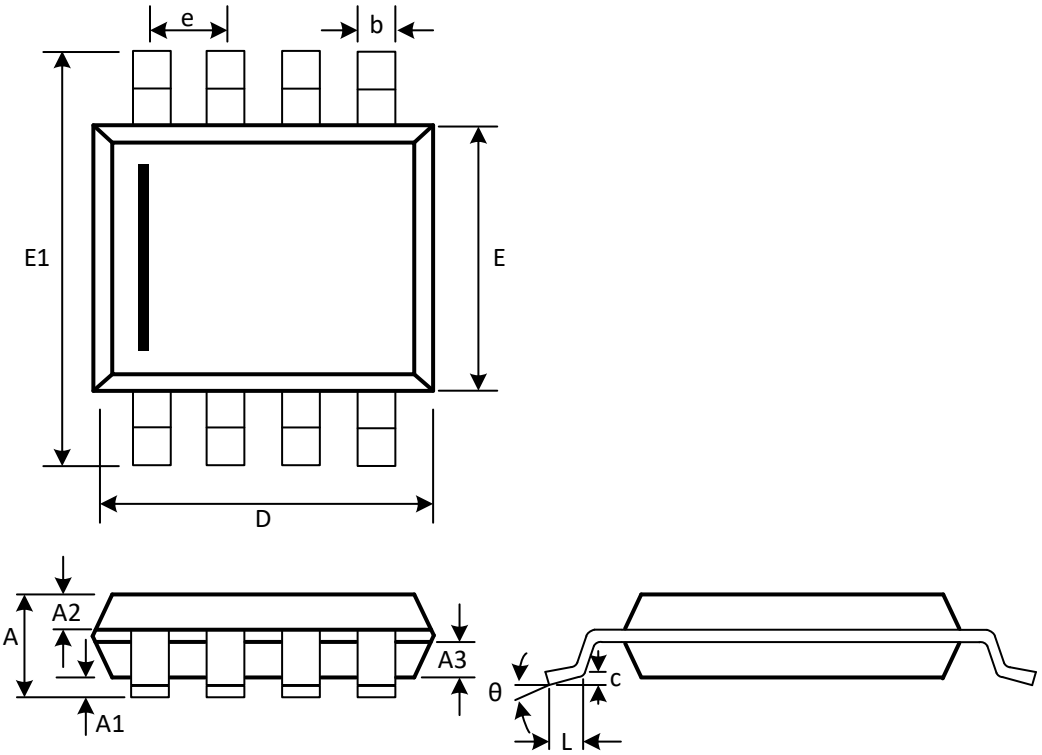
SOP-8



(Unit: mm)

Symbol	Min	Max
A	1.300	1.600
A1	0.050	0.200
A2	0.550	0.650
A3	0.550	0.650
b	0.356	0.456
c	0.203	0.233
D	4.800	5.000
e	1.270(BSC)	
E	3.800	4.000
E1	5.800	6.200
L	0.400	0.800
θ	0°	8°

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