1. DESCRIPTION

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The ’LS160 and ’LS161 are decade counters and the ’LS163 is 4-bit binary counters.Synchronous operation is provided by having all flip-flops clocks simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating.This mode of operating eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters, however counting spikes may occur on the (RCO) ripple carry output.A buffered clock input triggers the four flip-flops on the rising edge of the clock input waveform.

These counters are fully programmable; that is,the outputs may be preset to either level.As presetting is synchronous,setting up a low level at the load input disables the counter and causes and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.Low-to-high transition.This restriction is not application to the ’LS160 or’LS163.The clear function for the’LS160,and ’LS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock,load,or enable inputs.The clear function for the ’LS163 is synchronous and a low level at the clear input sets all full of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs.This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate.The gate output is connected to the clear input too synchronously clear the counter to 0000(LLLL).

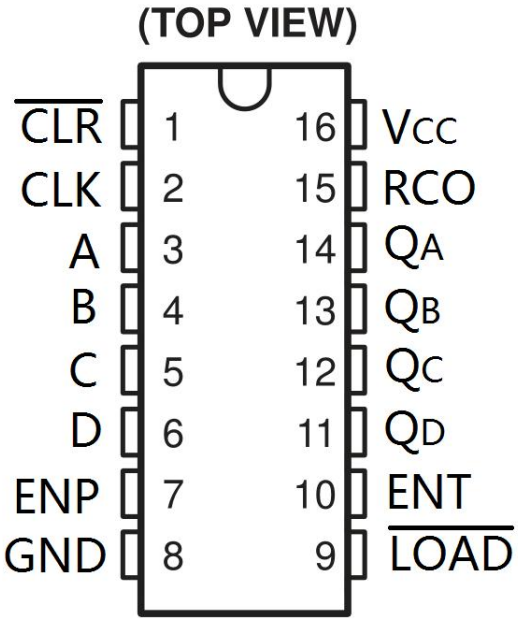
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating.Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output.The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output.This high level overflow ripple carry pulse can be used to enable successive cascaded stages.Transitions at the enable P or T inputs of the ’LS160 thru ’LS163 are allowed regardless of the level of the clock input.

’LS160 thru ’LS163 feature a fully independent clock circuit.Changes at control inputs(enable P or T,or load) that will modify the operating mode have no effect until clocking occurs,The function of the counter(whether enabled,disabled,loading,or counting)will be dictated solely by the conditions meeting the stable setup and hold times.

2. FEATURES

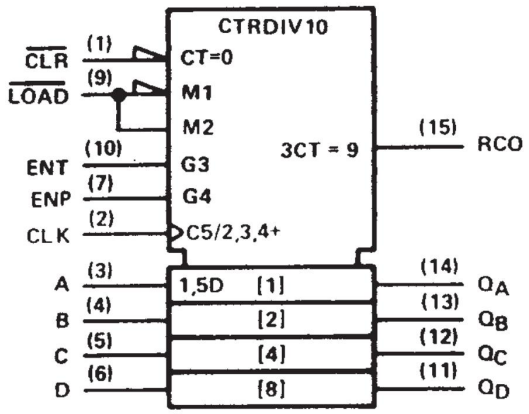
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

3. PIN CONFIGURATIONS

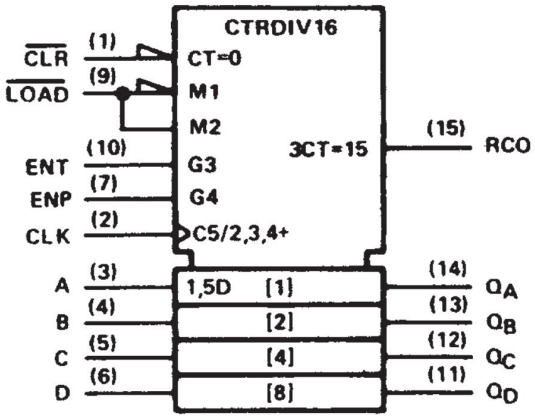


4. LOGIC SYMBOLS

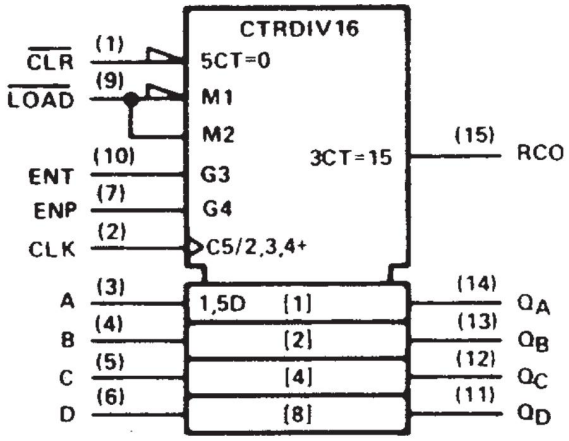
'LS160



'LS161

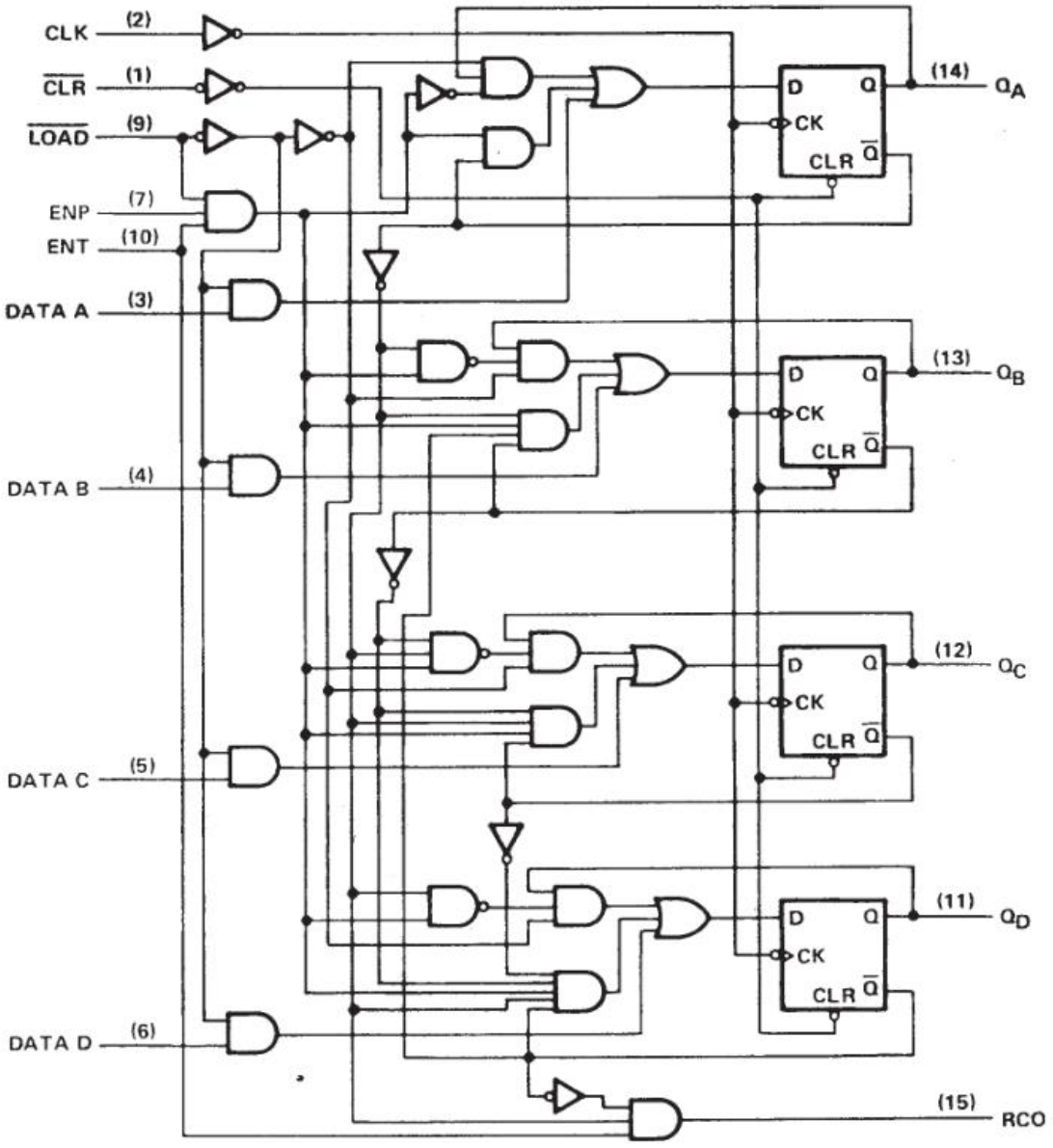


'LS163

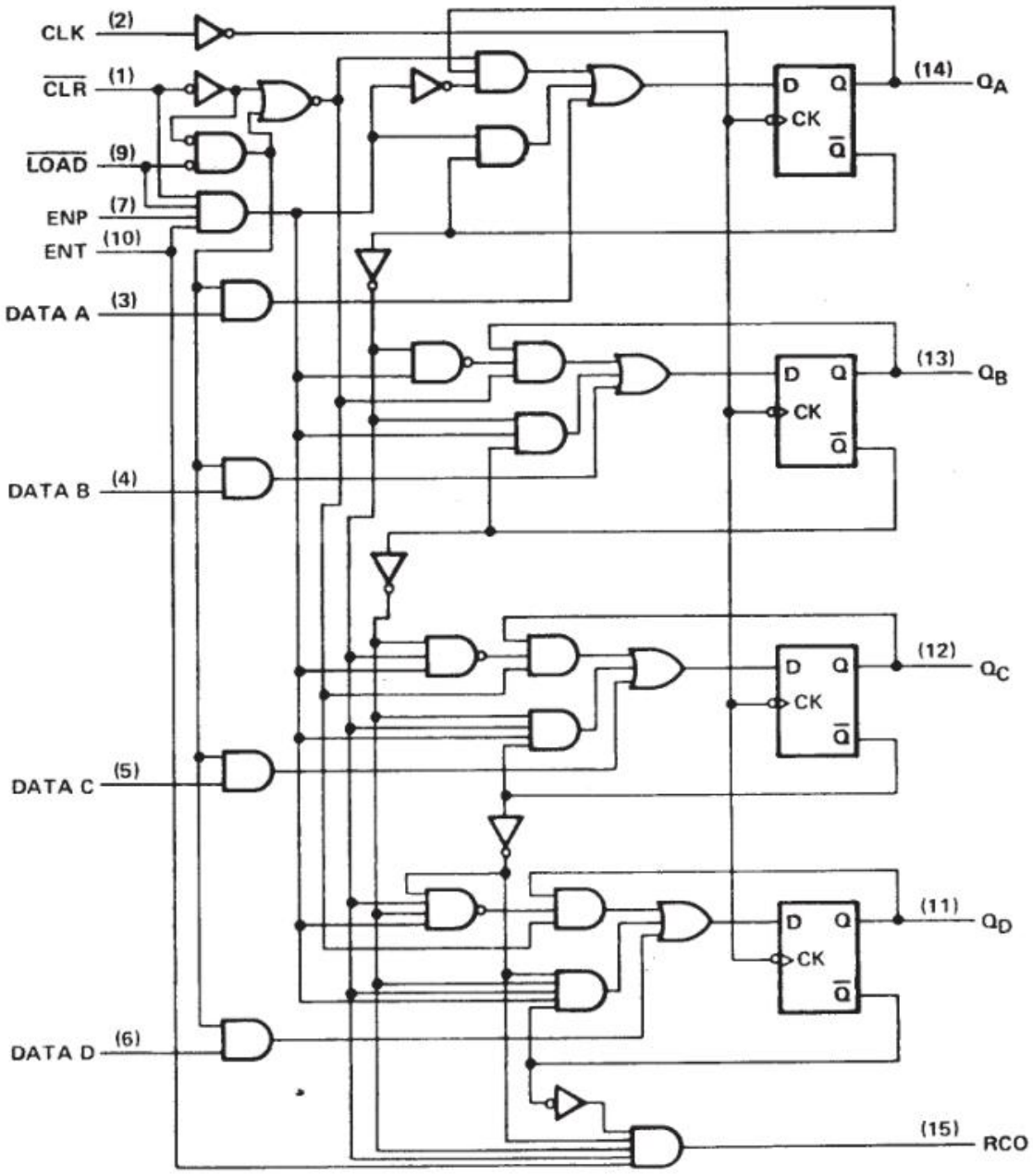


5. LOGIC DIAGRAM

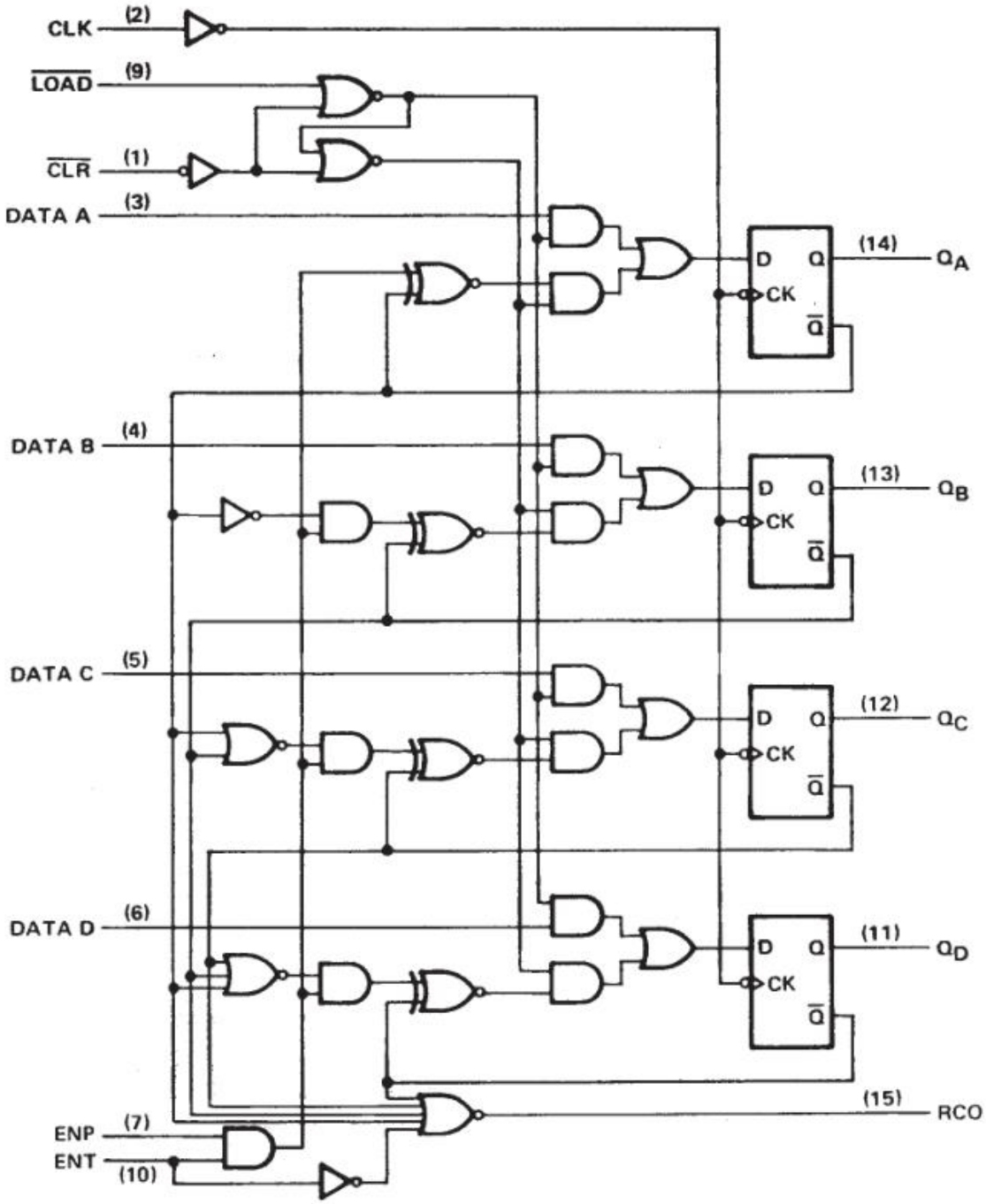
’74LS160



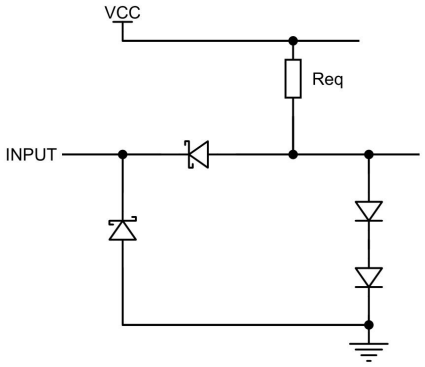
’74LS161


CLK (2)
CLR (1)
LOAD (9)
ENP (7)
ENT (10)
DATA A (3)
DATA B (4)
DATA C (5)
DATA D (6)
D Q
CK
Q
(14) QA
(13) QB
(12) QC
(11) QD
(15) RCO

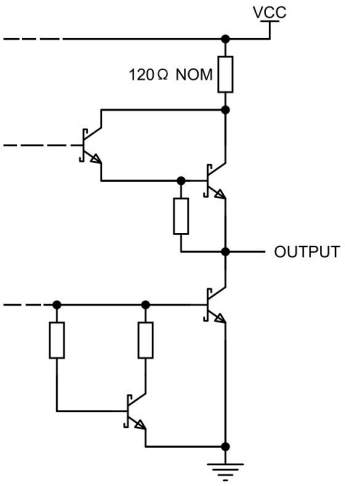
’74LS163


CLK
(2)
LOAD
(9)
CLR
(1)
DATA A
(3)
DATA B
(4)
DATA C
(5)
DATA D
(6)
ENP
(7)
ENT
(10)
D
Q
CK
Q
(14)
QA
(13)
QB
(12)
QC
(11)
QD
(15)
RCO

6. SCHEMATICS OF INPUTS AND OUTPUTS



EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS

7. ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTES)

Supply voltage, V_{CC} 7V

Input voltage, VI: 74LS160,74LS161,74LS163..... 7V

Operating free-air temperature range: DIP package..... 0°C to 70°C

Storage temperature range, Tstg..... −65°C to 150°C

8. RECOMMENDED OPERATING CONDITIONS

			74LS160/161/163			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current				−400	μA
I_{OL}	Low-level output current				8	mA
f_{clock}	Clock frequency		0		25	MHz
$t_{w\ (clock)}$	Width of clock pulse		25			ns
$t_{w\ (clear)}$	Width of clear pulse		20			ns
t_{su}	Set up time	Data inputs A,B,C,D	20			ns
		ENP or ENT	20			
		$\overline{LOAD}$	20			
		$\overline{LOAD}$ inactive state	20			
		$\overline{CLR}\uparrow$	20			
		$\overline{CLR}$ inactive state	25			
t_h	Hold time at any input		3			ns
T_A	Operating free-air temperature		0		70	°C

9. ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR RANGE (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS†		74LS160/161/163			UNIT
					MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} MAX	I_{OL} = 4 mA		0.25	0.4	V
				I_{OL} = 8 mA		0.35	0.5	
I_I	Input current at maximum input voltage	Data or ENP	V_{CC} = MAX,	V_I = 7 V			0.1	mA
		$\overline{LOAD}$,CLK,or ENT					0.2	
		$\overline{CLR}$					0.1	
		$\overline{CLR}$					0.2	
I_{IH}	High-level input current	Data or ENP	V_{CC} = MAX,	V_I = 2.7 V			20	μA
		$\overline{LOAD}$,CLK,or ENT					40	
		$\overline{CLR}$					20	
		$\overline{CLR}$					40	
I_{IL}	Low-level input current	Data or ENP	V_{CC} = MAX,	V_I = 0.4 V			−0.4	mA
		$\overline{LOAD}$,CLK,or ENT					−0.8	
		$\overline{CLR}$					−0.4	
		$\overline{CLR}$					−0.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	mA
I_{CCH}	Supply current,all outputs high		V_{CC} = MAX			18	31	mA
I_{CCL}	Supply current,all outputs high		V_{CC} = MAX			19	32	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

10. SWITCHING CHARACTERISTICS,VCC = 5 V, TA = 25℃

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX}			C_L = 15 pF, R_L = 2 kΩ	25	32		MHz
t_{PLH}	CLK	RCO			20	35	ns
t_{PHL}					18	35	
t_{PLH}	$\overline{\text{CLK}}$ (LOAD input high)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	$\overline{\text{CLK}}$ (LOAD input low)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	ENT	RCO			9	14	ns
t_{PHL}					9	14	
t_{PHL}	$\overline{\text{CLR}}$	Any Q			20	28	ns

† t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

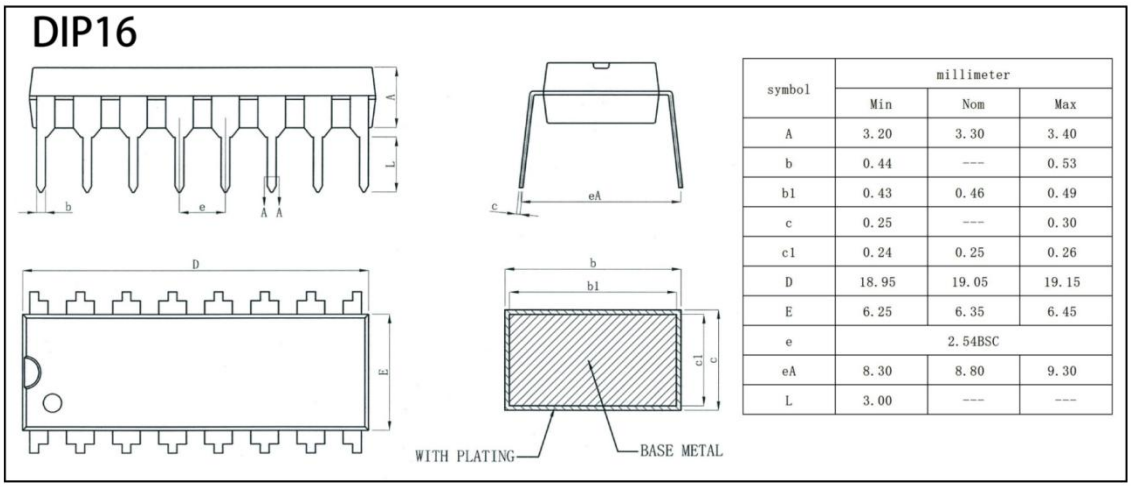
11. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XD74LS160	XD74LS160	DIP16	19.05 * 6.35	-0 to 70	MSL3	Tube 25	1000
XD74LS161	XD74LS161	DIP16	19.05 * 6.35	-0 to 70	MSL3	Tube 25	1000
XD74LS163	XD74LS163	DIP16	19.05 * 6.35	-0 to 70	MSL3	Tube 25	1000

12. DIMENSIONAL DRAWINGS

DIP16



symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---