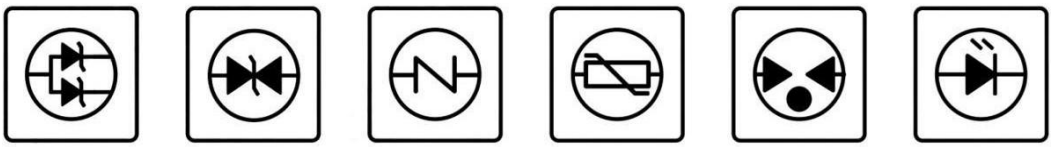
MSKSEMI 美森科
SEMICONDUCTOR



LM339DR-MS

Product specification

GENERAL DESCRIPTION

The LM339DR-MS is a voltage comparator usedinintegratedcircuit.Itprovidesloweroffset voltage, higher power supply voltage capability, lower power supply current, lower propagation delay, wider temperature range and higher ESD performance.

The chip supports single power and duel power supply. For duel power supply, the supply voltage ranges from ±1.5V to ±18V, and the VS is at least 1.5V higher than the input common-mode voltage. The output is compatible with TTL and CMOS, and the drain current is not affected by the power supply voltage. The output can be connected to other drain open circuit output to achieve the wired-and" relationship.

The LM339DR-MS are available in Green SOP-14. It operates over an ambient temperature range of -40°C to +125°C.

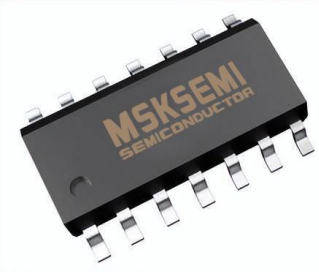
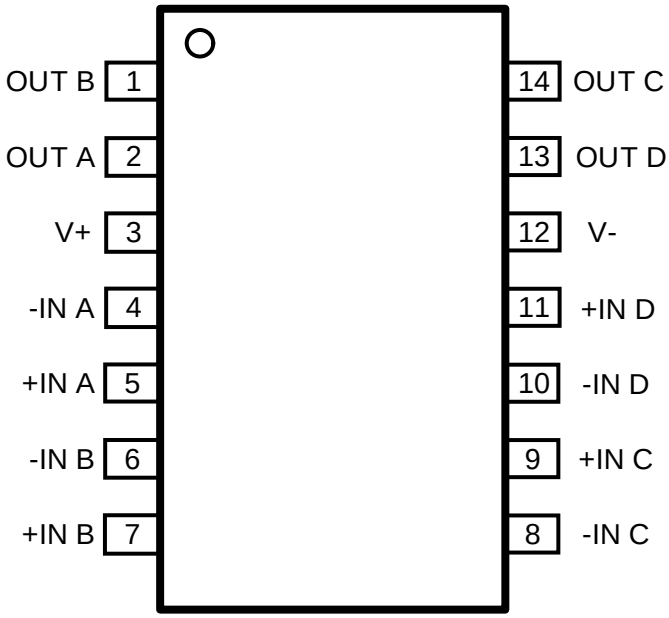
Features

- Wide Supply Range: 3V to 36V
- Low Inuput Offset: 2mV (Typ)
- LowQuiescent Current：
  75μA at Vs=5V
- Low Input Bias Current：1nA
- Input Common-Mode Voltage Range
- Includes Ground
- Open-Drain Output
- Short Response Time
- SIZE PACKAGES: SOP-14

Applications

- Hysteresis Comparators
- Floor mopping robot
- One-way UPS
- Server PSU
- Cordless power tool
- Industrial Automation and Control
- Motor driver
- Instruments and apparatus

Pin Description AND MARKING

SOP-14	Pin Description	Marking
		

Pin Description

Pin Name	Pin Number SOP-14	I/O	Description
OUTB	1	O	Output, channel B
OUTA	2	O	Output, channel A
V+	3	_	Positive (highest) power supply
-INA	4	I	Inverting input, channel A
+INA	5	I	Noninverting input, channel A
-INB	6	I	Inverting input, channel B
+INB	7	I	Noninverting input, channel B
-INC	8	I	Inverting input, channel C
+INC	9	I	Noninverting input, channel C
-IND	10	I	Inverting input, channel D
+IND	11	I	Noninverting input, channel D
V-	12	_	Negative(lowest) power supply
OUTD	13	O	Output, channel D
OUTC	14	O	Output, channel C

Package/Order Information

ORDERING NUMBER	Op Temp(℃)	Package	Packing Option
LM339DR-MS	-40°C~125°C	SOP-14	2500PCS

Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Voltage	Supply, V_s=(V+) - (V-)		40	V
	Input pin (IN+, IN-) (2)	(V-) - 0.3	(V+) + 0.3	V
	Signal output pin (3)	(V-) - 0.3	(V+) + 0.3	V
Current	Signal Input pin (IN+, IN-) (2)	-10	10	mA
	Signal output pin (3)	-55	55	mA
Temperature	Operating Range	-40	125	°C
	Storage	-65	150	°C
	Junction		150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5V beyond the supply rails should be current-limited to ±55mA or less.

(3) Short-circuit from output to V_{CC} can cause excessive heating and eventual destruction.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

		MIN	MAX	UNIT
Supply voltage， Vs= (V+) - (V-)	Single-supply	3	36	V
	Dual-supply	±1.5	±18	V

SIMPLIFIED SCHEMATIC

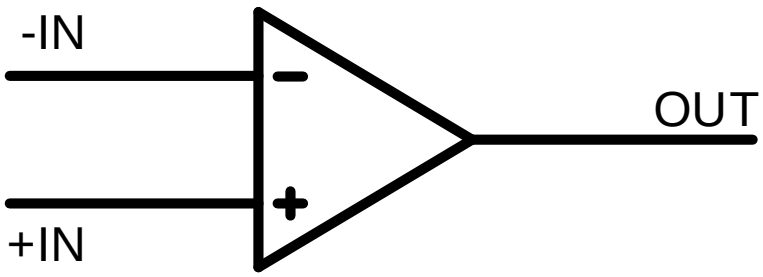


Figure 1. Simplified Schematic

ELECTRICAL CHARACTERISTICS

At T_A = 25°C, V_S=+5V V_{IN+}=V_S, V_{IN-}=1.4V, R_{PU}=10kΩ, unless otherwise noted.

Symbol	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
Vs	Operating Voltage Range		3		36	V
I_Q	Quiescent Current /per channel	Vs=5V		75		μA
		Vs=36V		110		μA
INPUT CHARACTERISTICS						
Vos	Input offset voltage		-5	2	5	mV
I_B	Input Bias Current	V_{CM}=V_S/2		1		nA
I_{OS}	Input Offset Current			1		nA
V_{CM}	Common-Mode Voltage Range		V_{s-}		V_{s+}-1.5	V
A_{VD}	Large-signal Differential-voltage Amplification	V_S = 15 V, V_O = 1.4 V to 11.4 V, R_L ≥ 15 kΩ to V_S	50	200		V/mV
OUTPUT CHARACTERISTICS						
I_{OH}	High-level Output Current	V_{OH}=36V, V_{ID}=1V		2	30	nA
I_{OL}	Low-level Output Current	V_{OL}=1.5V, V_{ID}=-1V		30		mA
V_{OL}	Low-level Output Voltage	I_{OL}=4mA, V_{ID}=-1V		270		mV
DYNAMIC CHARACTERISTICS						
t_{RT}	Propagation Delay H To L	V_S=5V , R_{PU}=5.1kΩ, Overdrive =10mV		485		ns
		V_S=5V , R_{PU}=5.1kΩ, Overdrive =100mV		400		
	Propagation Delay L To H	V_S=5V , R_{PU}=5.1kΩ, Overdrive =10mV		360		
		V_S=5V , R_{PU}=5.1kΩ, Overdrive =100mV		90		

DETAILED DESCRIPTION

Overview

The LM339DR-MS family of comparators can operate up to 36V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its low power and high speed. The open-drain output allows the user to configure the output's logic low voltage (V_{OL}) and can be utilized to enable the comparator to be used in AND functionality.

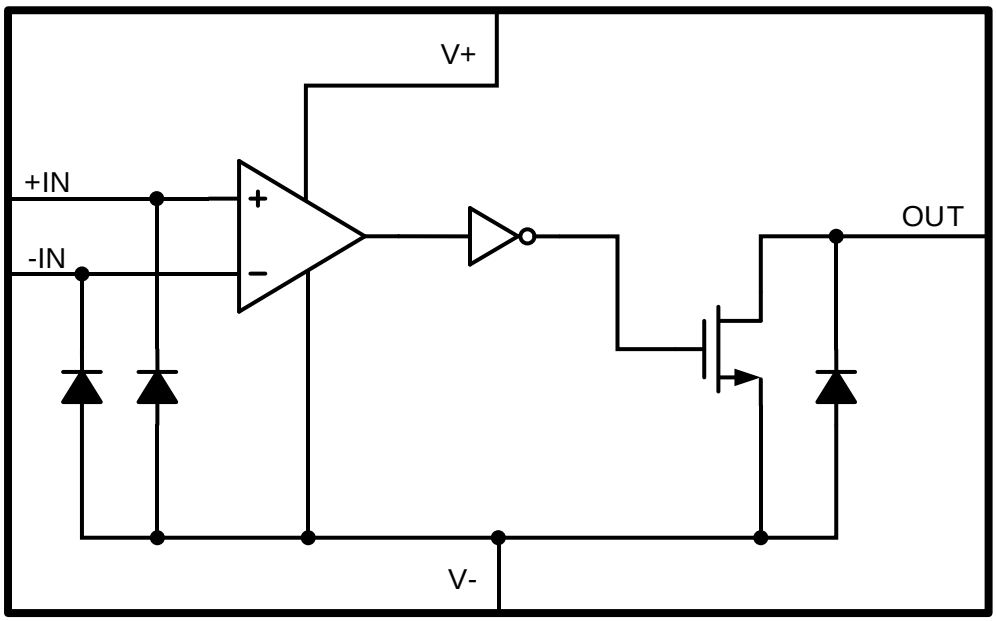


Figure 2. Functional Block Diagram

APPLICATION and IMPLEMENTATION

Application Information

The LM339DR-MS will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output (logic high with pull-up) to drive the comparison logic output to a logic voltage level to an MCU or logic device.

Typical Application

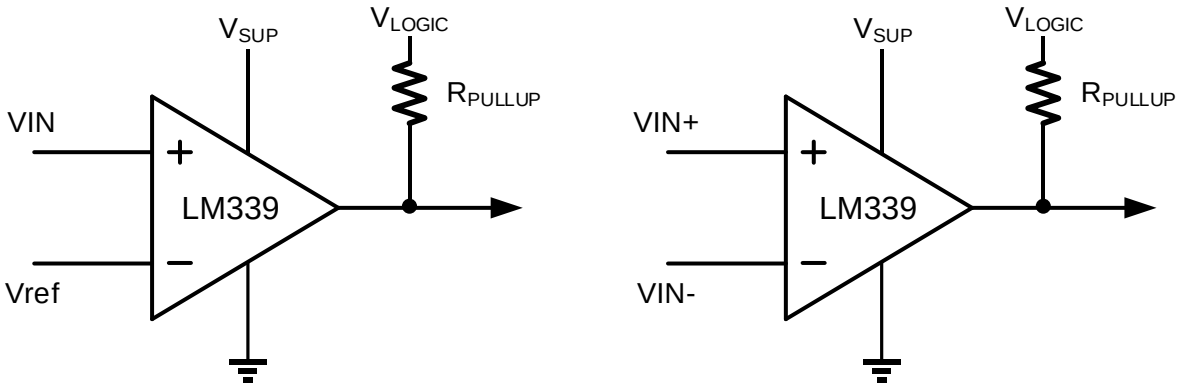


Figure 3. Typical Application Schematic

Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, it is recommended to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation causes temporary fluctuations in the comparator's input common mode range and create an inaccurate comparison.

Layout

Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches, which can affect the high-level input common mode voltage range. In order to achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

Layout Example

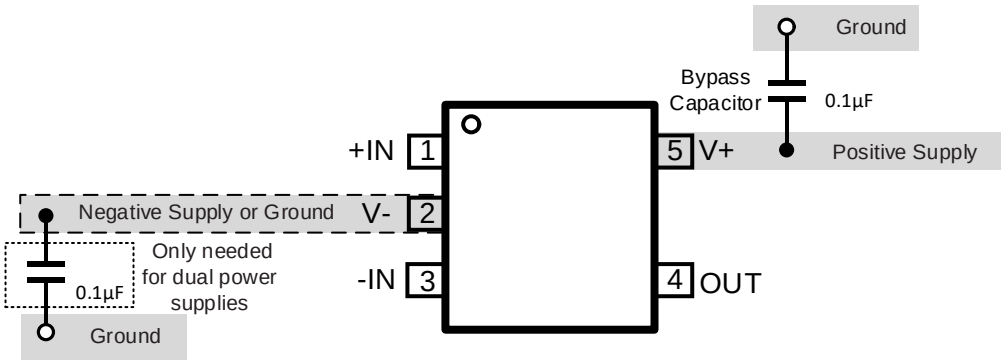
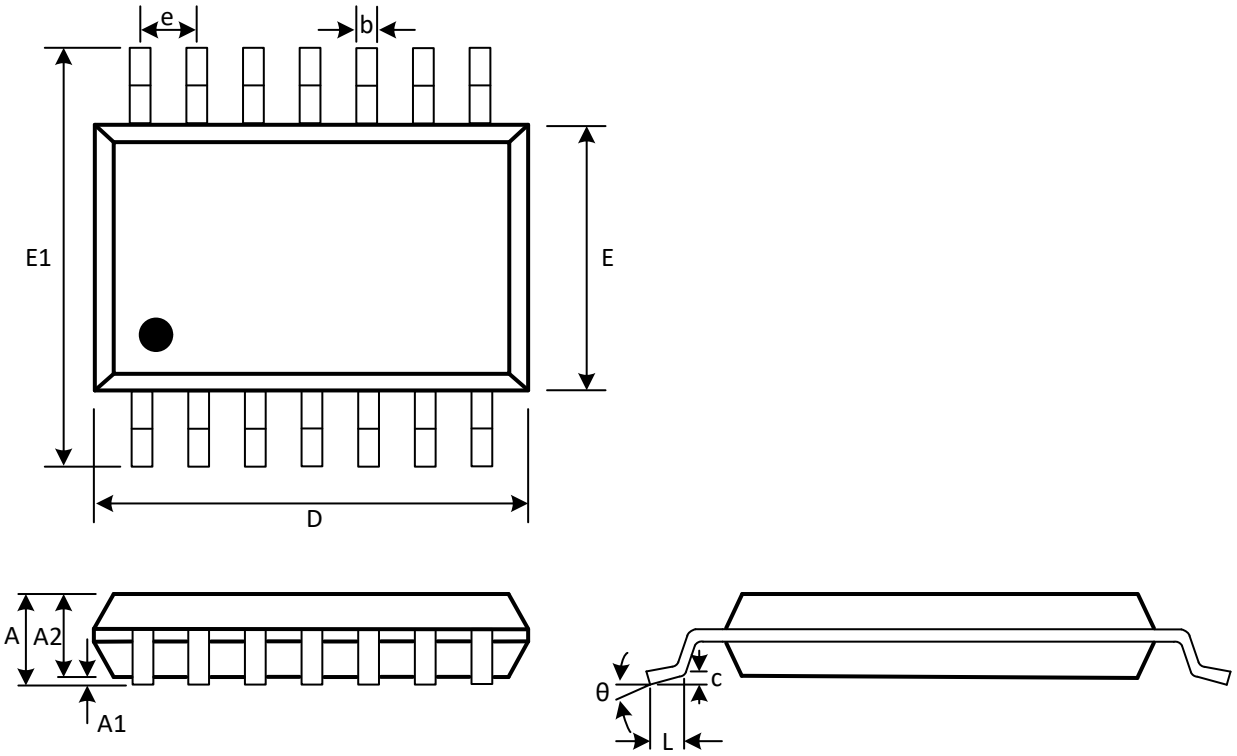


Figure 4. LM339DR-MS Layout Example

PACKAGE DESCRIPTION

SOP-14



(Unit: mm)

Symbol	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.310	0.510
c	0.100	0.250
D	8.450	8.850
e	1.270(BSC)	
E1	5.800	6.200
E	3.800	4.000
L	0.400	1.270
θ	0°	8°

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