Triple 3A, Ultralow Noise, High PSRR, Ultrafast µModule Linear Regulator with Configurable Output Array

FEATURES

- **Linear Regulator µModule® with Triple 3A Output**
- **Input Voltage: 0.6V to 5.5V**
- **Configurable Output Voltage: 0.5V to 4.2V**
- **Ultralow RMS Noise: 1.3µV_{RMS} (10Hz to 100kHz)**
- **High Frequency PSRR: 51dB at 1MHz**
- **Low Dropout Voltage: 45mV Typical at 3A**
- **Ultrafast Transient Response**
- **50% Smaller Than Discrete Solutions**
- ±1.5% Output Voltage Regulation Over Line, Load, and Temperature
- ±2.4% Precision Current Monitor Accuracy at 3A
- Stable with Ceramic Output Capacitors (10µF Minimum)
- Parallel Multiple Devices for Higher Current
- PG Flag, UVLO, Overcurrent and Overtemperature Protection
- 150°C Rated Available
- 6mm × 12mm × 1.92mm BGA Package

APPLICATIONS

- RF Power Supplies: PLLs, VCOs, Mixers, LNAs, PAs
- High Speed/High Precision Data Converter
- FPGA, DSP, and Microprocessor Power Supplies
- High-Speed Servers and Storage Devices
- Medical and Healthcare
- Very-Low-Noise Instrumentation
- Post-Regulation for Switching Supplies

DESCRIPTION

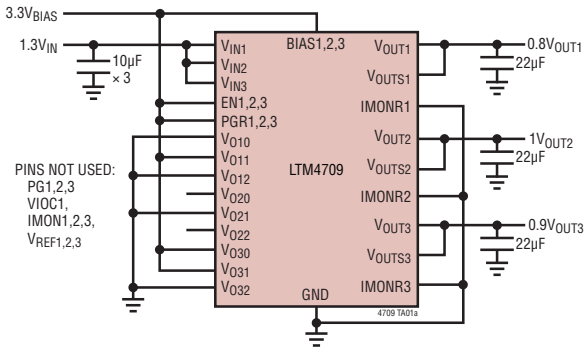
The LTM®4709 is a low voltage, triple 3A µModule linear regulator offering a high power supply rejection ratio (PSRR), ultralow noise, and ultrafast transient response. The µModule regulator includes low dropout linear regulators (LDO), capacitors, and resistors. Operating over an input voltage range of 0.6V to 5.5V, the LTM4709 supports an output voltage range of 0.5V to 4.2V for triple 3A channels with a typical dropout voltage of 45mV. The output voltage is digitally configurable in 50mV increments from 0.5V to 1.2V; 100mV increments from 1.2V to 1.8V; and discrete levels at 2V, 2.5V, 3V, 3.3V, and 4.2V. A precision current monitor provides accurate current monitoring for the energy management system and current limit. The LTM4709 is ideal for RF communication, noise-sensitive instrumentation, post-regulation for switching regulators, high-performance FPGAs, and microprocessors. Only input, output, and bias ceramic capacitors are needed for its application.

Fault protection features include UVLO, power good, overcurrent, and overtemperature protection. The LTM4709 is offered in 6mm × 12mm × 1.92mm, 98-pin BGA package with 0.8mm ball pitch.

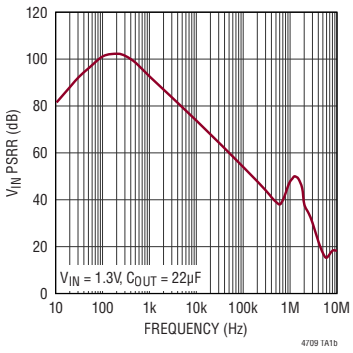
Configurable Output Array

TYPICAL APPLICATION

Triple 3A µModule Regulator



V_{IN} PSRR at 1V_{OUT} and 3A

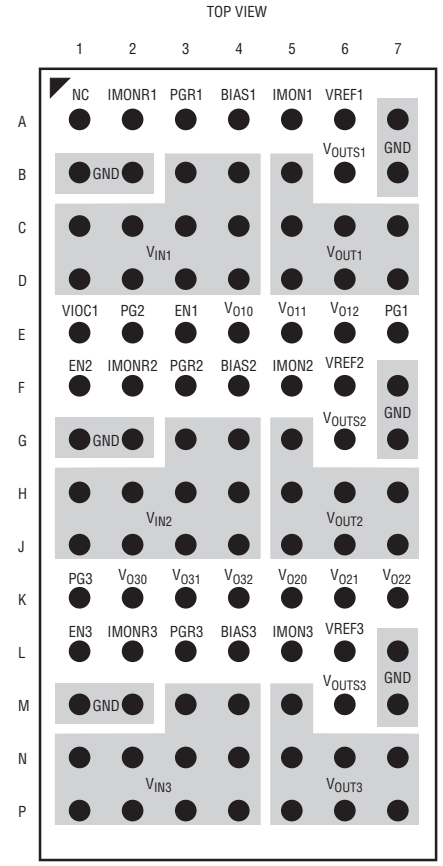


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1}, V_{IN2}, V_{IN3} ..... –0.3V to 6V
V_{OUT1}, V_{OUT2}, V_{OUT3} ..... –0.3V to 6V
V_{OUTS1}, V_{OUTS2}, V_{OUTS3} ..... –0.3V to 6V
BIAS1, BIAS2, BIAS3 ..... –0.3V to 6V
V_{O10}, V_{O11}, V_{O12}, V_{O20}, V_{O21}, V_{O22},
V_{O30}, V_{O31}, V_{O32} ..... –0.3V to 5.5V
EN1, EN2, EN3 ..... –0.3V to 6V
IMON1, IMON2, IMON3, IMONR1,
IMONR2, IMONR3 ..... –0.3V to 6V
PG1, PG2, PG3, PGR1, PGR2, PGR3, VIOC1 –0.3V to 6V
V_{REF1}, V_{REF2}, V_{REF3} ..... –0.3V to 6V
Operating Junction Temperature (Note 2)
E-Grade/I-Grade ..... –40°C to 125°C
H-Grade ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Maximum Reflow (Package Body) Temperature ..... 260°C

PIN CONFIGURATION



BGA PACKAGE
98-PIN (6mm × 12mm × 1.92mm)
T_{JMAX} = 150°C,
θ_{JCtop} = 15.5°C/W, $\theta_{JCbottom}$ = 3°C/W, θ_{JA} = 15°C/W, WEIGHT = 331mg

NOTES:
1. θ VALUES ARE DETERMINED BY SIMULATION PER JESD-51 CONDITIONS.
2. θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
3. SEE THE APPLICATION INFORMATION SECTION FOR LAB MEASUREMENT DERATING INFORMATION.

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4709EY#PBF	SAC305 (RoHS)	4709	e1	BGA	4	–40°C to 125°C
LTM4709IY#PBF	SAC305 (RoHS)	4709	e1	BGA	4	–40°C to 125°C
LTM4709HY#PBF	SAC305 (RoHS)	4709	e1	BGA	4	–40°C to 150°C

- Contact the factory for parts specified with wider operating temperature ranges. Pad or ball finish code is per IPC/JEDEC J-STD-609.
- This product is not recommended for second side reflow.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), C_{OUT} = 10µF, per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	0.6		5.5	V
V_{BIAS}	BIAS Voltage	(Note 3)	●	2.375		5.5	V
V_{OUT}	Regulated Output Voltage, Total Variation with Line and Load (Note 5)	V_{OUT} = 0.5V, 10mA ≤ I_{OUT} ≤ 3A, 0.70V ≤ V_{IN} ≤ 0.9V V_{OUT} = 1.0V, 10mA ≤ I_{OUT} ≤ 3A, 1.2V ≤ V_{IN} ≤ 1.4V V_{OUT} = 1.2V, 10mA ≤ I_{OUT} ≤ 3A, 1.4V ≤ V_{IN} ≤ 1.6V V_{OUT} = 3.3V, 10mA ≤ I_{OUT} ≤ 3A, 3.5V ≤ V_{IN} ≤ 3.7V V_{OUT} = 4.2V, 10mA ≤ I_{OUT} ≤ 3A, 4.4V ≤ V_{IN} ≤ 4.6V	● ● ● 	0.4925 0.988 1.182 3.2505 4.137	0.500 1.000 1.200 3.300 4.200	0.5075 1.012 1.218 3.3495 4.263	V V V V V
$\Delta V_{OUT(LINE)}$	Line Regulation to V_{IN}	V_{OUT} = 0.5V, V_{IN} = 0.7V to 5.5V, V_{BIAS} = 2.375V, I_{OUT} = 10mA V_{OUT} = 4.2V, V_{IN} = 4.4V to 5.5V, V_{BIAS} = 5.5V, I_{OUT} = 10mA	● ●			1.5 1.8	mV mV
$\Delta V_{OUT(BIAS)}$	Line Regulation to V_{BIAS}	V_{OUT} = 0.5V, V_{BIAS} = 2.375V to 5.5V, V_{IN} = 0.7V, I_{OUT} = 10mA V_{OUT} = 3.3V, V_{BIAS} = 4.5V to 5.5V, V_{IN} = 3.5V, I_{OUT} = 10mA	● ●			0.35 2.5	mV mV
$\Delta V_{OUT(LOAD)}/V_{OUT}$	Load Regulation, ΔI_{OUT} = 10mA to 3A (Note 5)	V_{BIAS} = 2.4V, V_{IN} = 1.4V, V_{OUT} = 1.2V	●			0.26	%
V_{DO}	Dropout Voltage, V_{IN} = $V_{OUT(PROG)}$, V_{BIAS} ≥ V_{OUT} + 1.2V (Note 4)	I_{OUT} = 1A, V_{IN} = V_{OUT} = 1.2V	 ●		15	22 33	mV mV
		I_{OUT} = 2A, V_{IN} = V_{OUT} = 1.2V	 ●		30	44 66	mV mV
		I_{OUT} = 3A, V_{IN} = V_{OUT} = 1.2V	 ●		45	65 100	mV mV
Minimum Load Current			●	10			mA
I_{BIAS}	BIAS Pin Current V_{IN} = 1.4V, V_{OUT} = 1.2V, V_{BIAS} = 3.3V	I_{OUT} = 10mA I_{OUT} = 3A			4 5.5	6 7.4	mA mA
$I_{BIAS(DROPOUT)}$	BIAS Pin Current in Dropout (Notes 4 and 5)	V_{BIAS} = V_{OUT} + 1.2V, V_{IN} = V_{OUT} = 1.2V, I_{OUT} = 3A V_{BIAS} = 5.5V V_{IN} = V_{OUT} = 1.2V, I_{OUT} = 3A	 ●		5.5 35	7.0 45	mA
$I_{BIAS(SHUTDOWN)}$	BIAS Pin Shutdown Mode Current	V_{BIAS} = 5.5V, EN = 0V				10	µA
I_{MON}	IMON Pin Output Current (Note 5)	I_{OUT} = 3A, V_{IN} = 1.4V, V_{OUT} = 1.2V I_{OUT} = 1A, V_{IN} = 1.4V, V_{OUT} = 1.2V	● ●	0.98 313	1.0 333.3	1.02 353	mA µA
I_{OUT}/I_{MON}	I_{OUT}/I_{MON} Ratio (Note 5)	I_{OUT} = 3A, V_{IN} = 1.4V, V_{OUT} = 1.2V I_{OUT} = 1A, V_{IN} = 1.4V, V_{OUT} = 1.2V	● ●	2970 2970	3000 3000	3030 3030	
$I_{MON(OFF)}$	IMON Shutdown Current	V_{BIAS} = 5.0V, EN = 0V				1	µA
I_{LIM}	Programmable Current Limit (Note 5)	IMONR Connected to GND R_{IMON} = 1kΩ R_{IMON} = 2kΩ	● ● ●	3.2 2.94 1.45	3.3 3.0 1.5	3.4 3.06 1.55	A A A
$V_{TH(PG)}$	V_{OUT} Threshold for Power Good	Percentage of $V_{OUT(NOMINAL)}$, V_{OUT} Rising Percentage of $V_{OUT(NOMINAL)}$, V_{OUT} Falling		91 88	93 90	95 92	% %
$V_{PG(LO)}$	Power Good V_{OL}	I_{PG} = 200µA (Fault Condition)			42	100	mV
$I_{PG(LK)}$	Power Good V_{OH} Leakage	V_{PG} = V_{BIAS} = 5V				1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), C_{OUT} = 10µF, per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{REF(START-UP)}$	Fast Start-Up Ref Pin Current				2		mA
$V_{TH(START-UP)}$	Fast Start-Up Turn Off Threshold	Measured as Percentage of Final REF Pin Voltage	●	96	98.9	101.5	%
UVLO (BIAS)	V_{BIAS} Undervoltage Lockout	EN = V_{BIAS}, V_{IN} = 0.9V, V_{OUT} = 0.5V, V_{BIAS} Rising EN = V_{BIAS}, V_{IN} = 0.9V, V_{OUT} = 0.5V, V_{BIAS} Falling	● ●	2.16 2.02	2.21 2.06	2.25 2.10	V V
V_{IOC}	Input to Output Differential Voltage Control	V_{IOC} Amplifier Gain V_{IOC} Amplifier Offset V_{IOC} Pin Source Current: V_{BIAS} > V_{IOC} + 1V V_{IOC} Pin Sink Current: V_{BIAS} > V_{IOC} + 1V	 ● ● 	 790 200 	1 800 20	 810 	V/V mV µA µA
V_{OL}	Logic-0 State of V_{O10}, V_{O11}, V_{O12}, V_{O20}, V_{O21}, V_{O22}, V_{O30}, V_{O31}, V_{O32}		●			0.3	V
V_{OZ}	Logic-Hi-Z State of V_{O10}, V_{O11}, V_{O12}, V_{O20}, V_{O21}, V_{O22}, V_{O30}, V_{O31}, V_{O32}		●	0.95		1.15	V
V_{OH}	Logic-1 State of V_{O10}, V_{O11}, V_{O12}, V_{O20}, V_{O21}, V_{O22}, V_{O30}, V_{O31}, V_{O32}		●	1.9			V
I_{CTRL}	Pin Current of V_{O10}, V_{O11}, V_{O12}, V_{O20}, V_{O21}, V_{O22}, V_{O30}, V_{O31}, V_{O32}	Apply 2.5V to Output Control Pins				50	µA
V_{EN}	EN Pin Threshold	EN Rising, V_{BIAS} = 2.375V Hysteresis	●	1.20	1.26 80	1.32	V mV
I_{EN}	EN Pin Current	V_{EN} = 0V, V_{BIAS} = 5.5V V_{EN} = 1.3V, V_{BIAS} = 5.5V V_{EN} = 5.5V, V_{BIAS} = 0V	 	 	 0.1 10	±1 20	µA µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4709 is tested under pulsed loading conditions such that $T_J \approx T_A$. The LTM4709E is guaranteed to meet performance specifications from 0°C to 125°C operating junction temperature range. The LTM4709E specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4709I is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range, and the LTM4709H is guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: To maintain proper performance and regulation, the BIAS supply voltage must be higher than the input voltage V_{IN}. For the output voltage V_{OUT}, the BIAS voltage must satisfy the following conditions: 2.375V ≤ V_{BIAS} ≤ 5.5V and V_{BIAS} ≥ (V_{OUT} + 1.2V).

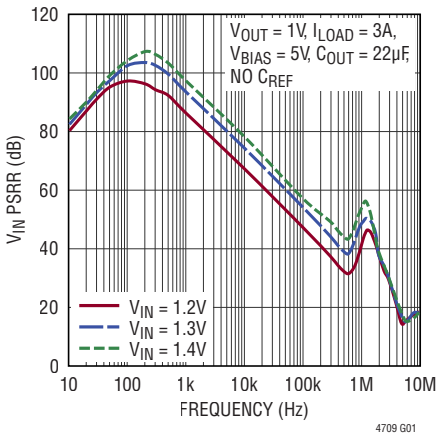
Note 4: Dropout voltage, V_{DO}, is the minimum input-to-output voltage difference at a specified output current. In dropout, the output voltage equals $V_{IN} – V_{DO}$.

Note 5: Operating conditions are limited by maximum junction temperature. See output current thermal derating curves for different V_{IN}, V_{OUT}, and T_A in Figure 7 to Figure 13. The regulated output voltage specification does not apply to all possible combinations of input voltage and output current. When operating at maximum output current, limit the input voltage range to $V_{IN} – V_{OUT}$ ≤ 300mV.

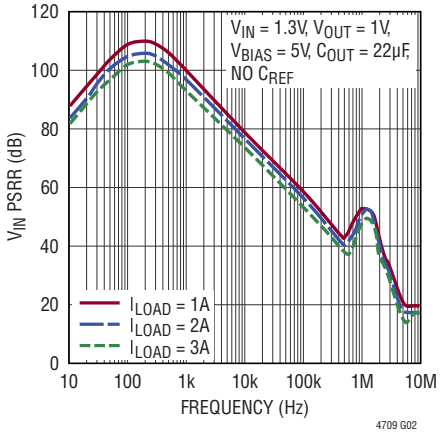
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

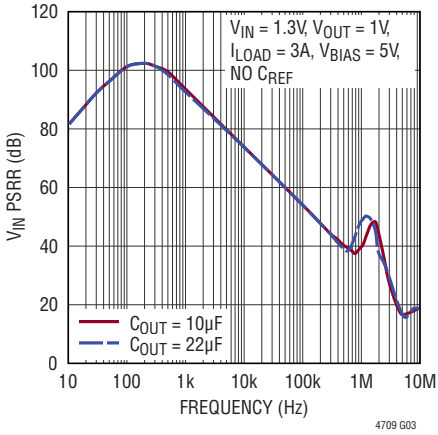
V_{IN} PSRR with Various $V_{IN} – V_{OUT}$



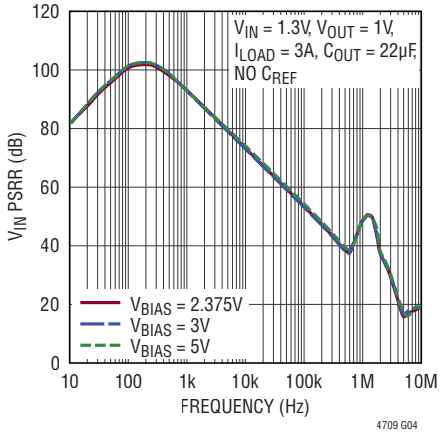
V_{IN} PSRR with Various Load Current



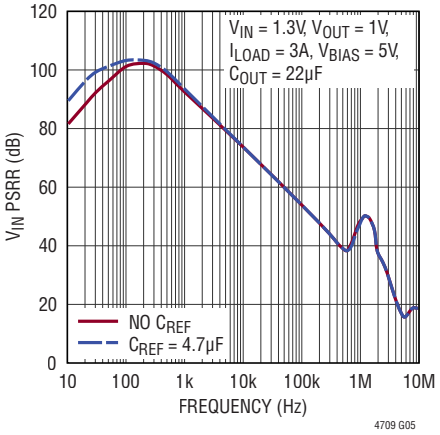
V_{IN} PSRR with Various C_{OUT}



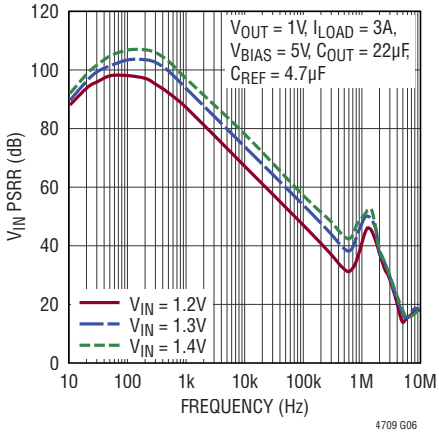
V_{IN} PSRR with Various V_{BIAS}



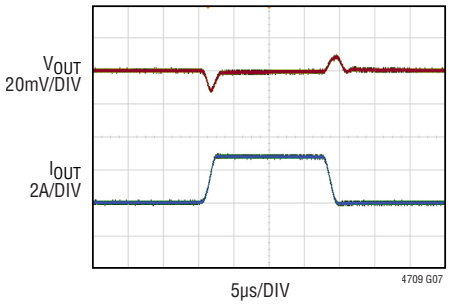
V_{IN} PSRR with Various C_{REF}



V_{IN} PSRR with 4.7µF C_{REF} and Various $V_{IN} – V_{OUT}$

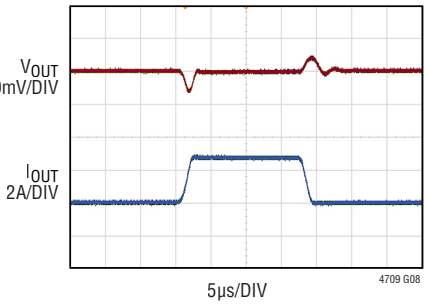


Load Transient Response with 10µF C_{OUT}



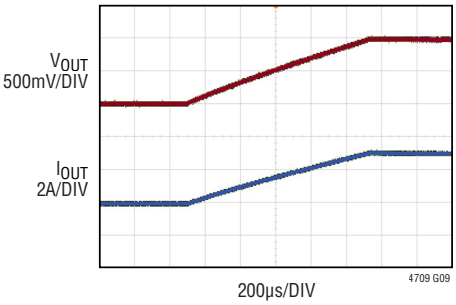
V_{IN} = 1.3V, V_{OUT} = 1V, V_{BIAS} = 5V
C_{OUT} = 10µF CERAMIC CAPACITOR
NO EXTERNAL V_{REF} CAPACITOR
LOAD STEP 0.3A TO 3A WITH SLEW RATE OF 3A/µs

Load Transient Response with 22µF C_{OUT}



V_{IN} = 1.3V, V_{OUT} = 1V, V_{BIAS} = 5V
C_{OUT} = 22µF CERAMIC CAPACITOR
NO EXTERNAL V_{REF} CAPACITOR
LOAD STEP 0.3A TO 3A WITH SLEW RATE OF 3A/µs

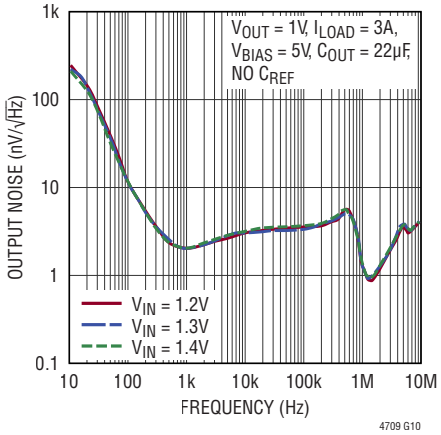
Start-Up with Full Load



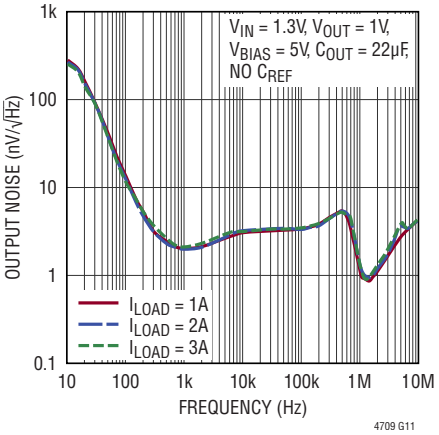
V_{IN} = 1.3V, V_{OUT} = 1V, V_{BIAS} = 5V
C_{OUT} = 10µF CERAMIC CAPACITOR
NO EXTERNAL V_{REF} CAPACITOR

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

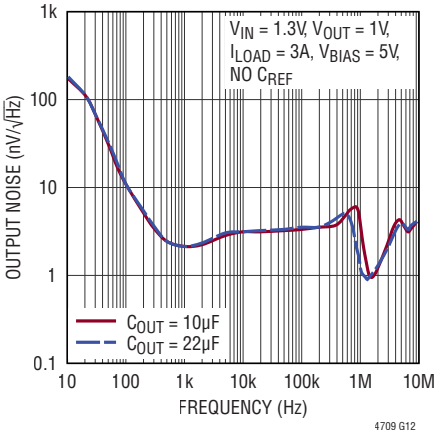
Noise Spectrum Density with Various $V_{IN} - V_{OUT}$



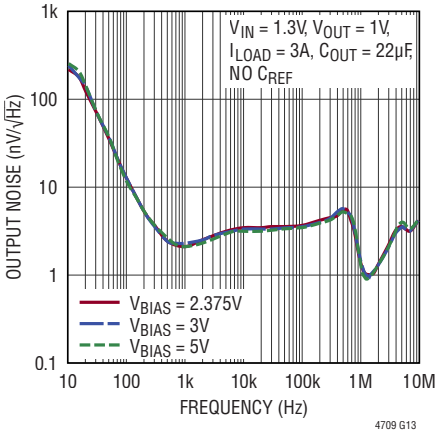
Noise Spectrum Density with Various Load



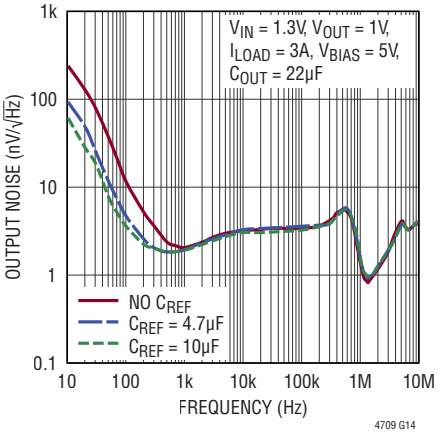
Noise Spectrum Density with Various C_{OUT}



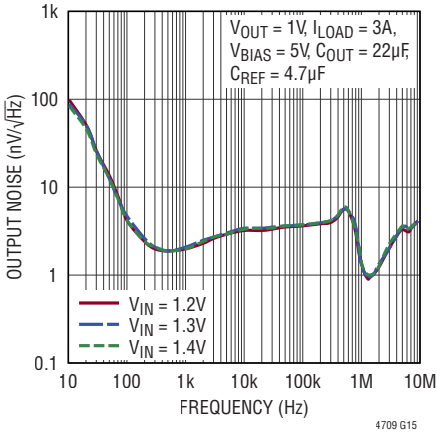
Noise Spectrum Density with Various V_{BIAS}



Noise Spectrum Density with Various C_{REF}



Noise Spectrum Density with 4.7uF C_{REF} and Various $V_{IN} - V_{OUT}$



PIN FUNCTIONS

NC (Pin A1): Not Connected. Do not connect this pin. Leave the pin floating.

IMONR1, IMONR2, IMONR3 (Pins A2, F2, L2): Current Limit Resistor Connected to IMON. A 1% accuracy 909Ω resistor is integrated inside the module between these pins and IMON pin. Directly connect these pins to GND to set the current limit at 3.3A. To set the current limit lower than 3A, select a resistor based on the pin description for IMON, leave the IMONR pin floating, and connect the resistor between the IMON pin and GND.

PGR1, PGR2, PGR3 (Pins A3, F3, L3): Pull-Up Resistor Connected to PG1,2,3 (Pins E7, E2, K1). A 100k resistor is integrated inside the module between these pins and PG pins. Directly connect these pins to BIAS or any rail to pull up PG pins.

BIAS1, BIAS2, BIAS3 (Pins A4, F4, L4): Bias Supply. These pins supply current to the internal control circuitry and the gate driving of the pass transistor. The three pins could be connected together. To ensure proper operation, the BIAS voltage must satisfy the following conditions: $2.375V \le V_{BIAS} \le 5.5V$ and $1.2 + V_{OUT} \le V_{BIAS}$.

IMON1, IMON2, IMON3 (Pins A5, F5, L5): Output Current Monitor. The IMON pins source a current that typically equals to $I_{OUT}/3000$. If IMONR is floating, connect these pins with a resistor to GND to produce a voltage proportional to I_{OUT}. Current limiting is triggered when the voltage at these pins reaches 1V. The current limit equals to 3000/resistance. For example, with a 1.5k resistor to GND, these pins set the current limit at 2A.

These pins are internally connected to an IMONR pin with a 1% accuracy 909Ω resistor. Users can directly connect the IMONR pin to GND to set the current limit at 3.3A.

V_{REF1}, V_{REF2}, V_{REF3} (Pins A6, F6, L6): Reference Filter. These pins have been connected to GND internally with a 2.2µF ceramic capacitor to decrease the output noise and provide a soft-start function to the reference. No additional ceramic capacitor is required, and it can be left floating in the application. Additional capacitor C_{REF} at this pin is optional. Additional C_{REF} could be added if lower noise below 1kHz is desired. For most applications, no C_{REF} is needed.

GND (Pins B1, B2, A7, B7, G1, G2, F7, G7, M1, M2, L7, M7): Ground. To ensure proper performance, tie all GND pins to the PCB ground.

V_{IN1}, V_{IN2}, V_{IN3} (Pins B3, B4, C1–C4, D1–D4; G3, G4, H1–H4, J1–J4; M3, M4, N1–N4, P1–P4): Input Supply. These pins supply power to the high current pass transistor. The V_{IN} pins can be connected together or separate. The LTM4709 requires a decoupling capacitor at V_{IN} to maintain stability and lower input impedance over frequency. An input bypass capacitor of no less than 4.7µF is recommended for most applications. Minimize the trace inductance between the decoupling capacitor and this pin to optimize performance. The application that operates with low $V_{IN} – V_{OUT}$ voltage difference or that has large and fast transient step may require higher input capacitance to prevent the input supply from drooping.

V_{OUT1}, V_{OUT2}, V_{OUT3} (Pins B5, C5–C7, D5–D7; Pins G5, H5–H7, J5–J7; Pins M5, N5–N7, P5–P7): Output. These pins supply power to the load. A minimum output capacitance of 10µF is required for stability. It is recommended to place low ESR X5R or X7R dielectric ceramic capacitors directly between these pins and GND pins for best performance. The large load step requires higher output capacitance to meet transient requirements.

V_{OUTS1}, V_{OUTS2}, V_{OUTS3} (Pins B6, G6, M6): Kelvin Sense for Output. These pins are the inverting input to the error amplifier. Optimum regulation is obtained when it is connected to the V_{OUT} pins of the regulator. In some applications, the resistance of PCB traces between the regulator and the load causes small voltage drops, creating a load regulation error at the point of load. Connecting these pins directly to the load to eliminate the voltage error.

VIOC1 (Pin E1): Voltage for In-to-Out Control. This pin can be used to control the upstream buck regulator to maintain a constant voltage for channel 1 of LTM4709 and hence minimize its power dissipation. It can also be used to control multiple channels when they are in parallel. See Applications Information section for more information on this function.

PIN FUNCTIONS

EN1, EN2, EN3 (Pins E3, F1, L1): Device Enable. These pins enable/disable the output. Pulling the EN pin low disables the output transistor and auxiliary functions. Drive the EN pin with a digital logic port, an open-collector NPN or an open-drain N-channel MOSFET terminated with a pull-up resistor to BIAS. The pull-up resistor must be less than 200k to meet the V_{OH} condition of the EN pin. If unused, connect the EN pin to BIAS.

V_{O10}, V_{O11}, V_{O12}, V_{O20}, V_{O21}, V_{O22}, V_{O30}, V_{O31}, V_{O32} (Pins E4, E5, E6, K5, K6, K7, K2, K3, K4): Output Voltage Select. These three-state pins combine to select a nominal output voltage from 0.5V to 4.2V. The input logic low threshold is less than 300mV referenced to GND and the logic high threshold is greater than 1.9V. The range between 0.95V and 1.15V defines the logic Hi-Z state. See Table 1 in the Applications Information section that defines the V_{OUT} versus output voltage select pins.

PG1, PG2, PG3 (Pins E7, E2, K1): Power Good. The PG pins are an open-drain N-channel MOSFET output that is pulled low if one of the following fault modes is detected.

- V_{OUT} is less than 93% of $V_{OUT(NOMINAL)}$ on the rising edge of V_{OUT}.
- V_{OUT} is less than 90% of $V_{OUT(NOMINAL)}$ on the falling edge of V_{OUT}.
- Voltage at BIAS pin is less than its undervoltage lockout threshold.
- Junction temperature exceeds 168°C typically.

These pins are internally connected to PGR1,2,3 (Pins A3, F3, L3) with a 100k resistor.

BLOCK DIAGRAM

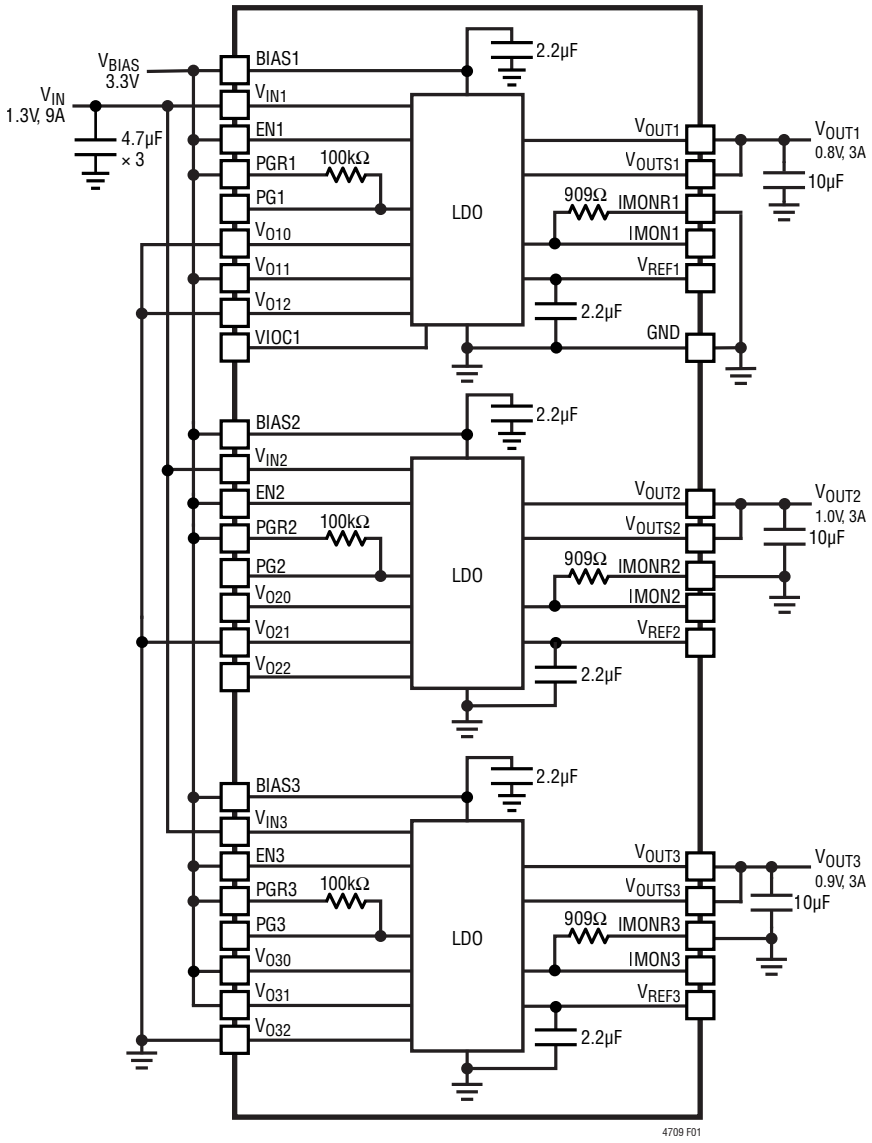


Figure 1. LTM4709 Block Diagram

OPERATION

The LTM4709 is a high-density, low voltage, triple 3A µModule linear regulator that offers high PSRR, ultralow noise, and ultrafast transient response. The device supplies up to 9A output current with a typical dropout voltage of 45mV. Output voltage noise of 1.3µV_{RMS} (BW = 10Hz to 100kHz) is achieved with no reference bypass capacitor required. The power supply rejection ratio (PSRR) at 1MHz is 51dB at full load with 300mV difference between input and output. The LTM4709's high bandwidth provides an ultrafast transient response that only requires just a single ceramic output capacitor (10µF minimum), saving bulk capacitance, PCB area, and cost. LTM4709 has the industry's best performance of high-frequency PSRR and low-frequency RMS noise at its current range and provides 9A output current in a compact size with outstanding thermal performance.

New generation of FPGA and ASIC processors place stringent demands on the power supplies for the core, ADCs, DACs, low noise amplifier, and transceiver channels. These applications require a power supply with a fast transient response and low noise. The processor load may change from near zero to a few amps in hundreds of nanoseconds. Output voltage specifications, especially in the 1V range, require tight tolerances on the transient response. The supply voltages need to have low noise and high bandwidth to achieve the low bit-error rates. These requirements mandate the need for high current, accurate, ultralow noise, ultrafast regulator operating at low input and output voltages.

The LTM4709 is ideal for high-performance FPGAs, microprocessors, noise-sensitive power supplies, and high-current applications that operate over low input and output voltages. Output voltage for the LTM4709 is digitally selectable in 50mV increments from 0.5V to 1.2V; 100mV increments from 1.2V to 1.8V; and discrete levels at 2V, 2.5V, 3V, 3.3V, and 4.2V. The LTM4709 provides a precision output current monitor with ±2.4% accuracy at 3A per channel. Terminating the current monitor (IMON) pin to GND with a resistor produces a voltage proportional to the output current, which allows for the measurement of the output current.

The LTM4709 incorporates a unique tracking function which controls the output voltage of an upstream switching regulator powering the LTM4709's input (see Figure 2 and Figure 3). This tracking function drives the upstream switching regulator to maintain a constant voltage across LTM4709. This input-to-output voltage control allows the user to change the output voltage of LTM4709, maximize the efficiency, and maintain the high PSRR performance.

The LTM4709's architecture drives an internal N-channel power MOSFET as a source follower. This configuration permits a user to have an extremely low dropout, ultrafast transient response with excellent PSRR performance, as well as providing significant cost savings on the PCB and external components. LTM4709 internal protection includes undervoltage lockout (UVLO), precision current limiting with power foldback and thermal shutdown. The LTM4709 is offered in a compact size of 6mm × 12mm × 1.92mm. It offers excellent thermal performance with less than 70°C junction temperature at 9A output current and ambient temperature of 25°C (see Figure 5). For applications where high ambient temperature (>70°C) is required, the 150°C rated version of LTM4709 is available.

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The LTM4709 is a low voltage, ultralow noise, and ultrafast transient response µModule linear regulator. The device supplies up to triple 3A with a typical dropout voltage of 45mV. The high bandwidth and high PSRR allow for the use of a single small ceramic capacitor for input and output, saving bulk capacitance, space, and cost. The LTM4709 is ideal for high-performance FPGAs, microprocessors, RF communication and noise-sensitive supply applications.

Output Voltage

Output voltages are digitally selectable in 50mV increments from 0.5V to 1.2V; 100mV increments from 1.2V to 1.8V; and discrete levels at 2V, 2.5V, 3V, 3.3V and 4.2V. The tri-level input pins, V_{O10}, V_{O11}, V_{O12}, V_{O20}, V_{O21}, V_{O22}, V_{O30}, V_{O31}, V_{O32} set the output voltage. Table 1 illustrates the three-bit digital word to output voltage relationship based on setting these pins high, low, or floating. An input logic low state is guaranteed with less than 300mV referenced to GND and a logic high state is guaranteed with greater than 1.9V. The range from 950mV to 1.15V defines the logic Hi-Z (input floating) state. These pins may be tied high by either pin strapping them to BIAS*n* or driving them with digital ports. Pins that float may either float or require logic that has Hi-Z output capability. This allows the output voltage to be dynamically changed if necessary.

Voltage Reference

The voltage reference $V_{REF1,2,3}$ pin is the voltage output of the internal current reference feeding into a resistor. A 2.2µF ceramic capacitor has been integrated between the V_{REF} and GND inside the LTM4709 to decrease the reference voltage noise and soft-start the output when the device is enabled. The V_{REF} pin must not be DC loaded by anything except for applications that need to be paralleled with other channels. See the Paralleling Devices for Higher Output Current section for more details.

Table 1. V_{OUT} Selection Matrix

V_{OUT} (V)	V_{OX0}	V_{OX1}	V_{OX2}
0.500	0	0	0
0.550	Z	0	0
0.600	1	0	0
0.650	0	Z	0
0.700	Z	Z	0
0.750	1	Z	0
0.800	0	1	0
0.850	Z	1	0
0.900	1	1	0
0.950	0	0	Z
1.000	Z	0	Z
1.050	1	0	Z
1.100	0	Z	Z
1.150	Z	Z	Z
1.200	1	Z	Z
1.300	0	1	Z
1.400	Z	1	Z
1.500	1	1	Z
1.600	0	0	1
1.700	Z	0	1
1.800	1	0	1
2.000	0	Z	1
2.500	Z	Z	1
3.000	1	Z	1
3.300	0	1	1
4.200	Z	1	1

Note: X is 1, 2, or 3 representing channel; 0 = Low, Z = Hi-Z (Float), 1 = High.

Enable

The EN1,2,3 pin enables/disables the output and reference pin. Pulling EN pin low places the regulator into shutdown mode. In shutdown mode, the quiescent current decreases to less than 10µA.

Drive the EN pin with either a digital logic port, an open-collector NPN or an open-drain NMOS terminated with a pull-up resistor to BIAS1,2,3. The pull-up resistor must be less than 200k to meet the V_{OH} condition of the EN pin. If not used, connect the EN pin to BIAS.

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Bias Undervoltage Lockout

An internal undervoltage lockout (UVLO) comparator monitors the BIAS1,2,3 pin. If BIAS drops below the UVLO threshold, all functions shut down, the pass transistors are off, and output currents fall to zero. The typical BIAS pin UVLO threshold is 2.21V on the rising edge of BIAS. The UVLO circuit incorporates about 150mV of hysteresis on the falling edge of BIAS.

High-Efficiency Linear Regulator: Input-to-Output Voltage Control (VIOC)

The VIOC1 pin is used to control an upstream switching converter to maintain a constant voltage across the LTM4709. This maximizes efficiency while maintaining high PSRR performance. The VIOC1 pin voltage equals to (V_{IN} – V_{OUT}) + 800mV, where V_{IN} and V_{OUT} are input voltage and output voltage of LTM4709. The basic operation of VIOC is shown in Figure 2. In the case that the internal reference voltage of the upstream switching regulator $V_{REFSW} \geq 1V$, just tie the VIOC1 pin to the feedback pin V_{FB} of the switching regulator. This will regulate the LTM4709's input-to-output difference to the switching regulator's internal reference voltage V_{REFSW} minus 800mV. When paralleling multiple channels of a single or multiple LTM4709, just connect the VIOC1 pin to the upstream switching regulator's feedback pin to achieve the VIOC function for all paralleled channels. When the LTM4709 is used for separate outputs, only channel 1 has a VIOC function. Channel 2 and Channel 3 do not have a VIOC function when the module is operating in separate outputs.

While the VIOC buffer is inside the switching converter's feedback loop, given the VIOC buffer's high bandwidth, the switching converter's frequency compensation doesn't need to be adjusted. Phase delay through the VIOC buffer is typically less than 2° for frequencies as high as 100kHz. Hence, the VIOC buffer will be transparent and just act like an ideal wire within the switching converter's bandwidth (which is usually less than 100kHz).

For example, for a switching converter with less than 100kHz bandwidth and a phase margin of 50°, using the VIOC buffer, the phase margin will degrade by at most 2°. The phase margin for the switching converter (using the VIOC pin) will be at least 48°. Given the VIOC buffer is inside the switching converter's feedback loop, the total capacitance on the VIOC pin is required to be below 20pF.

As shown in Figure 3, the input-to-output differential voltage is easily programmable to support different application needs (PSRR vs power dissipation) using Equation 1.

$$V_{IN1} - V_{OUT1} + 0.8V = V_{REFSW} \bullet \left(\frac{R1 + R2}{R1}\right) \qquad (1)$$

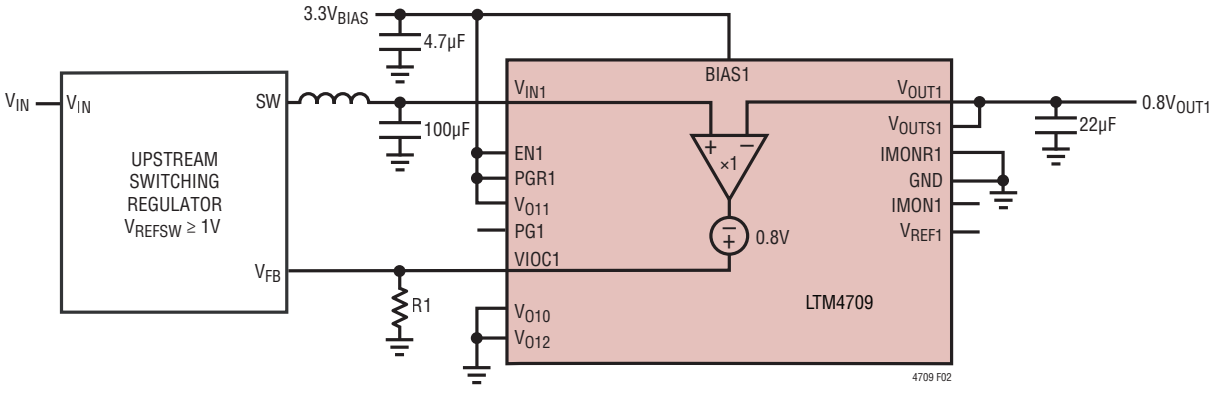

Figure 2. Input-to-Output Voltage Control (VIOC) Basic Operation

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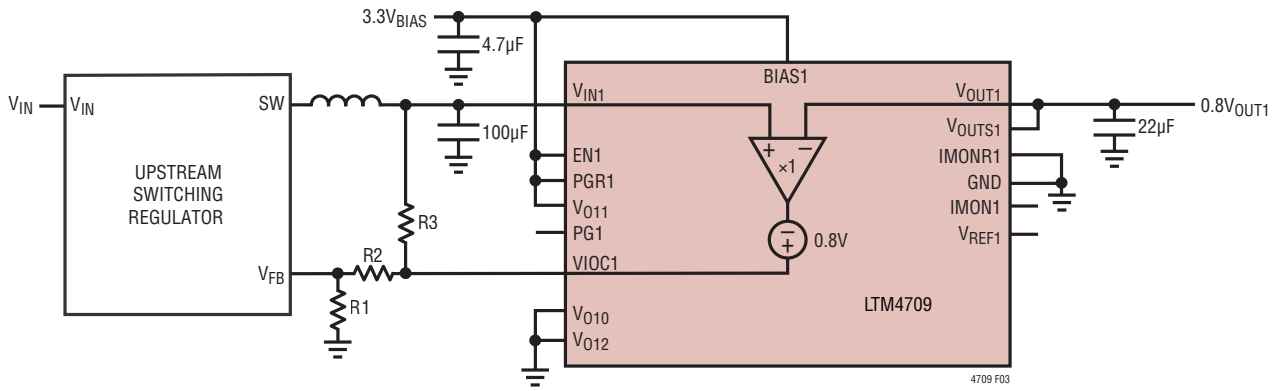

Figure 3. Programming Input-to-Output Difference

Furthermore, if the LTM4709 EN pin shorts to GND, the LTM4709 input voltage can rise up to the switcher's input voltage, and thus potentially exceed the LTM4709's absolute maximum rating. To prevent this, the maximum LTM4709 input voltage $V_{MAXLDOIN}$ can be set using a resistor R3 between the VIOC1 and the input pin of the LTM4709 (see Equation 2).

$$V_{MAXLDOIN} = V_{REFSW} \bullet \left(\frac{R1 + R2 + R3}{R1}\right) \quad (2)$$

The VIOC1 pin is capable of sourcing 200µA. Choose R1 and R3 values such that the VIOC1 pin sources at least 10µA to ensure system stability. See Figure 17 for a typical application to use an upstream switching regulator and LTM4709 with VIOC function.

Power Good

The PG1,2,3 pin is an open-drain NMOS output that actively pulls low if EN is low or if one of the following fault modes is detected.

- V_{OUT} is less than 93% of $V_{OUT(NOMINAL)}$ on the rising edge.
- V_{OUT} is less than 90% of $V_{OUT(NOMINAL)}$ on the falling edge.
- BIAS is less than its undervoltage lockout threshold.
- Junction temperature exceeds 168°C typically.

Stability and Output Capacitance

The LTM4709 feedback loop requires a minimum output capacitance of 10µF for stability. It is recommended to mount low ESR X5R or X7R ceramic capacitors close to the LTM4709 V_{OUT} and GND pins. Use wide copper planes for V_{OUT} and GND to minimize parasitic inductance. If possible, mount the module adjacent to the load to minimize distributed inductance for optimal load transient performance. Additional ceramic capacitors distributed around the load are recommended.

For many applications that LTM4709 best fit, such as FPGA, ASIC processor, or DSP supplies, typically require a high-frequency decoupling capacitor network for the device being powered. This network generally consists of many low-value ceramic capacitors in parallel. Multiple low-value capacitors in parallel present a favorable frequency characteristic that reduces the parasitic inductance of the capacitors.

Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients as shown in Figure 4. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature

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range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor.

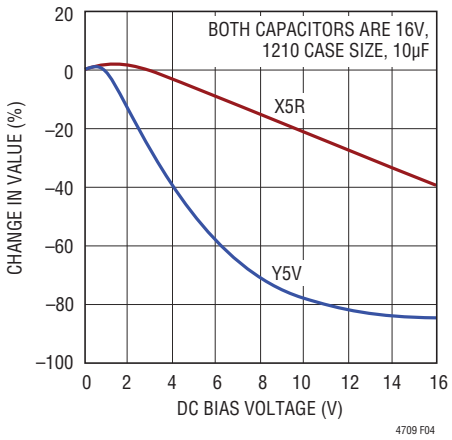

Figure 4. Ceramic Capacitor DC Bias Characteristics

The X7R type has better stability across temperatures, while the X5R is less expensive and is available in higher values. Care still must be taken when using X5R and X7R capacitors; the X5R and X7R codes only specify the operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases but expected capacitance at operating voltage should be verified. Voltage and temperature coefficients are not the only source of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates a voltage across its terminals due to mechanical stress, like the way a piezoelectric microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

Stability and Input Capacitance

The LTM4709 is stable with a minimum capacitance of 4.7µF connected to the V_{IN} pins. Use low ESR capacitors to minimize instantaneous voltage drops under large load step conditions. Large V_{IN} droop during transient may cause the regulator to enter dropout with the corresponding degradation in load transient response. Additional input and output capacitance may be necessary depending on an application's requirements. Sufficient input capacitance is critical as the circuit is intentionally operated close to dropout to minimize power. Ideally, the output impedance of the supply that powers V_{IN} should be less than 20mΩ to support a large change in the load step.

In case where wire is used to connect a power supply to the input of the LTM4709 (and from the ground of the LTM4709 back to the power supply ground), large input capacitors are required to avoid an unstable application. This is due to the inductance of the wire forming an LC tank circuit with the input capacitor and not a result of the LTM4709 being unstable. The self-inductance is directly proportional to its length. The width of a routing trace does not have a major influence on its self-inductance as compared to its length. For example, 1 inch of 18-AWG, 0.04-inch-wide routing trace has 28nH of self-inductance. The self-inductance of a 2-AWG trace with a width of 0.26-inch is about half the inductance of the 18-AWG wire. The overall self-inductance of a trace can be reduced in two ways. One is to divide the current flow toward the LTM4709 between two parallel conduction paths. In this case, the farther the wires are placed apart from each other, the more the inductance is reduced, up to a 50% reduction when placed a few inches apart. Splitting the wires basically connects two equal inductors in parallel. However, when placed near each other, mutual inductance is added to the overall self-inductance of the wires. The most effective way to reduce overall inductance is to place the forward and returning conductors (the trace for the input and the trace for the return ground) in very close proximity. In this case, two 18-AWG wires separated by 0.05-inch reduces the overall self-inductance to about one-fourth of a single trace. If the LTM4709 is powered by a battery mounted in proximity with ground and power planes on the same circuit board, a 10µF input capacitor is sufficient for stability. If, however, the LTM4709 is powered by a distant supply, use a low ESR, large value input capacitor in the order of 220µF.

Bias Requirement

The BIAS1,2,3 pin supplies current to the internal control circuitry and the output stage driving the pass transistor.

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A 2.2µF bypass capacitor has already been integrated between the BIAS pin and GND inside the LTM4709, so no bypass capacitor is needed on the BIAS pin. To ensure proper operation, the BIAS voltage must satisfy the following conditions: 2.375V ≤ V_{BIAS} ≤ 5.5V and V_{BIAS} ≥ (V_{OUT} + 1.2V). For V_{OUT} ≤ 1.15V, the minimum BIAS voltage is limited to 2.375V.

Load Regulation

The LTM4709 corrects for parasitic package and PCB I-R drops when the $V_{OUTS1,2,3}$ pin is Kelvin connected to the remote load. The LTM4709 handles moderate levels of output line impedance, but excessive impedance between V_{OUT} and C_{OUT} causes a phase shift in the feedback loop and adversely affects stability.

PCB Layout Considerations

Given the LTM4709's high bandwidth and high PSRR, care must be taken to the PCB layout of the application circuit to fully employ the high-performance of LTM4709. Figure 14 shows a recommended layout that delivers the best performance of the µModule. Refer to the DC3211A evaluation board demo manual for further details.

Protection Features

The LTM4709 has an internal current limit that typically clamps output current to 3.3A when the IMONR pin is connected to GND. In addition, the LTM4709 has a ±2.4% accurate programmable precision current limit. If the ambient temperature is high enough, the die junction temperature can exceed the maximum operation temperature of LTM4709. If this occurs, the LTM4709 relies on an internal thermal safety feature. At 168°C typically, the LTM4709 thermal shutdown is triggered, and the output is shut down until the IC temperature falls below its thermal hysteresis which is 7°C.

Current Monitor and Externally Programmable Current Limit

The current limit threshold voltage on the IMON1,2,3 pin is 1V. Connecting a resistor from IMON to GND sets the maximum current flowing out of the IMON pin, which in turn programs the LTM4709's current limit. If the IMONR pin is connected to GND with the IMON pin floating, it directly programs the current limit to 3.3A. The current limit equals to 3000/resistance. For example, with a 1.5k resistor to GND, the current limit is set at 2A. The voltage at the IMON pin, V_{IMON}, can be used to monitor output current I_{OUT} as well. By connecting the resistor R between IMON and GND, output current I_{OUT} can be calculated with Equation 3.

$$I_{OUT} = \frac{V_{IMON} \bullet 3000}{R} \quad (3)$$

Paralleling Devices for Higher Output Current

Multiple outputs of a single LTM4709 or multiple LTM4709 can be paralleled to obtain a higher output current. To achieve the paralleling, tie the V_{IN} pins and the V_{REF} pins of the multiple devices together. The output of the LTM4709 needs to be connected to a common load using a small ballast resistor (2mΩ), beyond the feedback V_{OUTS} pin of each channel. The ballast resistor ensures output current sharing. See the circuit schematic (Figure 17) for parallel operation.

Output Noise

The LTM4709 offers many advantages with respect to noise performance. Traditional linear regulators have several sources of noise. The most critical ones are from the voltage reference, error amplifier, and the resistor divider network used to set the output voltage. Inside the LTM4709, a 2.2µF bypass capacitor is connected between V_{REF} and GND to filter out voltage reference noise, resulting in a low output noise set just by the error amplifier's noise – typically 1.3µV_{RMS} in a frequency range from 10Hz to 100kHz.

Filtering High-Frequency Spikes

For applications where the LTM4709 is used to post regulate a switching converter, its high PSRR effectively suppresses any noise present at the switcher's switching frequency – typically 100kHz to 1MHz. However, the very high frequency (hundreds of MHz) spikes – beyond the LTM4709's bandwidth associated with the switcher's power switch transition times will almost directly pass

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through the LTM4709. While the output capacitor is partially intended to absorb these spikes, its equivalent series inductance (ESL) will limit its ability at these frequencies. A ferrite bead or even the inductance associated with a short (e.g., 0.5-inch) PCB trace between the switcher's output and the LTM4709's input can serve as an LC-filter to suppress these very high-frequency spikes.

Fast Start-Up

For ultralow noise applications that require low 1/f noise (i.e., at frequencies below 100Hz), a larger value V_{REF} pin capacitor is required, up to 22µF. While this would normally significantly increase the regulator's start-up time, the LTM4709 incorporates fast start-up circuitry that increases V_{REF} pin current to 2mA during start-up. For a 22µF capacitor, this will reduce the startup time from 100ms to 5ms.

The 2mA current source remains engaged until V_{REF} is 100% of its final value on the rising edge, and it will restart when V_{OUT} is below 94% of output setting on the falling edge, unless the regulator is in current limit, thermal shutdown, or UVLO situation.

Thermal Considerations and Output Current Derating

For application in high ambient temperature, care should be taken in the PCB layout to ensure good heat transfer from LTM4709 to the PCB. The V_{IN} and V_{OUT} should be connected to large copper layers below with thermal vias. The die temperature can be estimated by multiplying the LTM4709 power dissipation by the thermal resistance from the junction to the ambient.

The thermal picture when the LTM4709 is mounted on the EVAL-LTM4709-BZ evaluation board and is operating at $1.3V_{IN}$, $1V_{OUT}$, and 9A load current with three channels in parallel is shown in Figure 5. The highest temperature of the module top case is 66°C and the currents of the three channels are well balanced.

The internal overtemperature protection monitors the junction temperature of the LTM4709. If the junction temperature reaches 168°C, the LTM4709 output is shut down until the temperature drops by 7°C.

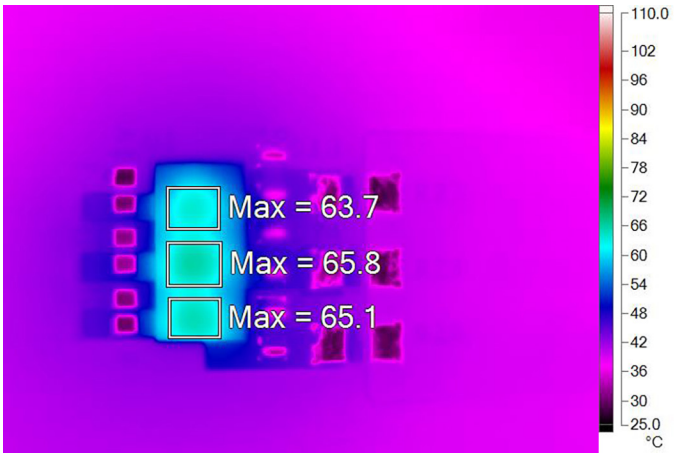

Figure 5. Thermal Image, Full Load with Three Channels in Parallel ($1.3V_{IN}$, $1V_{OUT}$, 9A) without Fan, T_A = 25°C

The thermal resistances reported in the Pin Configuration section are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients can be found in JESD51-12 (Guidelines for Reporting and Using Electronic Package Thermal Information).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in-and-of themselves, not relevant to providing guidance of thermal performance; instead, the derating curves (Figure 7 to Figure 13) can be used in a manner that yields insight and guidance pertaining to one's application usage and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives three thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below.

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in one cubic foot sealed

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enclosure. This environment is sometimes referred to as **still air**, although natural convection causes the air to move. This value is determined with the part mounted to a four-layer EVAL-LTM4709-BZ evaluation board.

2. $\theta_{JCbottom}$, the thermal resistance from the junction to the bottom of the product case, is determined with all the component power dissipation flowing through the bottom of the package. In the typical module regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don't generally match the user's application.

3. θ_{JCtop}, the thermal resistance from the junction to the top of the product case, is determined with all the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don't generally match the user's application.

A graphical representation of the thermal resistances is shown in Figure 6; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

As a practical matter, it should be clear to the reader that no individual or subgroup of the three thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through the bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, most of the heat flow is into the board.

Within the LTM4709 module, be aware that there are multiple power devices dissipating power, with the consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software defined JEDEC environment consistent with JSED51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4709 with and without airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model,

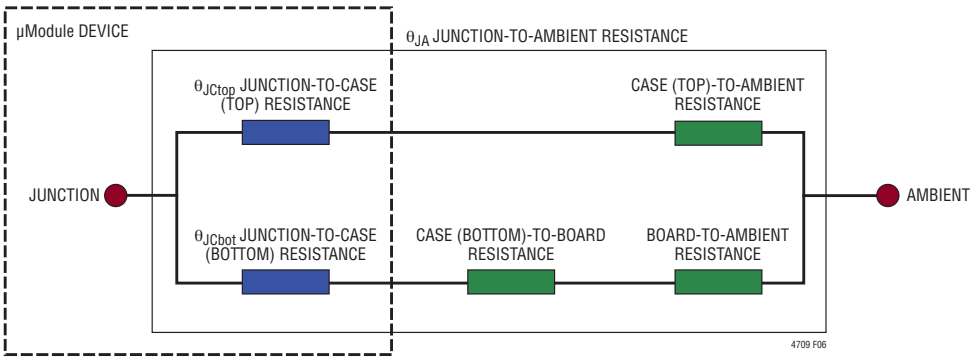


Figure 6. Graphical Representation of JESD51-12 Thermal Coefficients, Including JESD51-12 Terms

APPLICATIONS INFORMATION

a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as simulated. An outcome of this process and due diligence yields a set of derating curves (see Figure 7 to Figure 13).

After these laboratory tests have been performed and correlated to the LTM4709 model, then the θ_{JA} is provided assuming approximately 100% of the power loss flows from the junction through the board into the ambient with no airflow or top-mounted heat sink.

The load current derating curves are shown in Figure 7 to Figure 13. The maximum load current is achievable while increasing ambient temperature if the junction temperature is less than 145°C, which is 5°C guard band from the maximum junction temperature of 150°C. When the ambient temperature reaches a point where the junction temperature is 145°C, then the load current is lowered to maintain the junction at 145°C while increasing the ambient temperature up to 140°C. The derating curves are plotted with three channels in parallel, total current starting at full load 9A, and the ambient temperature at 25°C. The input-to-output differential voltages are 200mV, 250mV, 300mV, 400mV, 500mV, 600mV, 700mV. These are chosen to include the lower and higher output voltage ranges. Thermal models are derived from several temperature measurements in a controlled temperature chamber, along with thermal modeling analysis. The junction temperatures are monitored while the ambient temperature is increased with and without airflow. The decreased output current will decrease the internal module loss as ambient temperature is increased. Table 2 provides equivalent thermal resistances for with and without airflow. LTpowerCAD offers an empirical thermal model for thermal estimation based on the EVAL-LTM4709-BZ evaluation board as well. The printed circuit board is a 1.6mm thick four layers board with two-ounce copper for all four layers. The PCB dimensions are 114mm × 124mm.

Table 2. Derating Curve at Various $V_{IN} – V_{OUT}$

DERATING CURVE	$V_{IN} – V_{OUT}$ (V)	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 7	0.2	0	None	15
Figure 8	0.25			
Figure 9	0.3			
Figure 10	0.4			
Figure 11	0.5			
Figure 12	0.6			
Figure 13	0.7			
Figure 7	0.2	200	None	13.5
Figure 8	0.25			
Figure 9	0.3			
Figure 10	0.4			
Figure 11	0.5			
Figure 12	0.6			
Figure 13	0.7			
Figure 7	0.2	400	None	13
Figure 8	0.25			
Figure 9	0.3			
Figure 10	0.4			
Figure 11	0.5			
Figure 12	0.6			
Figure 13	0.7			

APPLICATIONS INFORMATION

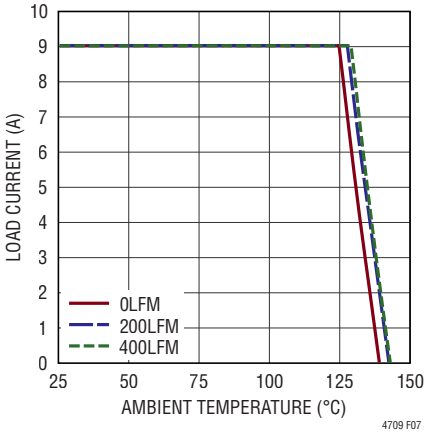


Figure 7. 1.2V to 1V Derating Curve, No Heat Sink

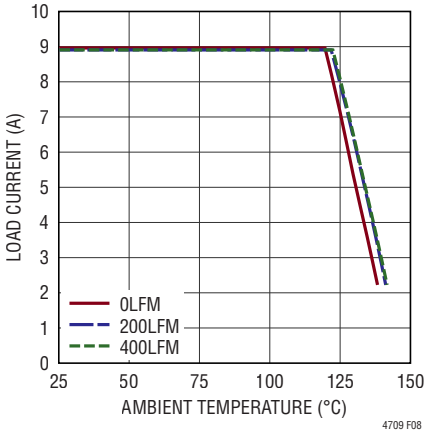


Figure 8. 1.25V to 1V Derating Curve, No Heat Sink

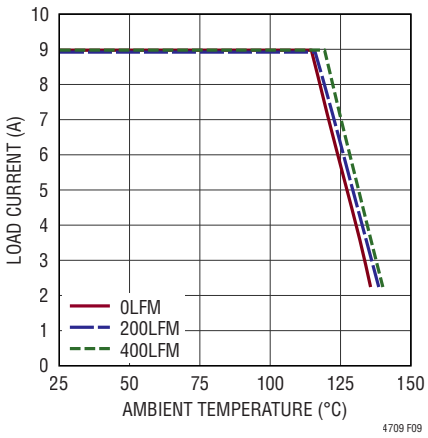


Figure 9. 1.3V to 1V Derating Curve, No Heat Sink

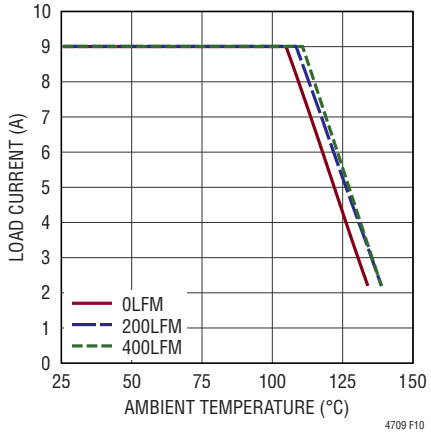


Figure 10. 1.4V to 1V Derating Curve, No Heat Sink

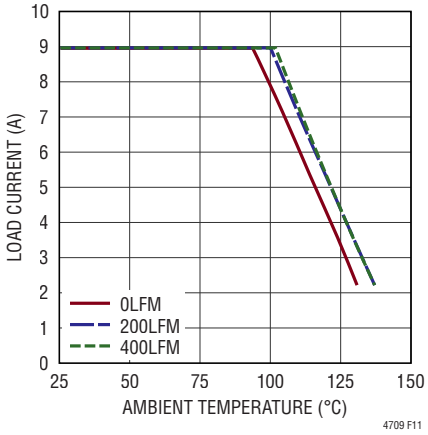


Figure 11. 1.5V to 1V Derating Curve, No Heat Sink

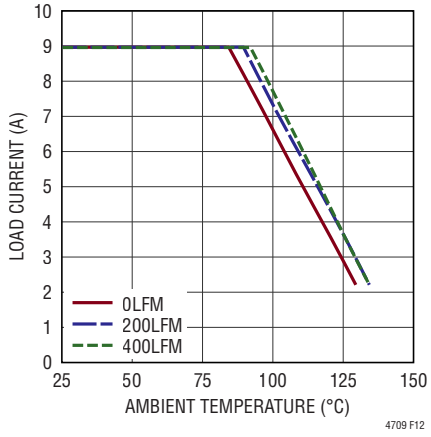


Figure 12. 1.8V to 1.2V Derating Curve, No Heat Sink

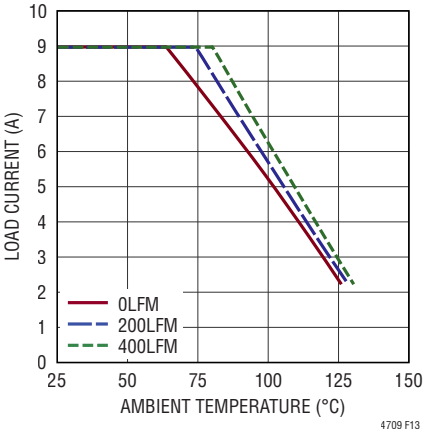


Figure 13. 4.9V to 4.2V Derating Curve, No Heat Sink

APPLICATIONS INFORMATION

Table 3. Output Voltage Response vs Component Matrix

C_{OUT}	VALUE	PART NUMBER
Murata	10µF, 6.3V, 1206, X7R	GRM31CR70J106K
Murata	22µF, 25V, 1206, X5R	GRM31CR61E226KE15L

V_{IN} (V)	V_{OUT} (V)	C_{OUT} CERAMIC (µF)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µs)	P-P DERIVATION (mV)	RECOVERY TIME (µs)
1.3	1	10	0.3 to 3	3	23	5
1.3	1	22	0.3 to 3	3	22	7

Safety Considerations

The LTM4709 µModule ICs do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current must be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and short-circuit protection.

PCB Layout Checklist/Example

The high integration of LTM4709 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high-frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high-frequency noise.
- Place a dedicated power ground layer underneath the unit.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between the top layer and other power layers.
- Do not put via directly on the pad unless they are capped or plated over.
- Flood all unused areas on all layers with copper. Flooding with copper will help release thermal stress. Connect the copper areas to GND.
- Use solder mask defined round pads.

Figure 14 gives a good example of the recommended layout.

For a detailed recommended layout to optimize the low noise and high PSRR performance, refer to the layout of demo board DC3211A.

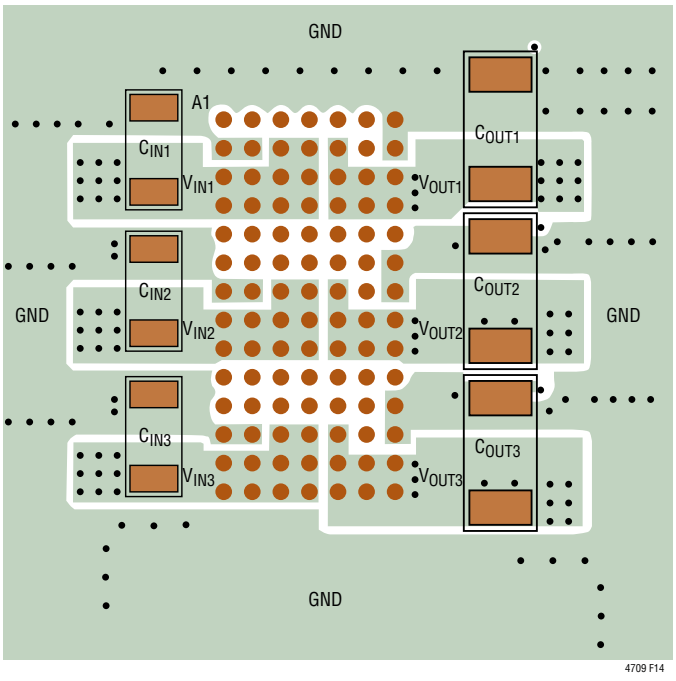


Figure 14. Recommended PCB Layout

TYPICAL APPLICATIONS

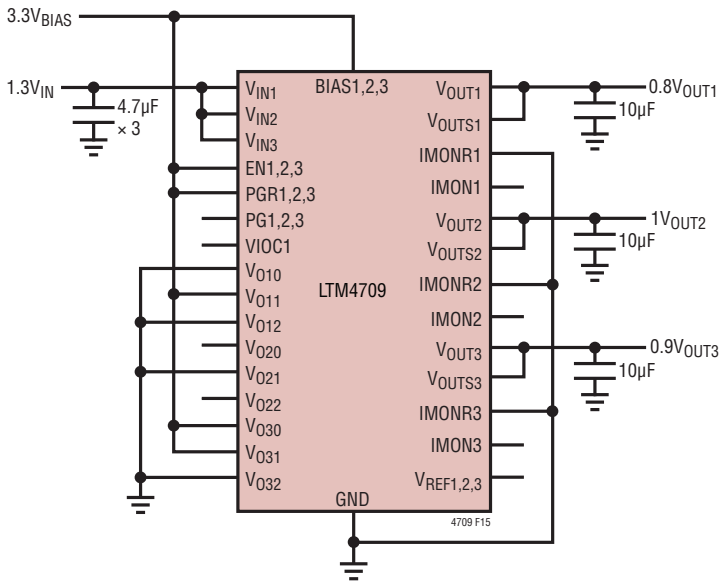


Figure 15. 1.3V Input, 0.8V, 1V, 0.9V Output at Triple 3A with Minimum Solution Size

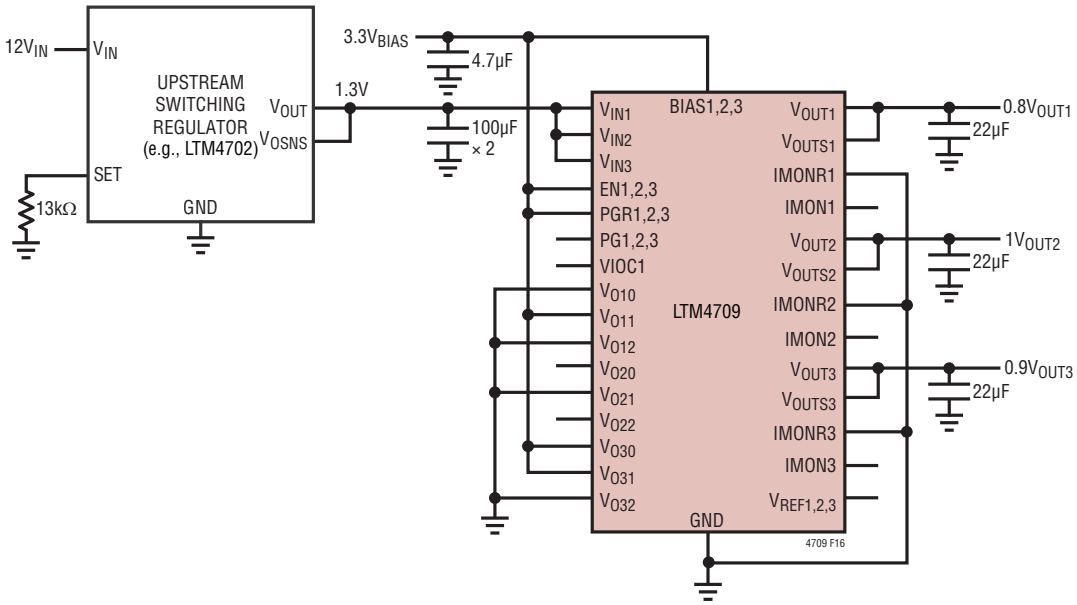


Figure 16. 12V Switching Regulator Input, 0.8V, 1V, 0.9V Output at Triple 2A with Optimized PSRR Performance

TYPICAL APPLICATION

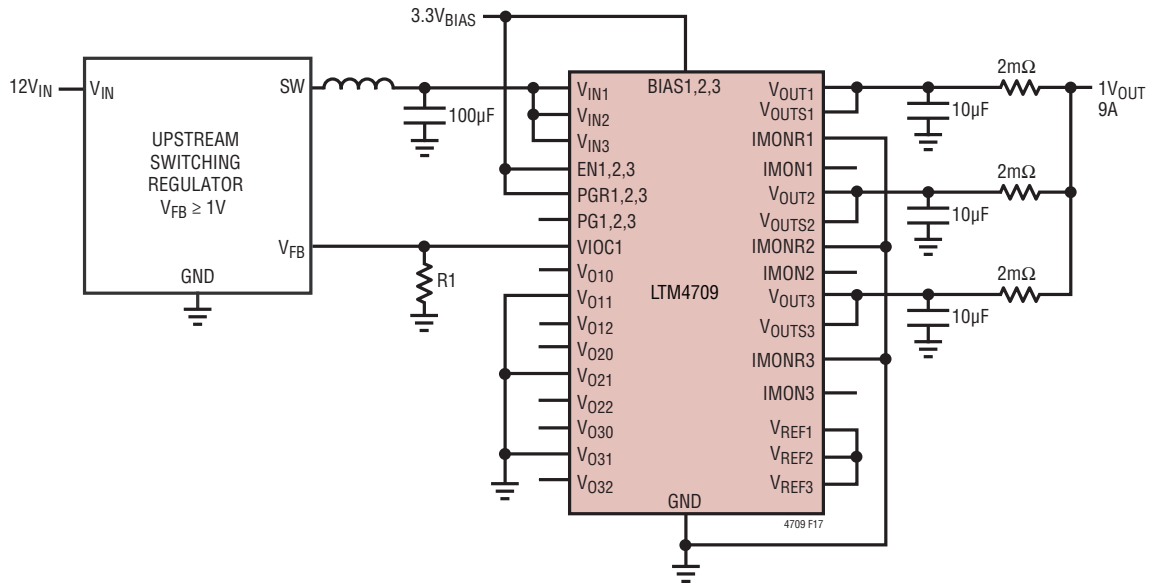


Figure 17. Paralleling Multiple Channels for $1V_{OUT}$, 9A Operation with Upstream Switching Regulator and VIOC for High Efficiency

PACKAGE DESCRIPTION

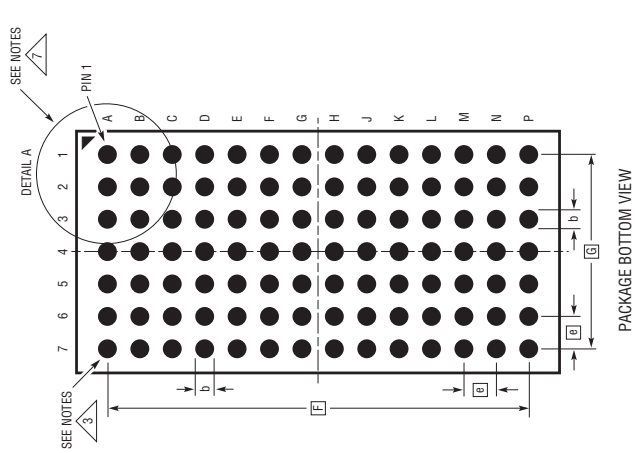
PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Table 4. Package Pinout Description

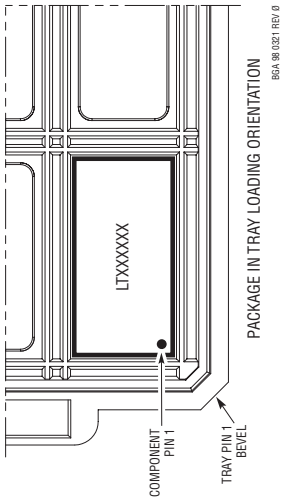
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	NC	A2	IMONR1	A3	PGR1	A4	BIAS1	A5	IMON1	A6	V_{REF1}	A7	GND
B1	GND	B2	GND	B3	V_{IN1}	B4	V_{IN1}	B5	V_{OUT1}	B6	V_{OUTS1}	B7	GND
C1	V_{IN1}	C2	V_{IN1}	C3	V_{IN1}	C4	V_{IN1}	C5	V_{OUT1}	C6	V_{OUT1}	C7	V_{OUT1}
D1	V_{IN1}	D2	V_{IN1}	D3	V_{IN1}	D4	V_{IN1}	D5	V_{OUT1}	D6	V_{OUT1}	D7	V_{OUT1}
E1	VIOC1	E2	PG2	E3	EN1	E4	V_{O10}	E5	V_{O11}	E6	V_{O12}	E7	PG1
F1	EN2	F2	IMONR2	F3	PGR2	F4	BIAS2	F5	IMON2	F6	V_{REF2}	F7	GND
G1	GND	G2	GND	G3	V_{IN2}	G4	V_{IN2}	G5	V_{OUT2}	G6	V_{OUTS2}	G7	GND
H1	V_{IN2}	H2	V_{IN2}	H3	V_{IN2}	H4	V_{IN2}	H5	V_{OUT2}	H6	V_{OUT2}	H7	V_{OUT2}
J1	V_{IN2}	J2	V_{IN2}	J3	V_{IN2}	J4	V_{IN2}	J5	V_{OUT2}	J6	V_{OUT2}	J7	V_{OUT2}
K1	PG3	K2	V_{O30}	K3	V_{O31}	K4	V_{O32}	K5	V_{O20}	K6	V_{O21}	K7	V_{O22}
L1	EN3	L2	IMONR3	L3	PGR3	L4	BIAS3	L5	IMON3	L6	V_{REF3}	L7	GND
M1	GND	M2	GND	M3	V_{IN3}	M4	V_{IN3}	M5	V_{OUT3}	M6	V_{OUTS3}	M7	GND
N1	V_{IN3}	N2	V_{IN3}	N3	V_{IN3}	N4	V_{IN3}	N5	V_{OUT3}	N6	V_{OUT3}	N7	V_{OUT3}
P1	V_{IN3}	P2	V_{IN3}	P3	V_{IN3}	P4	V_{IN3}	P5	V_{OUT3}	P6	V_{OUT3}	P7	V_{OUT3}

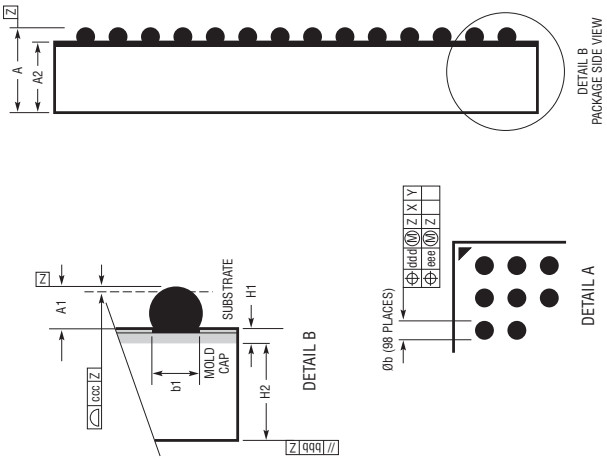
PACKAGE DESCRIPTION

BGA Package
98-Lead (6mm × 12mm × 1.92mm)
(Reference LTC DWG # 05-08-7090 Rev Ø)

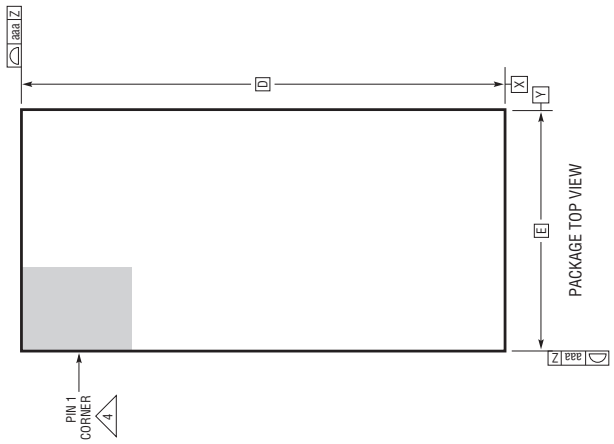


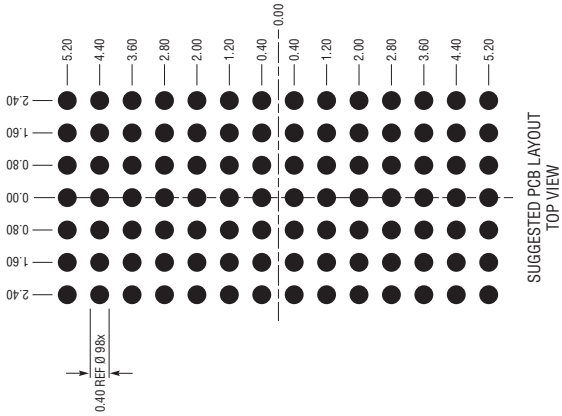
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS. DRAWING NOT TO SCALE
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY





DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.73	1.92	2.11	
A1	0.30	0.40	0.50	BALL HT
A2	1.43	1.52	1.61	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		12.00		
E		6.00		
e		0.80		
F		10.40		
G		4.80		
H1		0.32 REF		SUBSTRATE THK
H2		1.20 REF		MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 98				



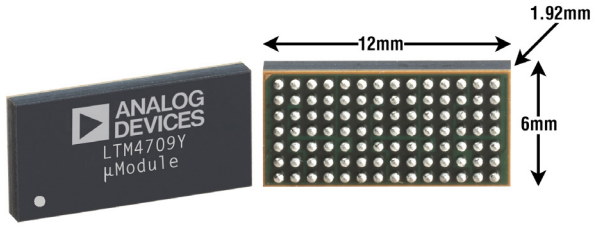


REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
0	07/23	Initial Release	—

PACKAGE PHOTOS

Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search INPUT | V_{in}(Min) V V_{in}(Max) V OUTPUT | V_{Out} V I_{out} A FEATURES | Low EMI Ultrathin Internal Heat Sink Multiple Outputs Search	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8080	$40V_{IN}$, Dual 500mA or Single 1A Ultralow Noise, Ultrahigh PSRR µModule Regulator	$3.5V \le V_{IN} \le 40V$, $0V \le V_{OUT} \le 8V$, 9mm × 6.25mm × 3.32mm, BGA Package
LTM4702	$16V_{IN}$, 8A Silent Switcher µModule Regulator with Low EMI Emission and RMS Noise	$3V \le V_{IN} \le 16V$, $0.3V \le V_{OUT} \le 5.7V$, 6.25mm × 6.25mm × 5.07mm, BGA Package
LTM8074	$40V_{IN}$, 1.2A Silent Switcher µModule Regulator	$3.2V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 12V$, 4mm × 4mm × 1.82mm, BGA Package
LTM8063	$40V_{IN}$, 2A Silent Switcher µModule Regulator	$3.2V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 15V$, 4mm × 6.25mm × 2.22mm, BGA Package
LTM8065	$40V_{IN}$, 2.5A Silent Switcher µModule Regulator	$3.4V \le V_{IN} \le 40V$, $0.97V \le V_{OUT} \le 18V$, 6.25mm × 6.25mm × 2.32mm, BGA Package
LTM8053	$40V_{IN}$, 3.5A Silent Switcher µModule Regulator	$3.4V \le V_{IN} \le 40V$, $0.97V \le V_{OUT} \le 15V$, 6.25mm × 9mm × 3.32mm, BGA Package
LTM8078	Dual 1.4A, $40V_{IN}$, Silent Switcher µModule Regulator	$3V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 10V$, 6.25mm × 6.25mm × 2.22mm, BGA Package
LTM8024	Dual 3.5A, $40V_{IN}$, Silent Switcher µModule Regulator	$3V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 8V$, 9mm × 11.25mm × 3.32mm, BGA Package
LTM8051	Quad 1.2A, $40V_{IN}$, Silent Switcher µModule Regulator	$3V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 8V$, 6.25mm × 11.25mm × 2.22mm, BGA Package
LTM8060	Quad 3A, $40V_{IN}$, Silent Switcher µModule Regulator	$\le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 8V$, 11.9mm × 16mm × 3.32mm, BGA Package