

P-Channel 200V (D-S) MOSFET

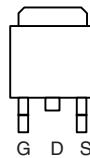
PRODUCT SUMMARY		
V _{DS} (V)	-200	
R _{DS(on)} (Ω)	V _{GS} = -10 V	2.0
Q _g max. (nC)	44	
Q _{gs} (nC)	7.1	
Q _{gd} (nC)	27	
Configuration	Single	

FEATURES

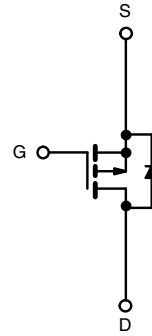
- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- Fast switching
- Ease of paralleling
- Simple drive requirements



TO-263



Top View



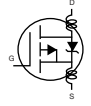

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL		LIMIT	UNIT	
Drain-Source Voltage	V _{DS}		-200	V	
Gate-Source Voltage	V _{GS}		± 20	V	
Continuous Drain Current	V _{GS} at -10 V	T _C = 25 °C	-4	A	
		T _C = 100 °C	-2		
Pulsed Drain Current ^a	I _{DM}		-8		
Linear Derating Factor			1.0	W/°C	
Single Pulse Avalanche Energy ^b	E _{AS}		400	mJ	
Repetitive Avalanche Current ^a	I _{AR}		-3	A	
Repetitive Avalanche Energy ^a	E _{AR}		10	mJ	
Maximum Power Dissipation	T _C = 25 °C		P _D	105	W
Peak Diode Recovery dV/dt ^c	dV/dt		-5.0	V/ns	
Operating Junction and Storage Temperature Range	T _J , T _{stg}		-55 to +150	°C	
Soldering Recommendations (Peak temperature) ^d	for 10 s		300		
Mounting Torque	6-32 or M3 screw		10	lbf · in	
			1.1	N · m	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = -50 V, starting T_J = 25 °C, L = 8.7 mH, R_g = 25 Ω, I_{AS} = -11 A (see fig. 12).
- I_{SD} ≤ -11 A, di/dt ≤ 150 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = -1\text{ mA}$	-	-0.2	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1.5	-	-4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 10	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$	-	-	-100	μA
		$V_{DS} = -160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -2.0\text{ A}^b$	-	2.0	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = -50\text{ V}, I_D = -2.0\text{ A}^b$	4.1	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5	-	700	-	pF
Output Capacitance	C_{oss}		-	370	-	
Reverse Transfer Capacitance	C_{rss}		-	81	-	
Total Gate Charge	Q_g	$V_{GS} = -10\text{ V}, I_D = -2\text{ A}, V_{DS} = -160\text{ V}$, see fig. 6 and 13 ^b	-	-	44	nC
Gate-Source Charge	Q_{gs}		-	-	7.1	
Gate-Drain Charge	Q_{gd}		-	-	27	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -100\text{ V}, I_D = -2\text{ A}, R_g = 9.1\text{ }\Omega, R_D = 8.6\text{ }\Omega$, see fig. 10 ^b	-	14	-	ns
Rise Time	t_r		-	43	-	
Turn-Off Delay Time	$t_{d(off)}$		-	39	-	
Fall Time	t_f		-	38	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Gate Input Resistance	R_g	$f = 1\text{ MHz}$, open drain	0.3	-	1.7	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p-n junction diode 	-	-	-2	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	-4	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = -2\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	-5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = -11\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	250	300	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	2.9	3.6	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

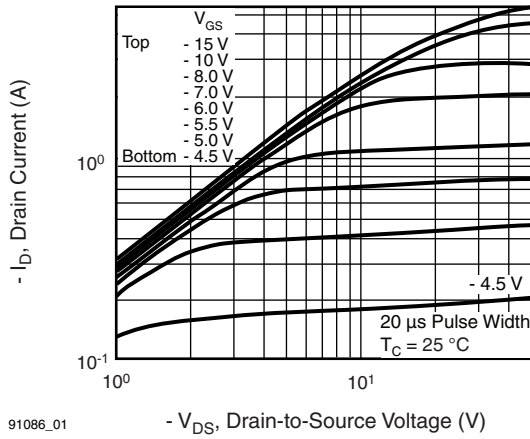


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

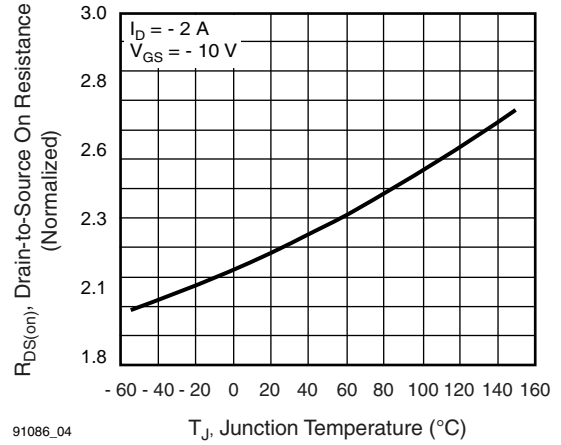


Fig. 4 - Normalized On-Resistance vs. Temperature

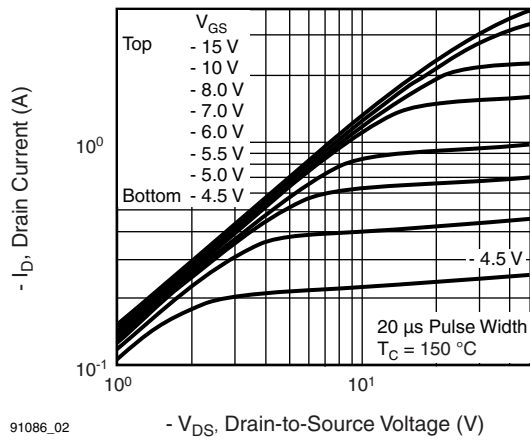


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

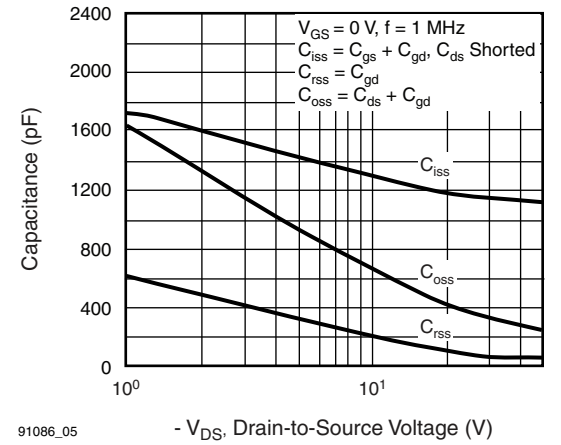


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

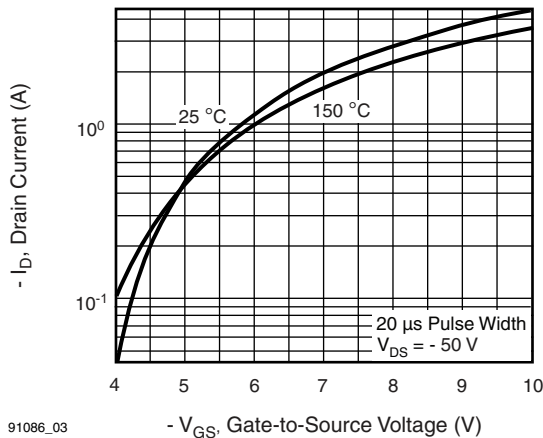


Fig. 3 - Typical Transfer Characteristics

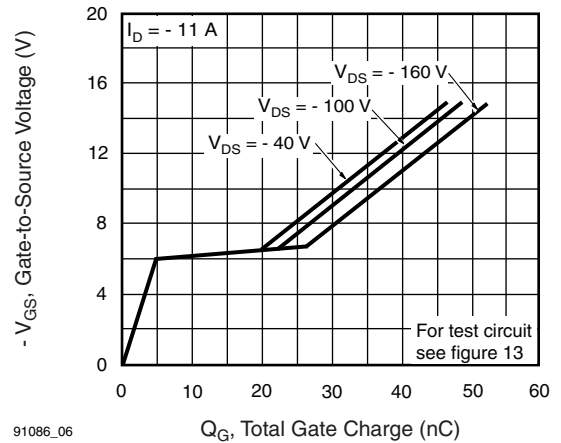
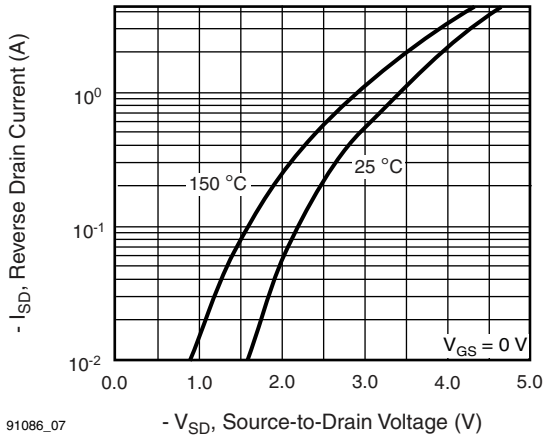
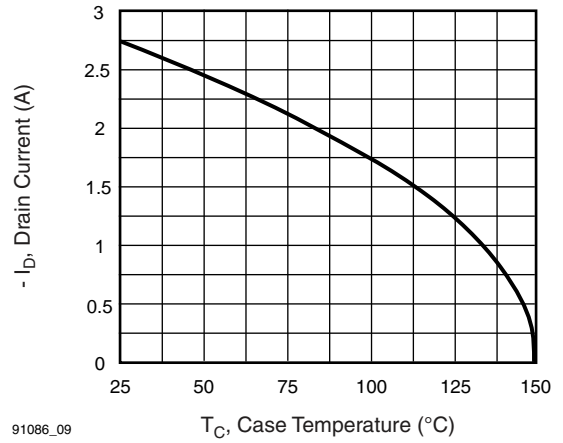


Fig. 6 - Typical Gate Charge vs. Drain-to-Source Voltage



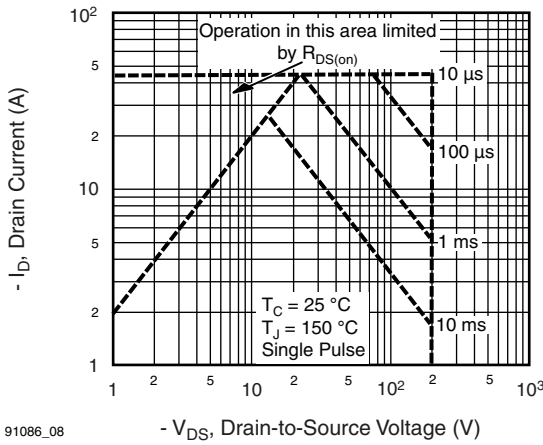
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 9 - Maximum Drain Current vs. Case Temperature



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Fig. 8 - Maximum Safe Operating Area

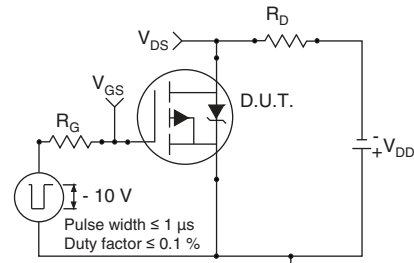


Fig. 10a - Switching Time Test Circuit

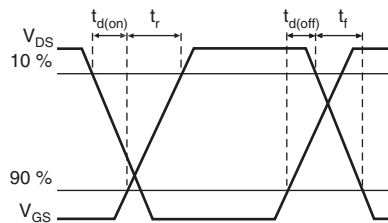
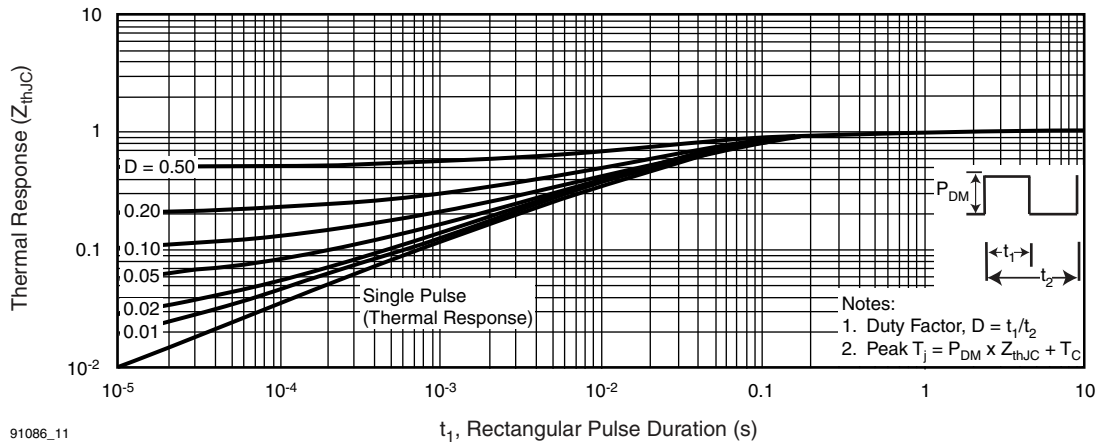


Fig. 10b - Switching Time Waveforms



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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

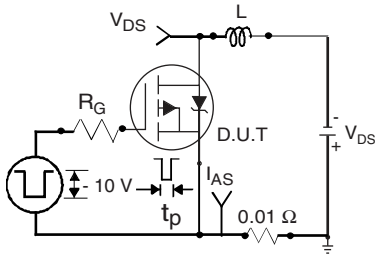


Fig. 12a - Unclamped Inductive Test Circuit

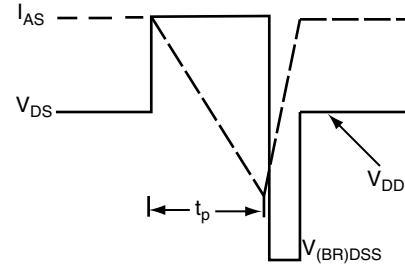


Fig. 12b - Unclamped Inductive Waveforms

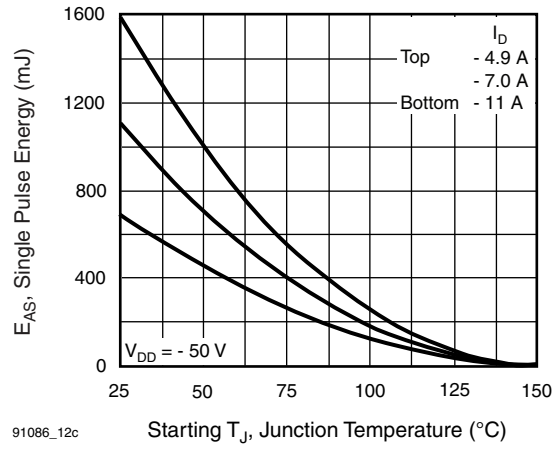


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

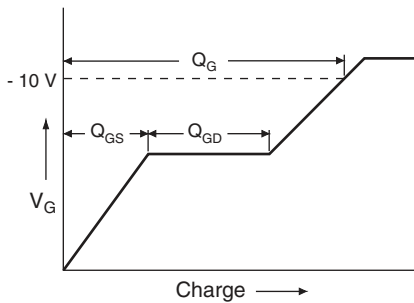


Fig. 13a - Basic Gate Charge Waveform

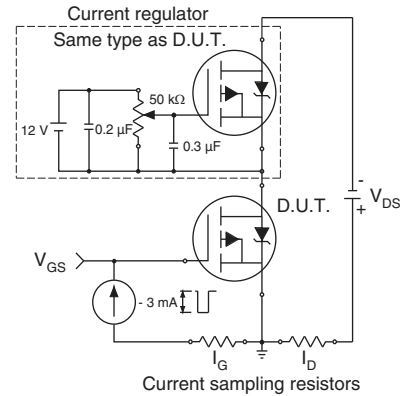
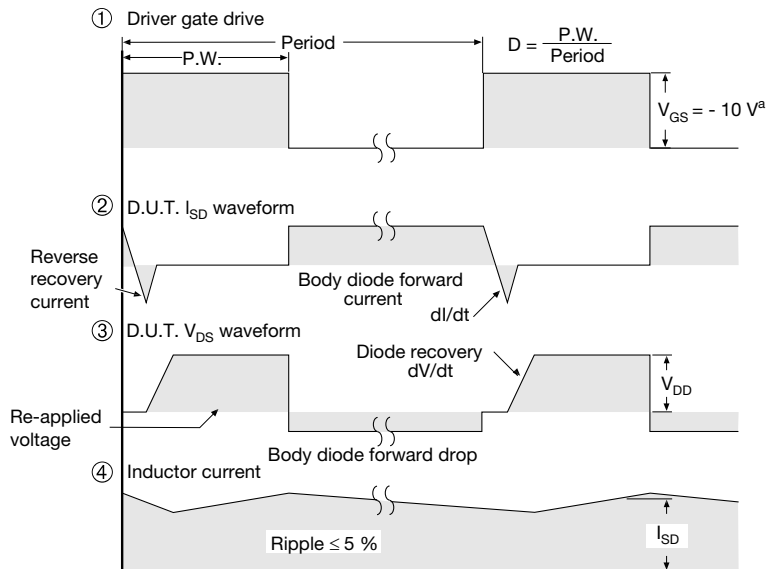
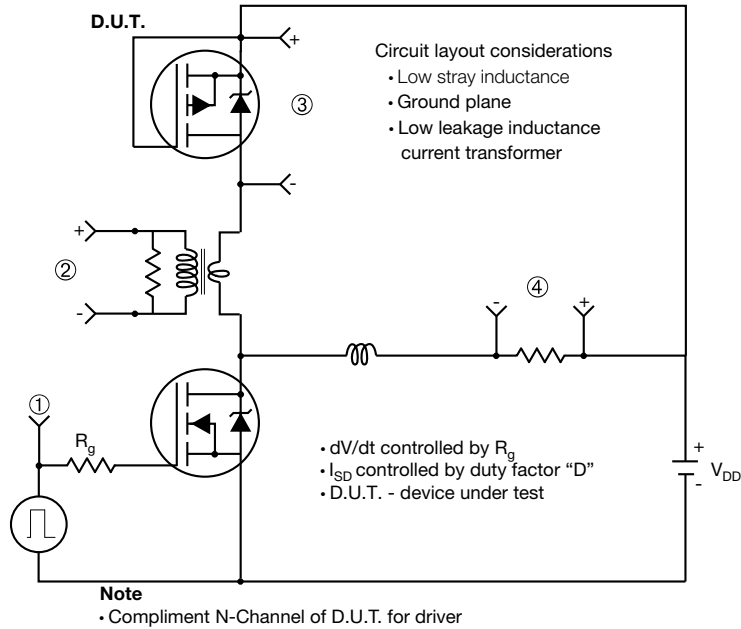


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

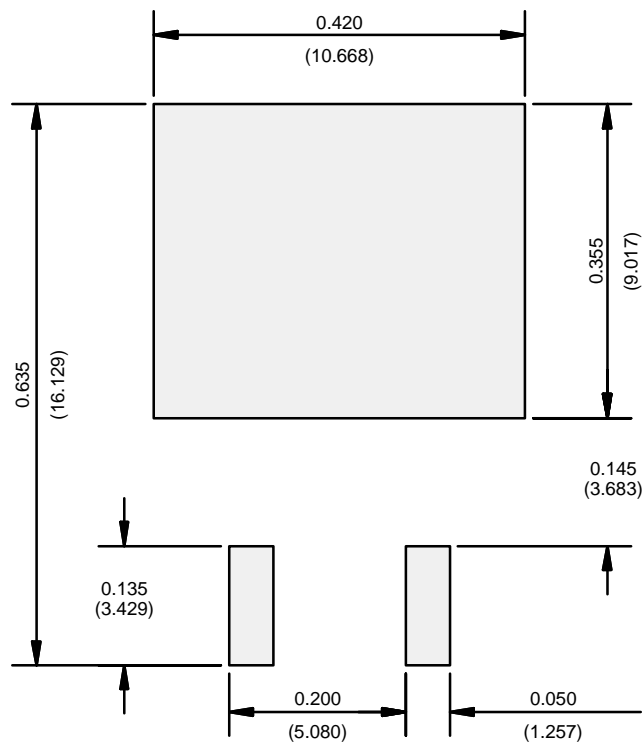


Note

a. $V_{GS} = -5 V$ for logic level and $-3 V$ drive devices

Fig. 14 - For P-Channel

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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