



CD4051 (LX) 8-channel Analog Multiplexer/Demultiplexer

Product Specification

Specification Revision History:

Version	Date	Description
2019-06-A1	2019-06	New
2021-12-A2	2021-12	Modify Ordering Information
2023-04-B1	2023-04	Update the template



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1、General Description

The CD4051 is an 8-channel analog multiplexer/demultiplexer with three address inputs (S1 to S3), an active LOW enable input ($\bar{E}$), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). The device contains eight bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y7) and the other side connected to a common input/output (Z). With $\bar{E}$ LOW, one of the eight switches is selected (low-impedance ON-state) by S1 to S3. With $\bar{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S1 to S3. If break before make is needed, then it is necessary to use the enable input.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S1 to S3, and $\bar{E}$). The V_{DD} to V_{SS} range is 3V to 9V. The analog inputs/outputs (Y0 to Y7, and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 9V. Unused inputs must be connected to V_{DD} , V_{SS} , or another input. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground). V_{EE} and V_{SS} are the supply voltage connections for the switches.

Features:

- Wide supply voltage range from 3V to 9V
- Fully static operation
- 5V and 9V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C
- Packaging information: DIP16/SOP16/TSSOP16



Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CD4051BE (LX)	DIP16	CD4051BE	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
CD4051BM (LX)	SOP16	CD4051BM	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
CD4051BPW (LX)	TSSOP16	CD4051B	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CD4051BM (LX)	SOP16	CD4051BM	2500 PCS/reel	5000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
CD4051BPW (LX)	TSSOP16	CD4051B	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



2、Block Diagram And Pin Description

2.1、Block Diagram

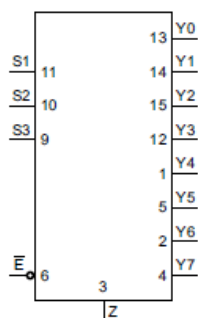


Figure 1. Logic symbol

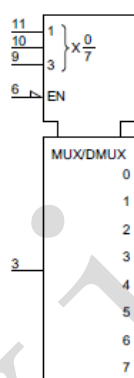


Figure 2. IEC logic symbol

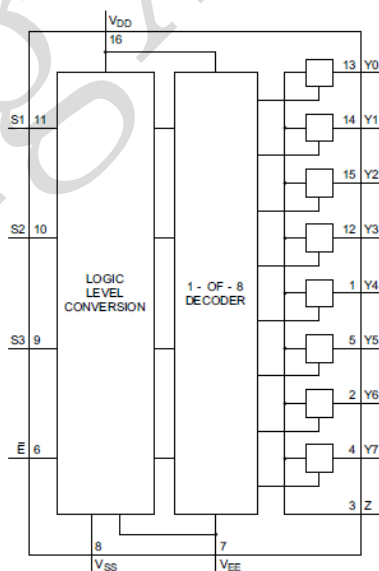


Figure 3. Functional diagram

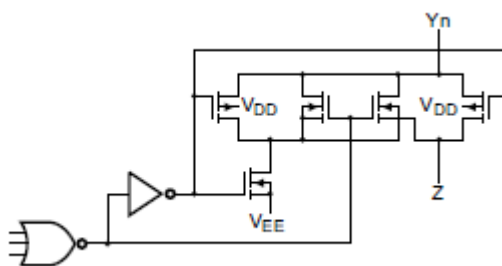


Figure 4. Schematic diagram (one switch)

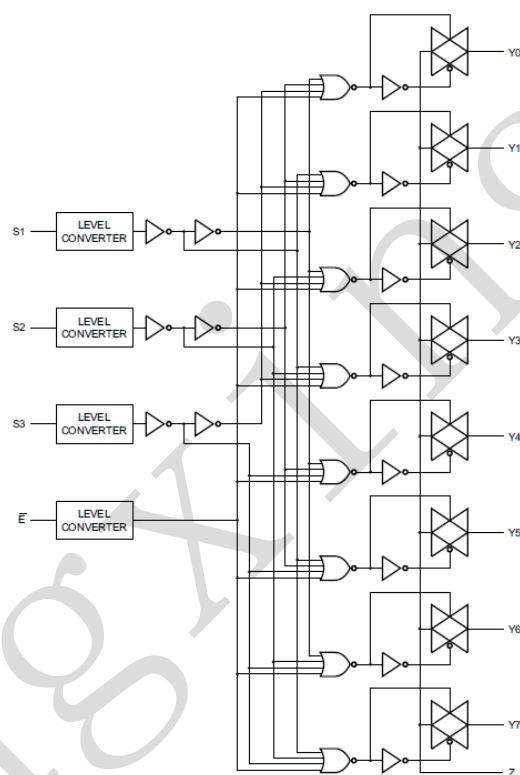
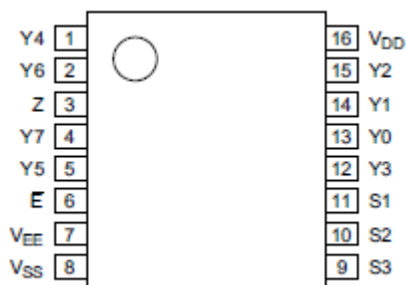


Figure 5. Logic diagram

2.2. Pin Configurations





2.3、Pin Description

Pin No.	Pin Name	Description
1	Y4	independent input or output
2	Y6	independent input or output
3	Z	common output or input
4	Y7	independent input or output
5	Y5	independent input or output
6	$\bar{E}$	enable input (active LOW)
7	V _{EE}	supply voltage
8	V _{SS}	ground (0V)
9	S3	select input
10	S2	select input
11	S1	select input
12	Y3	independent input or output
13	Y0	independent input or output
14	Y1	independent input or output
15	Y2	independent input or output
16	V _{DD}	supply voltage

2.4、Function Table

Input				Channel ON
$\bar{E}$	S3	S2	S1	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	switches off

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.



3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{DD}	-	-0.5	+12	V
Power Supply Voltage	V_{EE}	-	-12	+0.5	V
input clamping current	I_{IK}	$V_I < 0.5V$ or $V_I > V_{DD} + 0.5V$	-	± 10	mA
switch current	I	-	-	± 10	mA
input voltage	V_I	all inputs	-0.5	$V_{DD} + 0.5$	V
storage temperature	T_{stg}	-	-65	+150	°C
total power dissipation	P_{tot}	-	-	500	mW
device dissipation	P	per output transistor	-	100	mW
Soldering temperature	T_L	10s	DIP	245	°C
			SOP/TSSOP	260	°C

3.2、Recommended Operating Conditions

($T_{amb} = 25^\circ\text{C}$; $R_L = 10k\Omega$; $C_L = 50pF$; $\bar{E} = V_{DD}$; $V_{is} = V_{DD} = 5V$.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	5	9	V
ambient temperature	T_{amb}	in free air	-40	-	+125	°C
supply voltage	V_{EE}	-	-6.0	-	0	V
supply voltage	$V_{DD} - V_{EE}$	-	3.0	-	9.0	V
input voltage	V_I	-	0	-	V_{DD}	V
Disable output time (High level→turn off)	t_{PHZ}	$\bar{E}$ to Z or $\bar{E}$ to Y_n	-	85	170	ns
Disable output time (Low level→turn off)	t_{PLZ}	$\bar{E}$ to Z or $\bar{E}$ to Y_n	-	115	230	ns
Enable output time (turn off→high/low level)	t_{PZH}, t_{PZL}	-	-	40	80	ns
input capacitance	C_I	-	-	-	7.5	pF



3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)		$T_{amb}=25^{\circ}\text{C}$			Unit
				Min.	Typ.	Max.	
supply current	I_{DD}	$V_I=V_{DD}$ or V_{SS} , $I_O=0\text{A}$	$V_{DD}=5\text{V}$	-	-	20	μA
			$V_{DD}=9\text{V}$	-	-	40	μA
HIGH-level input voltage	V_{IH}	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$	3.5	-	-	V
			$V_{DD}=9\text{V}$	7.0	-	-	V
LOW-level input voltage	V_{IL}	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$	-	-	1.5	V
			$V_{DD}=9\text{V}$	-	-	3.0	V
input leakage current	I_I	$V_I=0\text{V}$ or 9V , $V_{DD}=9\text{V}$		-	-	1.0	μA
3 state output leakage current	I_{OZ}	$V_{DD}=9\text{V}$	output to V_{DD}	-	-	1.6	μA
			output to V_{SS}	-	-	-1.6	μA
ON resistance (rail)	R_{ON}	$V_{IS}=0\text{V}$ to $V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5\text{V}$	-	350	2500	Ω
			$V_{DD}-V_{EE}=9\text{V}$	-	80	245	Ω
		$V_{IS}=0\text{V}$	$V_{DD}-V_{EE}=5\text{V}$	-	115	340	Ω
			$V_{DD}-V_{EE}=9\text{V}$	-	50	160	Ω
		$V_{IS}=V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5\text{V}$	-	120	365	Ω
			$V_{DD}-V_{EE}=9\text{V}$	-	65	200	Ω
ON resistance mismatch between channels	ΔR_{ON}	$V_{IS}=0\text{V}$ to $V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5\text{V}$	-	25	-	Ω
			$V_{DD}-V_{EE}=9\text{V}$	-	10	-	Ω
OFF-state leakage current	$I_{S(OFF)}$	$V_{SS}=V_{EE}$, $V_{DD}-V_{EE}=9\text{V}$	all channel off; $\bar{E}=V_{DD}$	-	-	1.0	μA
			any channel; $\bar{E}=V_{SS}$	-	-	1.0	μA

3.3.2、DC Characteristics 2

($T_{amb}=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)		$T_{amb}=-40^{\circ}\text{C}$		$T_{amb}=+85^{\circ}\text{C}$		Unit
				Min.	Max.	Min.	Max.	
supply current	I_{DD}	$V_I=V_{DD}$ or V_{SS} , $I_O=0\text{A}$	$V_{DD}=5\text{V}$	-	20	-	150	μA
			$V_{DD}=9\text{V}$	-	40	-	300	μA
HIGH-level input voltage	V_{IH}	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$	3.5	-	3.5	-	V
			$V_{DD}=9\text{V}$	7.0	-	7.0	-	V
LOW-level input voltage	V_{IL}	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$	-	1.5	-	1.5	V
			$V_{DD}=9\text{V}$	-	3.0	-	3.0	V
input leakage current	I_I	$V_I=0\text{V}$ or 9V , $V_{DD}=9\text{V}$		-	1.0	-	1.0	μA
3 state output leakage current	I_{OZ}	$V_{DD}=9\text{V}$	output to V_{DD}	-	1.6	-	12.0	μA
			output to V_{SS}	-	-1.6	-	-12.0	μA



3.3.3、DC Characteristics 3

($T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)	$T_{amb} = -40^{\circ}\text{C}$		$T_{amb} = +125^{\circ}\text{C}$		Unit
			Min.	Max.	Min.	Max.	
supply current	I_{DD}	$V_I = V_{DD}$ or V_{SS} , $I_O = 0\text{A}$	$V_{DD} = 5\text{V}$	-	20	-	150 μA
			$V_{DD} = 9\text{V}$	-	40	-	300 μA
HIGH-level input voltage	V_{IH}	$ I_O < 1\mu\text{A}$	$V_{DD} = 5\text{V}$	3.5	-	3.5	V
			$V_{DD} = 9\text{V}$	7.0	-	7.0	V
LOW-level input voltage	V_{IL}	$ I_O < 1\mu\text{A}$	$V_{DD} = 5\text{V}$	-	1.5	-	1.5 V
			$V_{DD} = 9\text{V}$	-	3.0	-	3.0 V
input leakage current	I_I	$V_I = 0\text{V}$ or 9V , $V_{DD} = 9\text{V}$	-	1.0	-	1.0	μA
3 state output leakage current	I_{OZ}	$V_{DD} = 9\text{V}$	output to V_{DD}	-	1.6	-	12.0 μA
			output to V_{SS}	-	-1.6	-	-12.0 μA

3.3.4、AC Characteristics 1

($T_{amb} = 25^{\circ}\text{C}$, $V_{EE} = V_{SS} = 0\text{V}$, $t_r, t_f \leq 20\text{ns}$, $C_L = 50\text{pF}$, $R_L = 10\text{k}\Omega$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay time	t_{PHL}	Yn to Z; Z to Yn; see Figure 7	$V_{DD} = 5\text{V}$	-	15	30 ns
			$V_{DD} = 9\text{V}$	-	5	10 ns
		Sn to Yn, Z; see Figure 8	$V_{DD} = 5\text{V}$	-	150	300 ns
			$V_{DD} = 9\text{V}$	-	60	120 ns
LOW to HIGH propagation delay	t_{PLH}	Yn to Z; Z to Yn; see Figure 7	$V_{DD} = 5\text{V}$	-	15	30 ns
			$V_{DD} = 9\text{V}$	-	5	10 ns
		Sn to Yn, Z; see Figure 8	$V_{DD} = 5\text{V}$	-	150	300 ns
			$V_{DD} = 9\text{V}$	-	65	130 ns
HIGH to OFF-state propagation delay	t_{PHZ}	$\bar{E}$ to Yn, Z; see Figure 9	$V_{DD} = 5\text{V}$	-	120	240 ns
			$V_{DD} = 9\text{V}$	-	90	180 ns
LOW to OFF-state propagation delay	t_{PLZ}	$\bar{E}$ to Yn, Z; see Figure 9	$V_{DD} = 5\text{V}$	-	145	290 ns
			$V_{DD} = 9\text{V}$	-	120	240 ns
OFF-state to HIGH propagation delay	t_{PZH}	$\bar{E}$ to Yn, Z; see Figure 9	$V_{DD} = 5\text{V}$	-	140	280 ns
			$V_{DD} = 9\text{V}$	-	55	110 ns
OFF-state to LOW propagation delay	t_{PZL}	$\bar{E}$ to Yn, Z; see Figure 9	$V_{DD} = 5\text{V}$	-	140	280 ns
			$V_{DD} = 9\text{V}$	-	55	110 ns



3.3.5、AC Characteristics 2

($T_{amb}=25^{\circ}\text{C}$, $V_{EE}=V_{SS}=0\text{V}$, $V_I=0.5V_{DD}$ (p-p), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Square wave distortion	d _{sin}	see Figure 10; R _L =10kΩ; C _L =15pF; channel ON; f _i =1kHz	V _{DD} =5V	0.25	-	-	%
			V _{DD} =9V	0.04	-	-	%
any two channel crosstalk	f _{ct}	V _{DD} =9V, see note2		1	-	-	MHz
crosstalk voltage ($\bar{E}$ to Sn or Yn to Z)	V _{ct}	see Figure 11; R _L =10kΩ; C _L =15pF; $\bar{E}$ or Sn=V _{DD} (square-wave)		50	-	-	mV
OFF frequency	f _{OFF}	V _{DD} =9V, see note3		1	-	-	MHz
conduction frequency	f _{ON}	V _{DD} =5V, see note4		13	-	-	MHz
		V _{DD} =9V, see note4		40	-	-	MHz

Note:

[1] f_i is biased at $0.5V_{DD}$; $V_I=0.5V_{DD}$ (p-p).

[2] $R_L=1\text{k}\Omega$; $20\log V_{os}/V_{is}=-50\text{dB}$, see Figure 12.

[3] $R_L=1\text{k}\Omega$; $C_L=5\text{pF}$, channel off, $20\log V_{os}/V_{is}=-50\text{dB}$, see Figure 10.

[4] $R_L=1\text{k}\Omega$; $C_L=5\text{pF}$, channel on, $20\log V_{os}/V_{is}=-3\text{dB}$, see Figure 10.

4、Testing Circuit

4.1、AC Testing Circuit 1

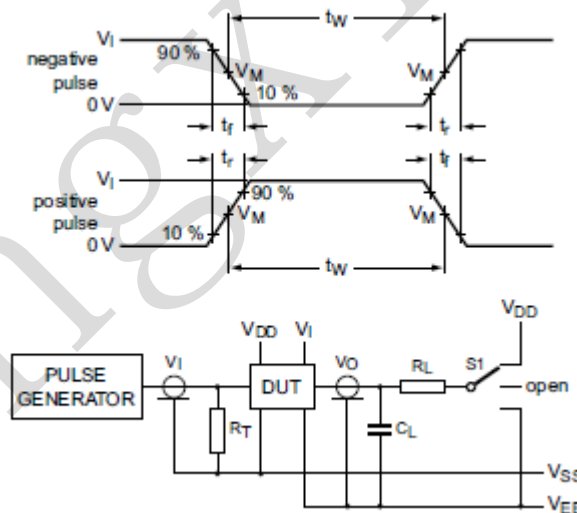


Figure 6. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L =Load resistance.

4.2、AC Testing Waveforms

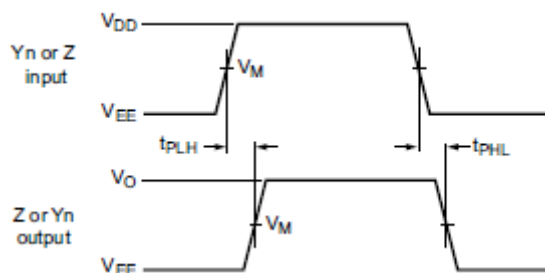


Figure 7. Yn, Z to Z, Yn propagation delays

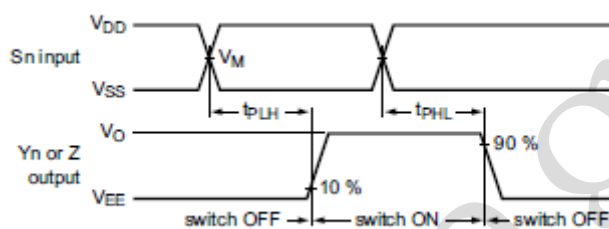


Figure 8. Sn to Yn, Z propagation delays

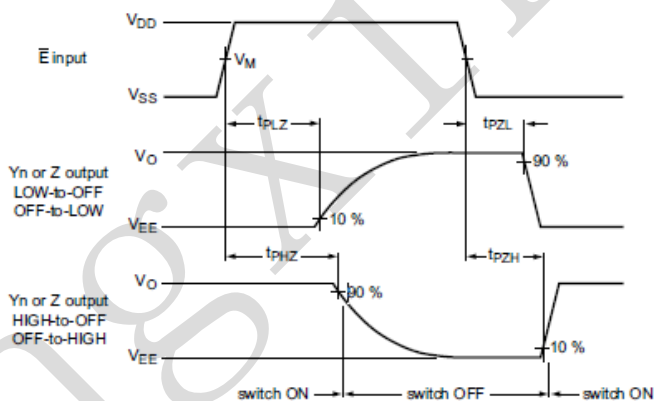


Figure 9. Enable and disable times

4.3、AC Testing Circuit 2

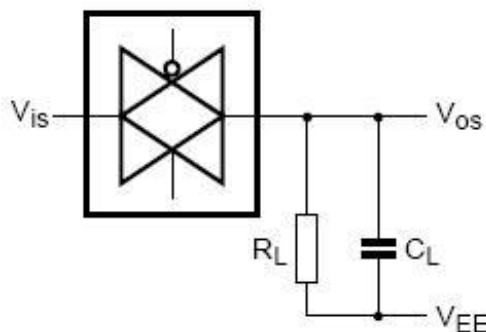


Figure 10. Square wave distortion degree of cut-off frequency and conduction frequency test pattern

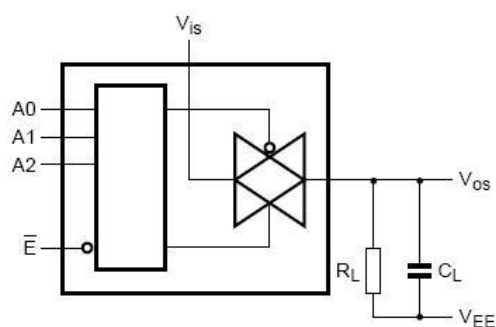


Figure 11. Crosstalk logical input/output test

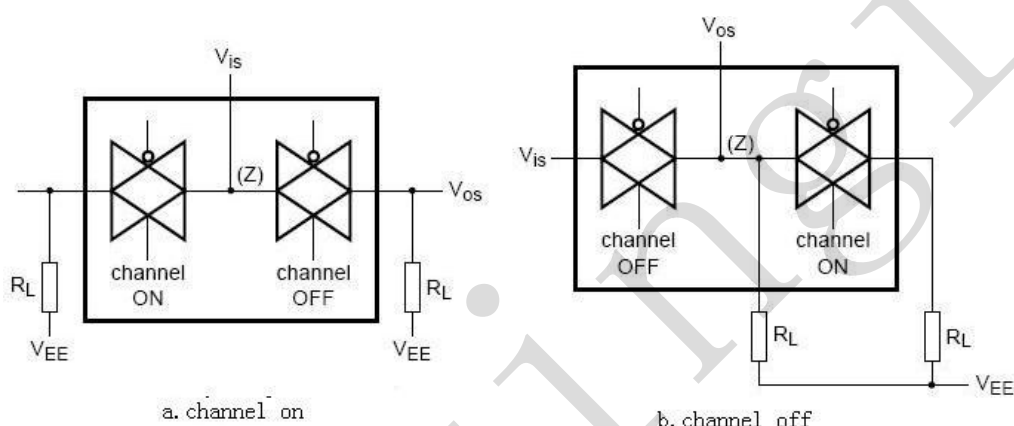


Figure 12. Inter channel Crosstalk

4.4、Measurement Points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
3V to 9V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

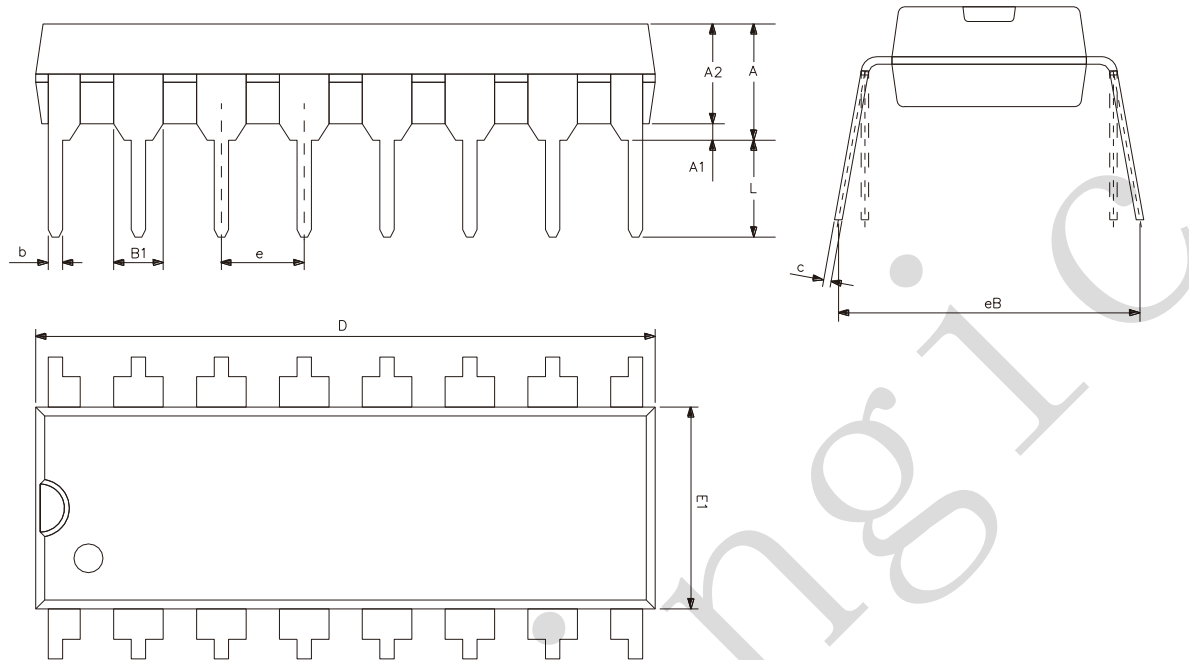
4.5、Test Data

Test	Input		Load		Switch
	V_{is}	t_r, t_f	C_L	R_L	
t_{PHL}	V_{EE}	20ns	50pF	10k Ω	V_{DD}
t_{PLH}	V_{DD}	20ns	50pF	10k Ω	V_{EE}
t_{pZH}, t_{pHZ}	V_{DD}	20ns	50pF	10k Ω	V_{EE}
t_{pZL}, t_{pLZ}	V_{EE}	20ns	50pF	10k Ω	V_{DD}
others	pulse	20ns	50pF	10k Ω	open



5、Package Information

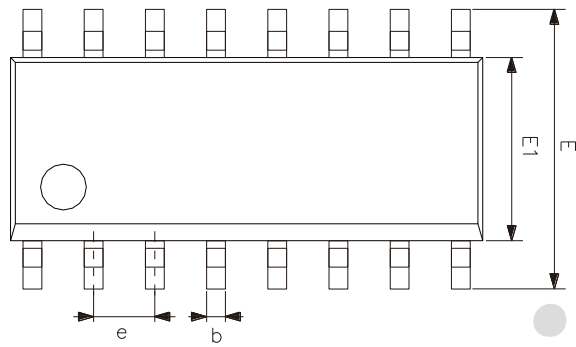
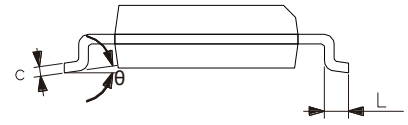
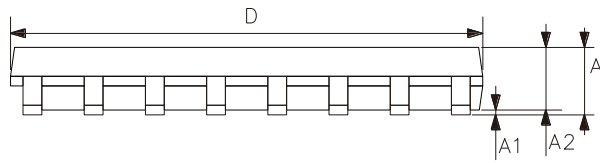
5.1、DIP16



Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30



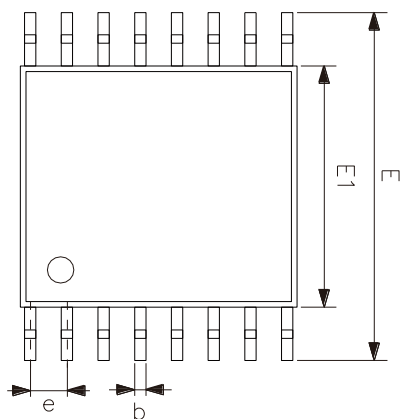
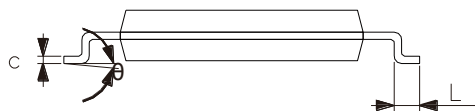
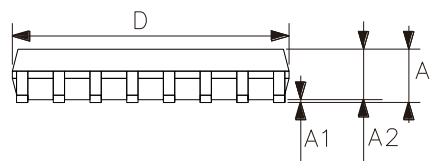
5.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°



5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°



6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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