

General Description

The AGM30P20AS combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

This device is ideal for load switch and battery protection applications.

Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance
- 100% Avalanche tested
- 100% DVDS tested

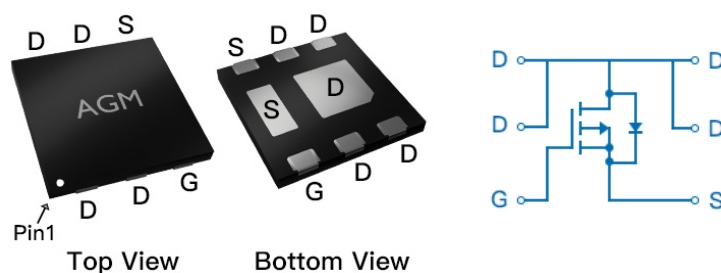
Application

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

Product Summary

BVDSS	RDSON	ID
-30V	13mΩ	-20A

DFN2*2 Pin Configuration



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM30P20	AGM30P20AS	DFN2*2	178mm	8mm	3000

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
VDS	Drain-Source Voltage (VGS=0V)	-30	V
VGS	Gate-Source Voltage (VDS=0V)	±20	V
ID	Drain Current-Continuous(Ta=25°C) (Note 1)	-20	A
	Drain Current-Continuous(Ta=100°C)	-14	A
IDM (pluse)	Drain Current-Continuous@ Current-Pulsed (Note 2)	-80	A
PD	Maximum Power Dissipation(Ta=25°C)	9.0	w
	Maximum Power Dissipation(Ta=100°C)	3.6	w
EAS	Avalanche energy (Note 3)	45	mJ
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	°C

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
RθJA	Thermal Resistance Junction-ambient (Steady State) ¹	---	68	°C/W
RθJC	Thermal Resistance Junction-Case ¹	---	13.9	°C/W

Table 3. Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V ID=250μA	-30	--	--	V
IDSS	Zero Gate Voltage Drain Current	VDS=-30V,VGS=0V	--	--	-1.0	μA
IGSS	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS,ID=-250μA	-1.2	-1.6	-2.1	V
gFS	Forward Transconductance	VDS=-5V,ID=-5A	--	5	--	S
RDS(on)	Drain-Source On-State Resistance	VGS=-10V, ID=-10A	--	13	16	mΩ
		VGS=-4.5V, ID=-5A	--	18	27	mΩ
Dynamic Characteristics						
Ciss	Input Capacitance	VDS=-15V,VGS=0V F=1MHZ	--	1330	--	pF
Coss	Output Capacitance		--	183	--	pF
Crss	Reverse Transfer Capacitance		--	156	--	pF
Rg	Gate resistance	VGS=0V, VDS=0V,f=1.0MHz	--	--	--	Ω
Switching Times						
td(on)	Turn-on Delay Time	VGS=-10V, VDS=-15V, ID=-10A	--	9	--	nS
tr	Turn-on Rise Time		--	13	--	nS
td(off)	Turn-Off Delay Time		--	48	--	nS
tf	Turn-Off Fall Time		--	20	--	nS
Qg	Total Gate Charge	VGS=-10V, VDS=-15V, ID=-5A	--	22	--	nC
Qgs	Gate-Source Charge		--	1.0	--	nC
Qgd	Gate-Drain Charge		--	1.8	--	nC
Source-Drain Diode Characteristics						
ISD	Source-Drain Current(Body Diode)		--	--	-20	A
VSD	Forward on Voltage	VGS=0V,IS=-10A	--	--	-1.2	V
trr	Reverse Recovery Time	IF=-10A , dI/dt=100A/μs , TJ=25℃	--	64	--	ns
Qrr	Reverse Recovery Charge		--	25	--	nc

Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature

Notes 3.EAS condition: T_J=25°C

Typical Performance Characteristics

Figure1: Output Characteristics

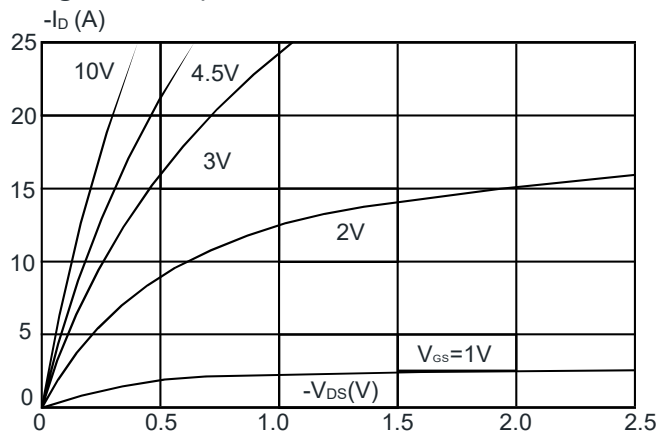


Figure 2: Typical Transfer Characteristics

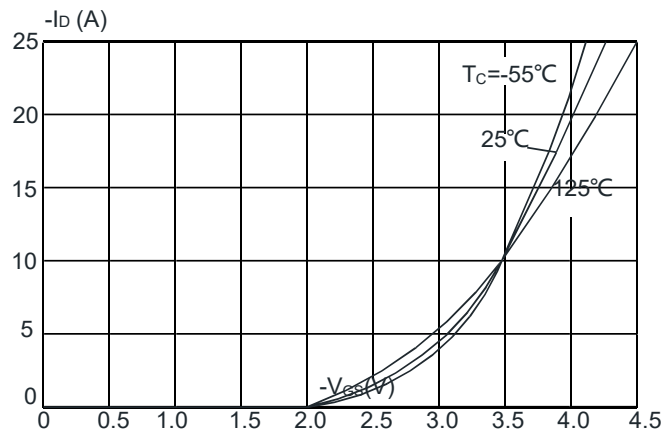


Figure 3: On-resistance vs. Drain Current

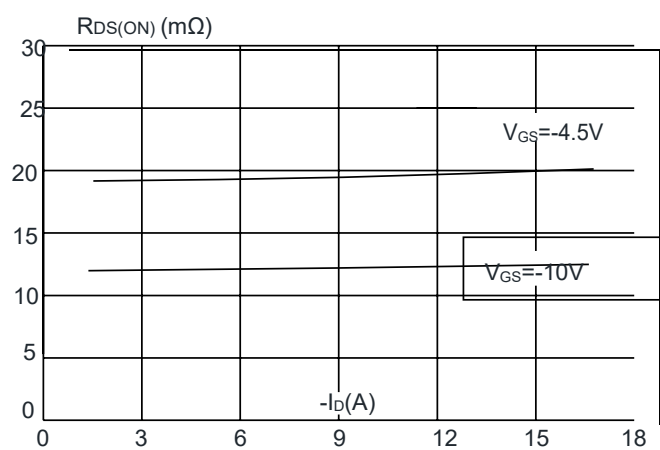


Figure 4 : Body Diode Characteristics

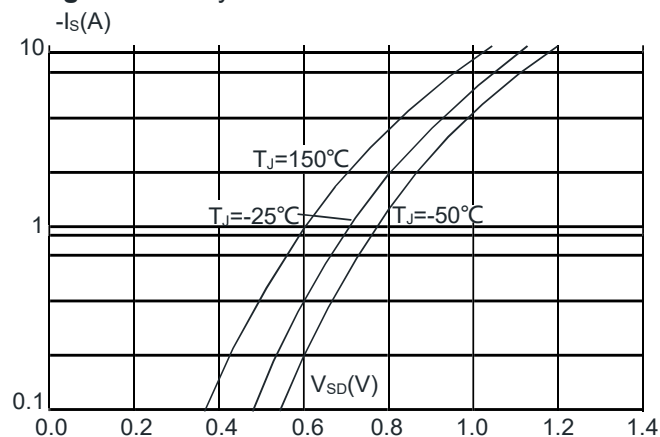


Figure 5: Gate Charge Characteristics

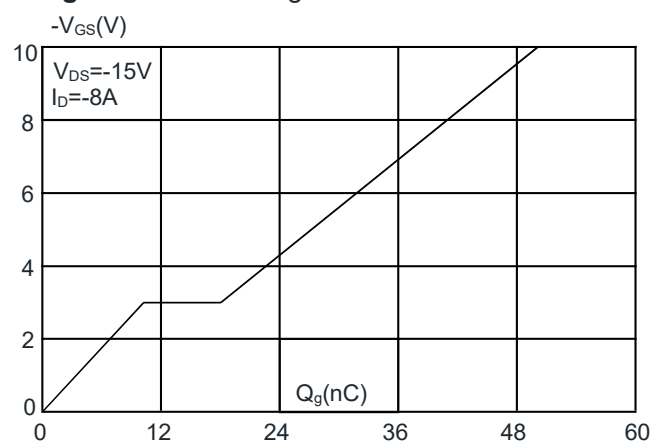


Figure 6: Capacitance Characteristics

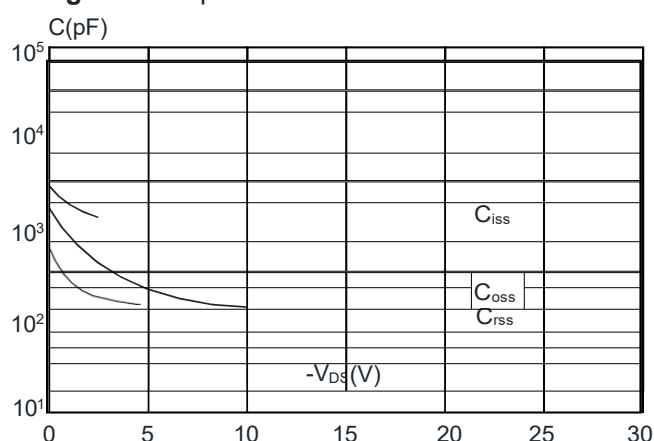


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

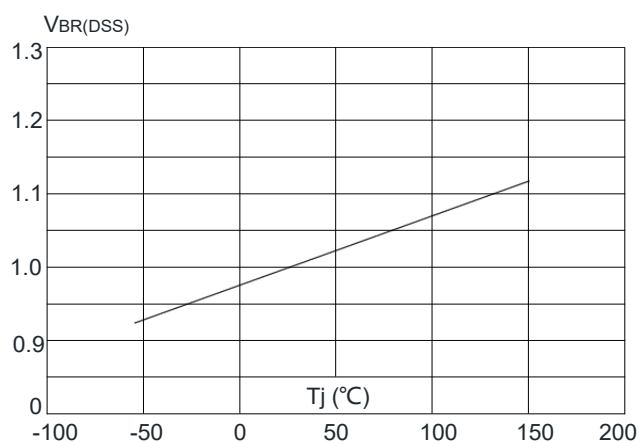


Figure 8: Normalized on Resistance vs. Junction Temperature

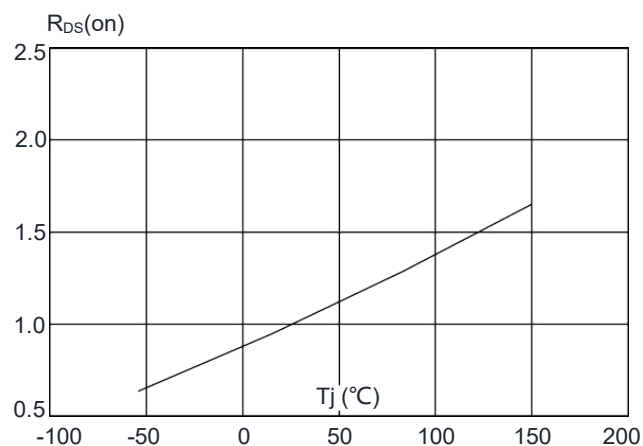


Figure 9: Maximum Safe Operating Area

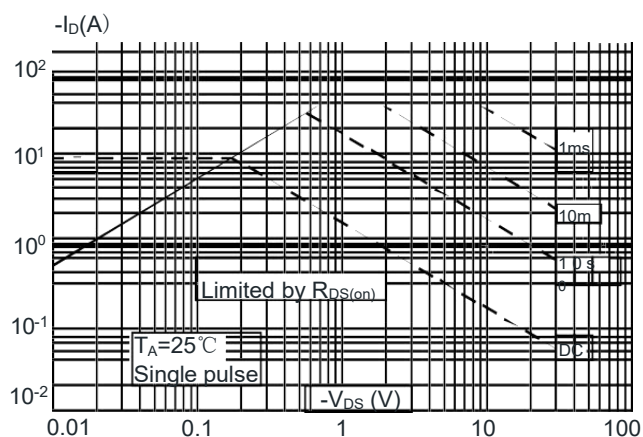


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

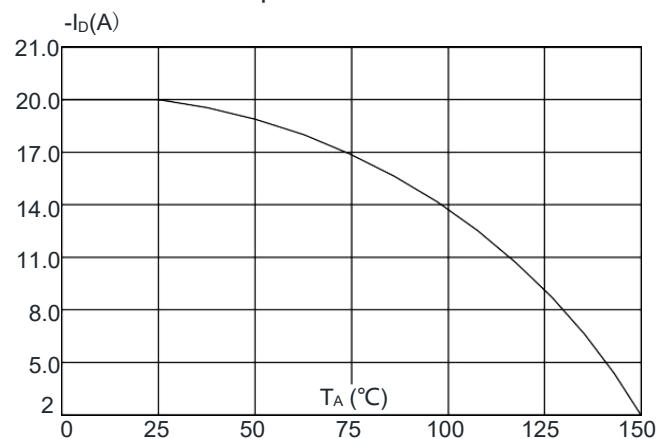
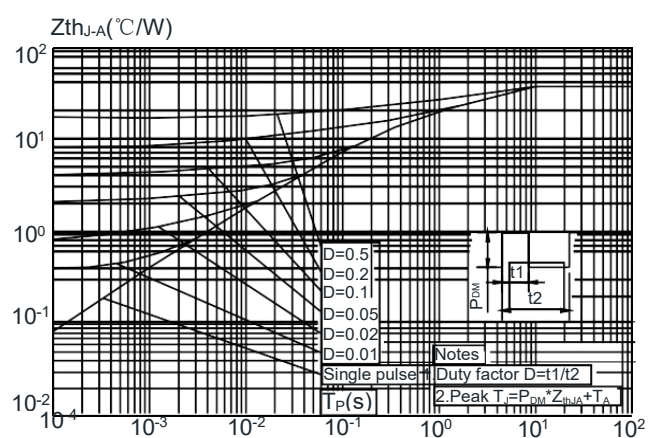
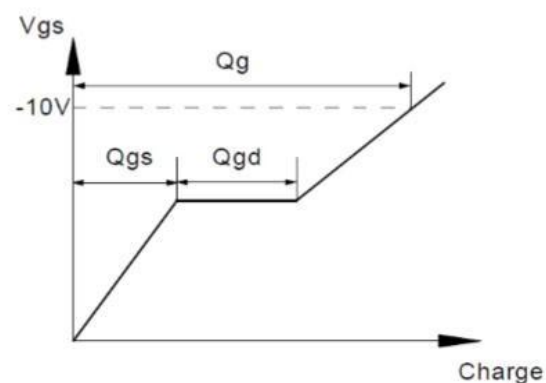
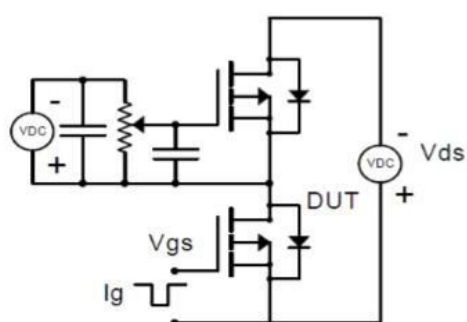


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

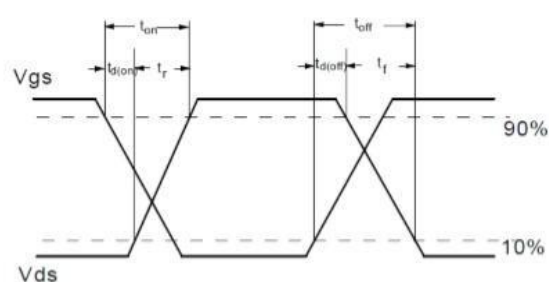
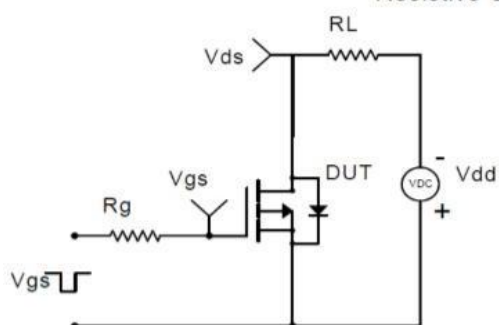


Test Circuit

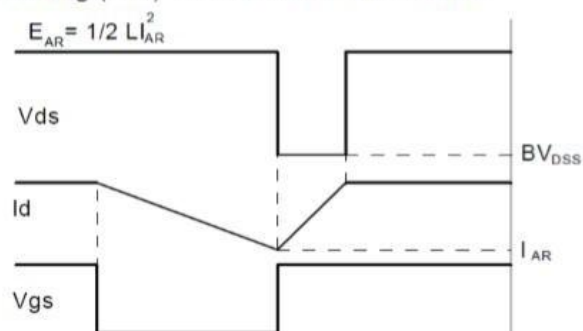
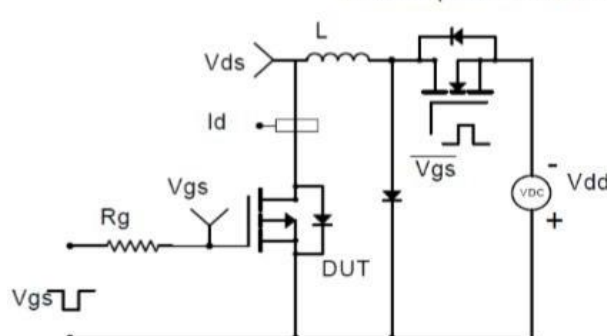
Gate Charge Test Circuit & Waveform



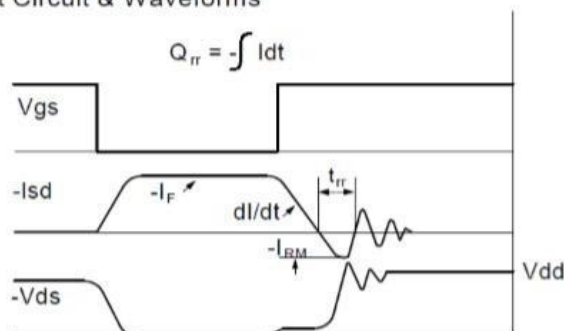
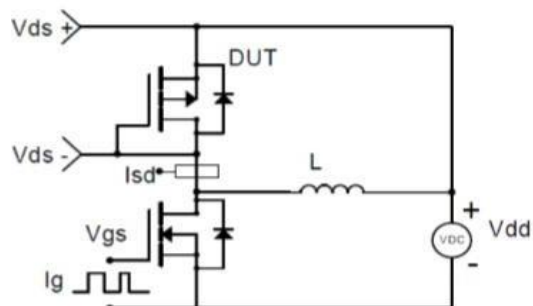
Resistive Switching Test Circuit & Waveforms



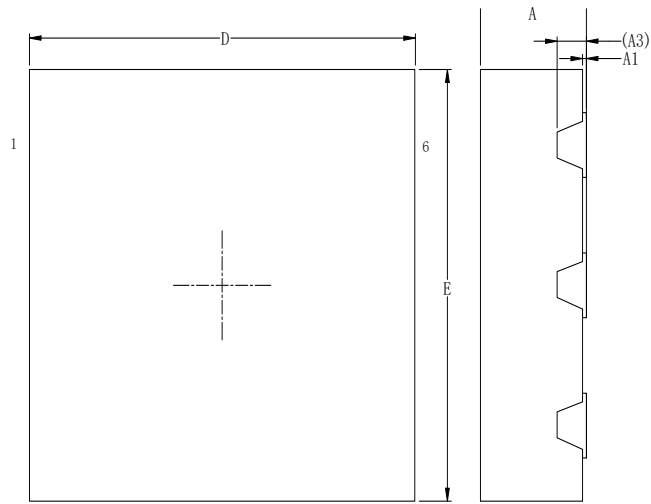
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

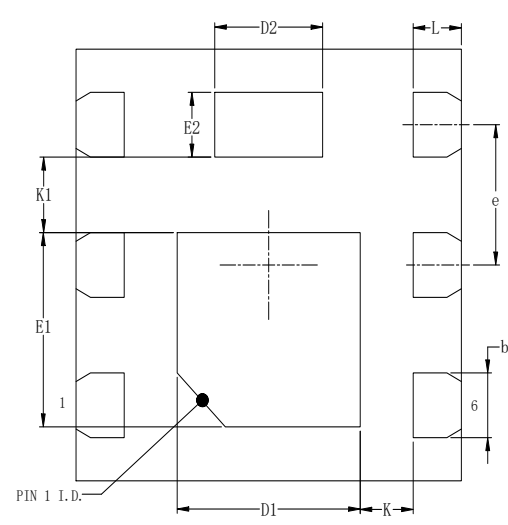


Dimensions (DFN2*2)



TOP VIEW
[顶视图]

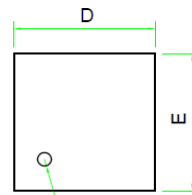
SIDE VIEW
[侧视图]



BOTTOM VIEW

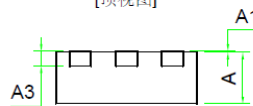
[背视图]

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
L/F THICKNESS		A3	0.152 REF		
LEAD WIDTH		b	0.25	0.3	0.35
BODY SIZE	X	D	1.9	2	2.1
	Y	E	1.9	2	2.1
LEAD PITCH		e	0.65 BSC		
EP SIZE	X	D1	0.85	0.95	1.05
		D2	0.46	0.56	0.66
	Y	E1	0.8	0.9	1
		E2	0.2	0.3	0.4
LEAD LENGTH		L	0.2	0.25	0.3
LEAD TIP TO EP EDGE		K	0.275 REF		
EP EDGE TO EP EDGE		K1	0.35 REF		

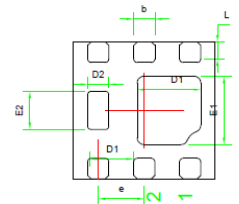


PIN 1#
LASER
MARKING

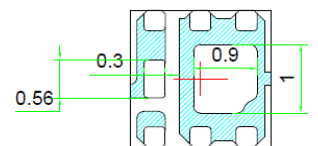
TOP VIEW
[顶视图]



SIDE VIEW
[侧视图]



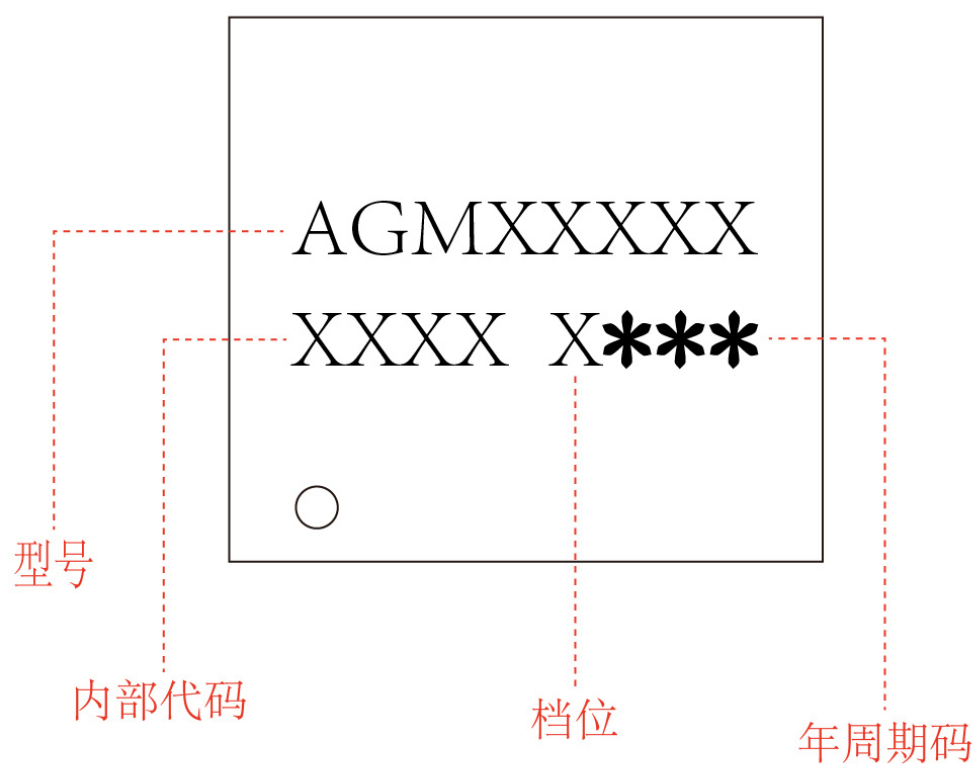
BOTTOM VIEW
[背视图]



Symbol	Dimensions In Millimeters		
	Min	Nom	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	0.203REF		
b	0.250	0.300	0.350
D	1.900	2.000	2.100
D1	0.850	0.900	0.950
D2	0.250	0.300	0.350
e	0.650BSC		
E	1.900	2.000	2.100
E1	0.950	1.000	1.050
E2	0.510	0.560	0.610
L	0.250	0.300	0.350

DFN2*2

Marking Instructions:



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