*Click **here** to ask an associate for production status of specific part numbers.*

MAX20071/MAX20072

Single 600mA/1A 2.2MHz Low-Voltage Step-Down DC-DC Converter

General Description

The MAX20071/MAX20072 high-efficiency switching regulator family delivers up to a 1A load current from 0.5V to 3.8V. The device operates from an input voltage range of 3.0V to 5.5V making it ideal for on-board point-of-load and post-regulation applications. Total output error is less than ±1.5% over load, line, and temperature.

The MAX20071/MAX20072 features fixed-frequency PWM mode operation with a switching frequency of 2.2MHz. High-frequency operation enables an all-ceramic capacitor design and small external components.

The MAX20071/MAX20072 provides an enable input and PGOOD output. The output voltage can be preset at the factory to allow customers to achieve ±1.5% output- voltage accuracy without external 0.1% resistors. In addition, the output voltage can be set to any customer value by using two external resistors at the feedback with 0.5V internal reference. The devices offers a fixed 0.85ms soft-start time.

The 8-pin TDFN exposed pad devices include overtemperature shutdown and overcurrent limiting. All devices are designed to operate from -40°C to +125°C ambient temperature.

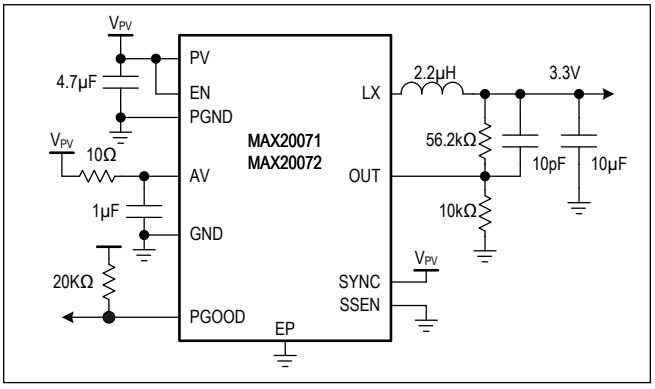
Applications

- Automotive
- Point-of-Load

Benefits and Features

- Rich Feature Set in Ultra-Small Footprint
  - High Efficiency DC-DC Converter
  - Up to 1A Output Current.
  - 3.0V to 5.5V Operating Supply Voltage
  - Resistor Adjustable or Factory-Preset Output Voltage
  - Synchronizable, 2.2MHz Switching Frequency
  - Enable Input
  - PGOOD Output
  - Current-Mode Architecture
  - Optional Spread Spectrum
  - 2mm x 2mm x 0.85mm 8-Pin TDFN
- High-Precision
  - 107% OV Monitor
  - 93% UV Monitor
  - ±1.5% Output-Voltage Accuracy
  - Forced-PWM and Skip Modes
- Protection
  - Overtemperature and Short-Circuit Protection
- -40°C to +125°C Operating Temperature Range

Typical Operating Circuit



Ordering Information appears at end of data sheet.

19-8542; Rev 11; 1/22

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LIST OF FIGURES

Absolute Maximum Ratings

PV to PGND ..... -0.3V to +6V
AV to PGND ..... -0.3V to +6V
PV to AV ..... -0.3V to +0.3V
OUT to PGND ..... -0.3V to V_{AV} + 0.3V
EN, SYNC to PGND ..... -0.3V to V_{PV} + 0.3V
PG to PGND ..... -0.3V to +6.0V
LX to PGND (Note 1) ..... -0.3V to V_{PV} + 0.3V
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
8-TDFN-EP (derate 11.7mW/°C > 70°C) 937.9mW
Operating Temperature ..... -40ºC to +125ºC
Junction Temperature ..... +150ºC
Storage Temperature Range ..... -65ºC to +150ºC
Lead Temperature Range ..... +300ºC

Note 1: Self-protected from transient voltages exceeding these limits in circuit under normal operation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8 TDFN

Package Code	T822+3C
Outline Number	21-0168
Land Pattern Number	90-0065
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	85.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8.9°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{PV} = 5.0V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SV}		3.0		5.5	V
Supply Current	I_{PV_SHDN}	V_{EN} = 0V		0.1	2	µA
	I_{PV_ON}	V_{EN} = 5V, SYNC low, no load		30	60	
UVLO	UVLO	Rising	2.48	2.55	2.9	V
		Falling	2.4	2.475	2.55	
Oscillator Frequency	f_{SW}		2.0	2.2	2.4	MHz
SYNC Input Frequency Range			1.7		2.4	MHz
Spread Spectrum		When enabled		±3		%
Voltage Accuracy	V_{OUT}	SYNC high 2.7V ≤ AV ≤ 5.5V, 0A ≤ I_{LOAD} ≤ I_{MAX}	-1.5		+1.5	%
FB Pullup Current	I_{FB}	FB = 0V, fixed mode	4.7	5	5.3	µA
FB Leakage	I_{FB_LEAK}	FB = 0V and 5V, adjustable mode	-0.5		0.5	µA

Electrical Characteristics (continued)

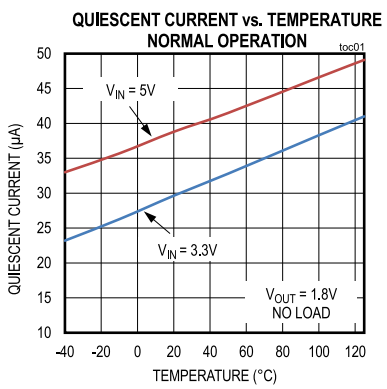
(V_{PV} = 5.0V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C under normal conditions, unless otherwise noted.) (Note 2)

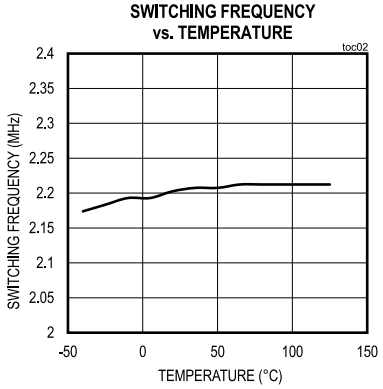
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Load Regulation		0A ≤ I_{LOAD} ≤ I_{MAX} (PWM Mode)		0.02		%/A
DC Line Regulation		PV_ from 2.7V to 5.5V		0.05		%/V
PMOS On-Resistance	HS_{RON}	PV = 5.0V	80	200	300	mΩ
NMOS On-Resistance	LS_{RON}	PV = 5.0V	50	125	200	mΩ
Current-Limit Threshold	I_{LIM}	MAX20071	0.9	1.1		A
		MAX20072	1.4	1.6		
Skip Mode Peak Current	I_{SKIP}	MAX20071		230		mA
		MAX20072		300		
NMOS Zero Crossing Threshold	Z_X			50		mA
Soft-Start Ramp Time	t_{SS}			0.85		ms
Max Duty Cycle	DC_{MAX}				100	%
Min On Time	t_{ONMIN}			40	60	ns
Output Discharge Resistance			20	50	80	Ω
PGOOD						
OV Threshold	OUT_{OV_R}	Rising	105	107	109	%
UV Threshold	OUT_{UV_F}	Falling	91	93	95	%
Active Hold Time	t_{HOLD}			50		µs
Output-Low Level	V_{OL}	I_{SINK} = 3mA		0.1	0.2	V
Output Leakage	I_{HZ}		-0.5		0.5	µA
Propagation Time		5% below UV / 5% above OV threshold	2.5	10	20	µs
THERMAL PROTECTION						
Thermal Shutdown Temperature				+165		ºC
Thermal Shutdown Hysteresis				15		ºC
ENABLE INPUT (EN)						
Input-High Level	V_{IH}	2.7V ≤ AV ≤ 5.5V	1.5			V
Input-Low Level	V_{IL}	2.7V ≤ AV ≤ 5.5V			0.5	V
Hysteresis		2.7V ≤ AV ≤ 5.5V		0.1		V
Pulldown Current		EN = 5.0V	0.5	1	2	µA
SYNCHRONIZATION (SYNC)						
Input High Level	V_{IH}	2.7V ≤ AV ≤ 5.5V	1.5			V
Input Low Level	V_{IL}	2.7V ≤ AV ≤ 5.5V			0.5	V
Hysteresis				0.1		V
Pulldown Resistance			50	100	150	kΩ

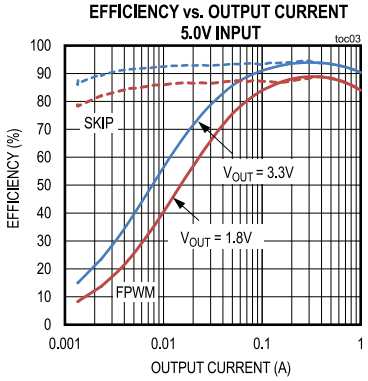
Note 2: All units are 100% production tested at +25°C. All temperature limits are guaranteed by design.

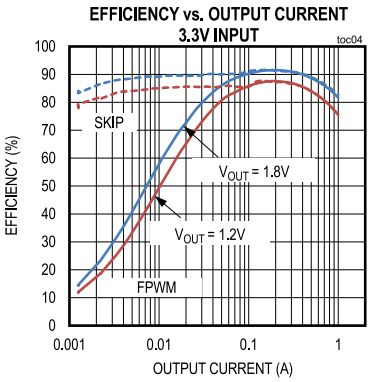
Typical Operating Characteristics

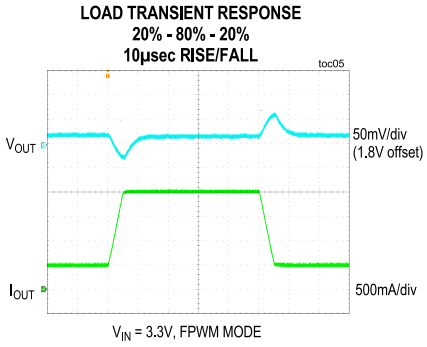
(V_{AV} = V_{PV} = 5.0V, T_A = 25°C, unless otherwise noted.)



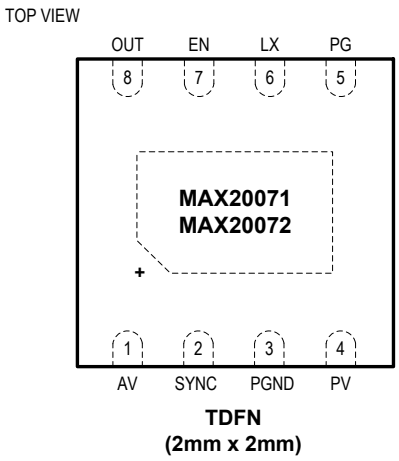








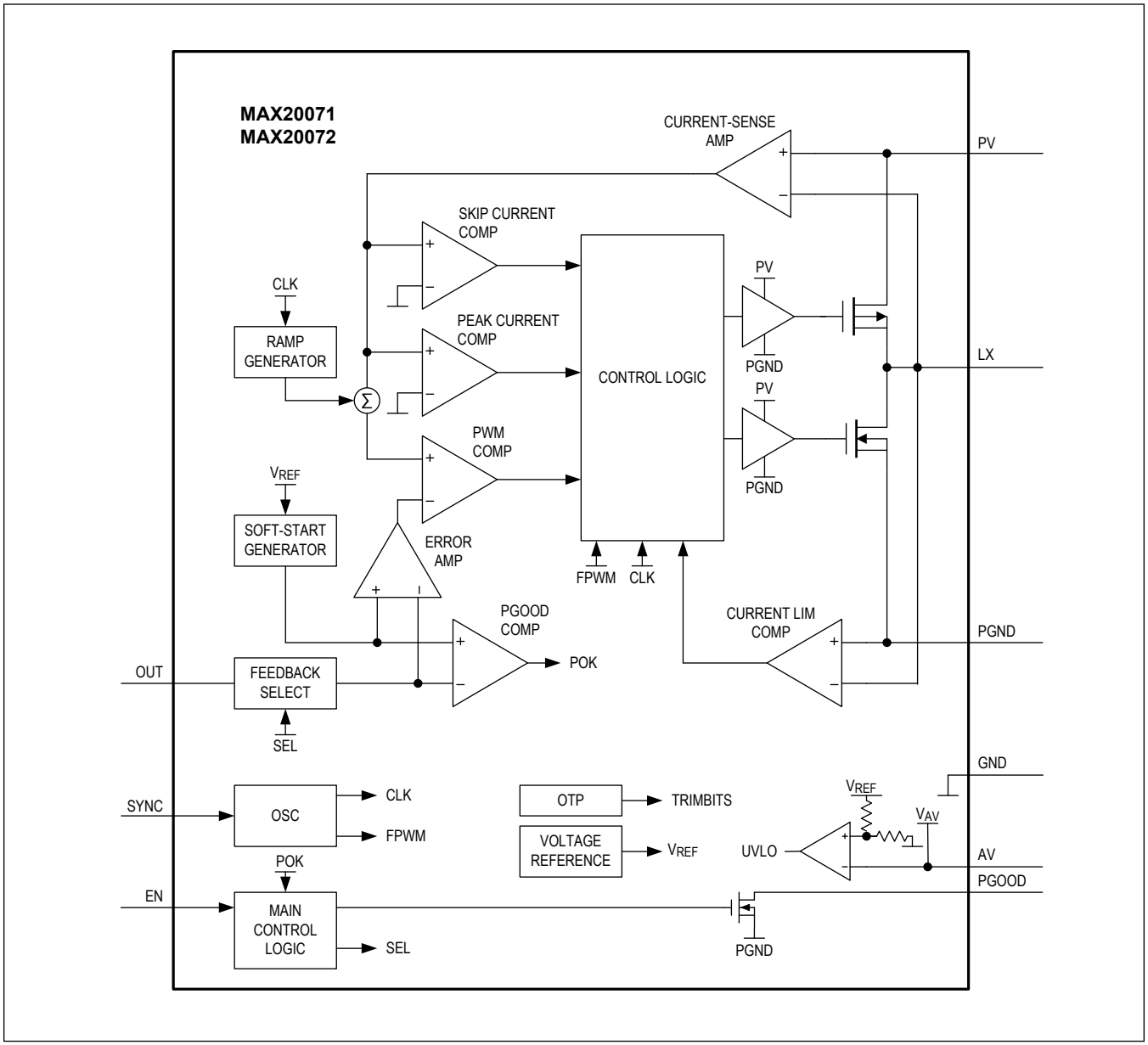
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	AV	Analog Supply. Connect to PV pin. For extra noise immunity, add a 1.0µF capacitor between AV and GND and place a 10Ω resistor in series between AV and the supply.
2	SYNC	SYNC Input. Connect SYNC to GND or leave unconnected to enable skip-mode operation under light loads. Connect SYNC to the input supply or an external clock to enable fixed-frequency forced-PWM-mode operation.
3	PGND	Power Ground.
4	PV	Power Input Supply. Connect a 4.7µF or larger ceramic capacitor from PV to PGND.
5	PG	Active-Low Open-Drain Power-Good Output. External pullup resistor required if used.
6	LX	Inductor Connection. Connect LX to the switched side of the inductor.
7	EN	Active-High Enable Input. Drive EN HIGH for normal operation. On the rising edge the device enters soft-start and on the falling edge the device enters shutdown.
8	OUT	Feedback Input. Connect an external resistive divider from the converter's output to OUT and GND to set the output voltage. Connect to the output capacitor when configured as a fixed output device.
-	EP	Exposed Pad. Connect to ground.

Internal Block Diagram



Detailed Description

The MAX20071/MAX20072 high-efficiency switching regulator family delivers up to 1A load current from 0.5V to 3.8V. The IC operates from 3.0V to 5.5V, making it ideal for on-board point-of-load and post-regulation applications. Total output error is less than ±1.5% over load, line, and temperature.

The ICs feature fixed-frequency PWM-mode operation with a switching frequency of 2.2MHz. High-frequency operation allows for an all-ceramic capacitor design. The high operating frequency also allows for small-size external components.

The low-resistance internal FETs ensure high-efficiency at full load while minimizing critical inductances, making the layout a simple task. Following a simple layout and footprint ensures first-pass success in new designs.

The MAX20071/MAX20072 provide an enable input and power-good output. The output voltage can be preset at the factory in 10mV steps to allow customers to achieve ±1.5% output-voltage accuracy without using expensive 0.1% resistors. In addition, the output voltage can be set to any customer value by using two external resistors at the feedback with 0.50V internal reference.

The devices include overtemperature shutdown and overcurrent limiting. All devices are designed to operate from -40°C to +125°C ambient temperature.

Enable Input

The enable (EN) control input activates the device from the low-power shutdown state. EN has an input threshold of 1.0V (typ) with a hysteresis of 80mV (typ). When the enable input goes high the associated output voltage ramps up with the programmed soft-start time.

PGOOD Output

The device features an open-drain power-good (PG) output that asserts LOW after a 10µs propagation delay when the output voltage drops 7% below, or rises 7% above, the regulated voltage. The PG output will continue to remain LOW for 50µs after the output voltage returns to its regulation point. Connect a pul- lup resistor from PG to the system I/O supply. The pullup resistance should normally be greater than or equal to 2kΩ to ensure that the device can pull down to the specified voltage level.

Spread Spectrum Oscillator

The MAX20071/MAX20072 has a spread spectrum oscillator option which varies the internal operating frequency up by ±3% relative to the internally generated operating frequency of 2.2MHz (typ). This function does not apply to externally-applied oscillation frequency. The spread frequency generated is psuedo-random. See *Ordering Information* for part numbers that have the spread spectrum oscillator enabled.

Synchronization

The devices have an on-chip oscillator that provides a switching frequency of 2.2MHz (typ). Depending on the condition of the synchronization pin (SYNC), two opera- tion modes exist. If SYNC is unconnected or at GND, the device will operate in highly-efficient pulse-skipping mode if the load current is below the skip-mode current threshold. If SYNC is at PV or has a frequency applied to it, the device is in forced PWM mode. The device can be switched during operation between forced PWM mode and skip mode by switching SYNC.

Soft-Start

The devices include a fixed soft-start of 0.85ms. Soft-start time limits start-up inrush current by forcing the output voltage to ramp up towards its regulation point.

Current Limit/Short-Circuit Protection

The devices feature a current limit that protects the device against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. The converter then turns on the low-side MOSFET to allow the inductor current to ramp down. Once the inductor current crosses below the low-side MOSFET current-limit threshold, the converter turns on the high- side MOSFET again. This cycle repeats until the short or overload condition is removed.

PWM/Skip Modes

The device features an input SYNC that puts the converter either in skip mode for forced PWM mode of operation (see *Pin Description* table for mode detail). In PWM mode, the converter switches at a constant frequency with variable on-time. In skip mode, the converter's switching frequency is load dependent until the output load reaches a certain threshold. At higher load currents, the switching frequency does not change and the operating mode is similar to the PWM mode. skip mode helps improve efficiency in light-load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch MOSFETs on and off as often as in PWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

Overtemperature Protection

Thermal overload protection limits the total power dissipation in the device. When the junction temperature exceeds 165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.

Applications Information

Input Capacitors

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. A 4.7µF X7R ceramic capacitor is recommended for the PV pin. A 0.1µF X7R ceramic capacitor is recommended for the AV pin with a series 10Ω resistor to the supply.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). Use the following formulas to determine the minimum inductor value.

Equation 1:

$$L_{MIN1} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times I_{MAX} \times 30\,\%}$$

I_{MAX}	1A or 0.6A depending on part number. Use the maximum output capability of the output channel for the part number being used.
f_{SW}	The operating frequency. This value is 2.2MHz unless externally synchronized to a different frequency.

The next equation ensures that the inductor-current downslope is less than twice the internal slope compensation. For this to be the case the following equation needs to be satisfied:

Equation 2:

$$\frac{-m}{R_{CS}} \geq \frac{m_2}{2}$$

R_{CS}	0.916Ω for 0.6A channel 0.624Ω for 1A channel
m_2	The inductor current downslope.
	$[\frac{V_{OUT}}{L} \times R_{CS}]$
-m	For adjustable versions and fixed output voltages ≤ 3.2V, slope compensation:
	$[0.78\frac{V}{\mu s}]$
	For fixed output versions and output voltages > 3.2V,
	slope compensation : $[0.94\frac{V}{\mu s}]$

Solving for L and adding a 1.3 multiplier to account for tolerances in the system is shown in Equation 3.

Equation 3:

$$L_{MIN2} = V_{OUT} \times \frac{R_{CS}}{2 \times -m} \times 1.3$$

To satisfy both L_{MIN1} and L_{MIN2}, L_{MIN} must be set to the larger of the two.

$$L_{MIN} = \max(L_{MIN1}, L_{MIN2})$$

The maximum inductor value recommended is 2 times the chosen value from the above formula.

$$L_{MAX} = 2 \times L_{MIN}$$

Select a nominal inductor value based on the following formula:

$$L_{MIN} < L_{NOM} < L_{MAX}$$

Output Capacitor

The MAX20071/MAX20072 is designed to be stable with low-ESR ceramic capacitors. Other capacitor types are not recommended as the ESR zero can affect stability of the device. The output capacitor calculations below are guidelines based on nominal conditions. The phase margin must be measured on the final circuit to verify proper stability is achieved.

Equation 4:

$$C_{OUT\_MIN} = 10.5\mu s \times \frac{I_{MAX}}{V_{OUT}}$$

$$C_{OUT\_NOM} = 27.5\mu s \times \frac{I_{MAX}}{V_{OUT}}$$

$$C_{OUT\_MAX} = 3 \times C_{OUT\_NOM}$$

where:

C_{OUT_MIN} = The minimum fully derated output capacitance needed for a stable output.

C_{OUT_NOM} = The nominal output capacitance. This capacitance value will normally provide the highest stability.

C_{OUT_MAX} = The maximum recommended output capacitance. Increased capacitance beyond this value is not recommended without measuring the phase margin to insure acceptable stability.

I_{MAX} = The maximum DC current capability.

I_{MAX} = 0.6A (MAX20071)
I_{MAX} = 1A (MAX20072)

V_{OUT} = Nominal output voltage

Adjustable Output-Voltage Option

The MAX20071/MAX20072's adjustable output voltage version (see *Ordering Information*) allows the customer to set the outputs to any voltage between 0.5V and approximately PV-0.5V. The actual maximum output voltage setting will be limited by the specific application conditions and components. Connect a resistive divider from output (V_{OUT}) to OUT to GND to set the output voltage (Figure 1). Select R_2 (OUT to GND resistor) ≤ 100kΩ. Calculate R_1 (V_{OUT} to OUT resistor) with the following equation.

Equation 5:

$$R_1 = R_2[(\frac{V_{OUT}}{V_{FB}}) - 1]$$

where VFB = 500mV (see the *Electrical Characteristics* table).

The external feedback resistive divider must be frequency compensated for proper operation. Place a capacitor across R1 in the resistive divider network. Use the following equation to determine the value of the capacitor.

Equation 6:

$$C_1 = 50\frac{R_2}{R_1}pF$$

PCB Layout Guidelines

Several guidelines should be followed to obtain the best performance from the device:

- Place several vias in the exposed pad (EP) and connect them to all ground layers below the part. EP is attached to the die with epoxy, making it a good method of transferring heat out of the IC. A line of three 0.3mm diameter vias is recommended.
- Place all DC-DC components on the same layer as the IC, and locate them as close as possible to the IC. Route the traces in a tight loop. Trace length (shorter is better) should be prioritized over trace thickness. This decreases the loop area of the circuit, minimizing EMI and jitter.
- The layer directly below the IC and DC-DC components should be a solid ground plane. Connect the GND pins of the

device and components together with a low-impedance connection and add several vias to GND near those pins. Do not split the ground plane at or near the circuit. See Figure 2 for an example layout of IC and DC-DC components.

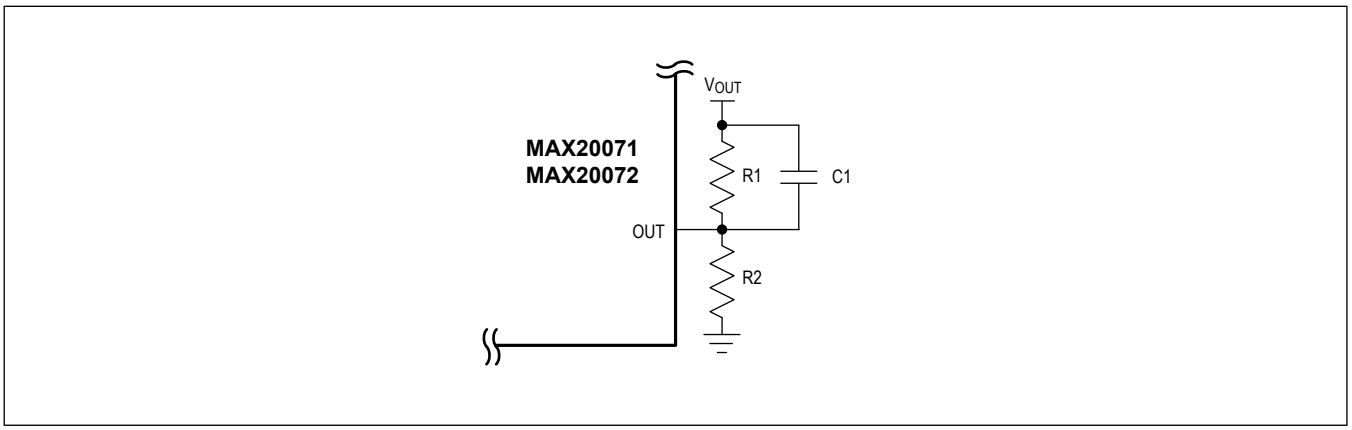


Figure 1. Adjustable Output-Voltage Configuration

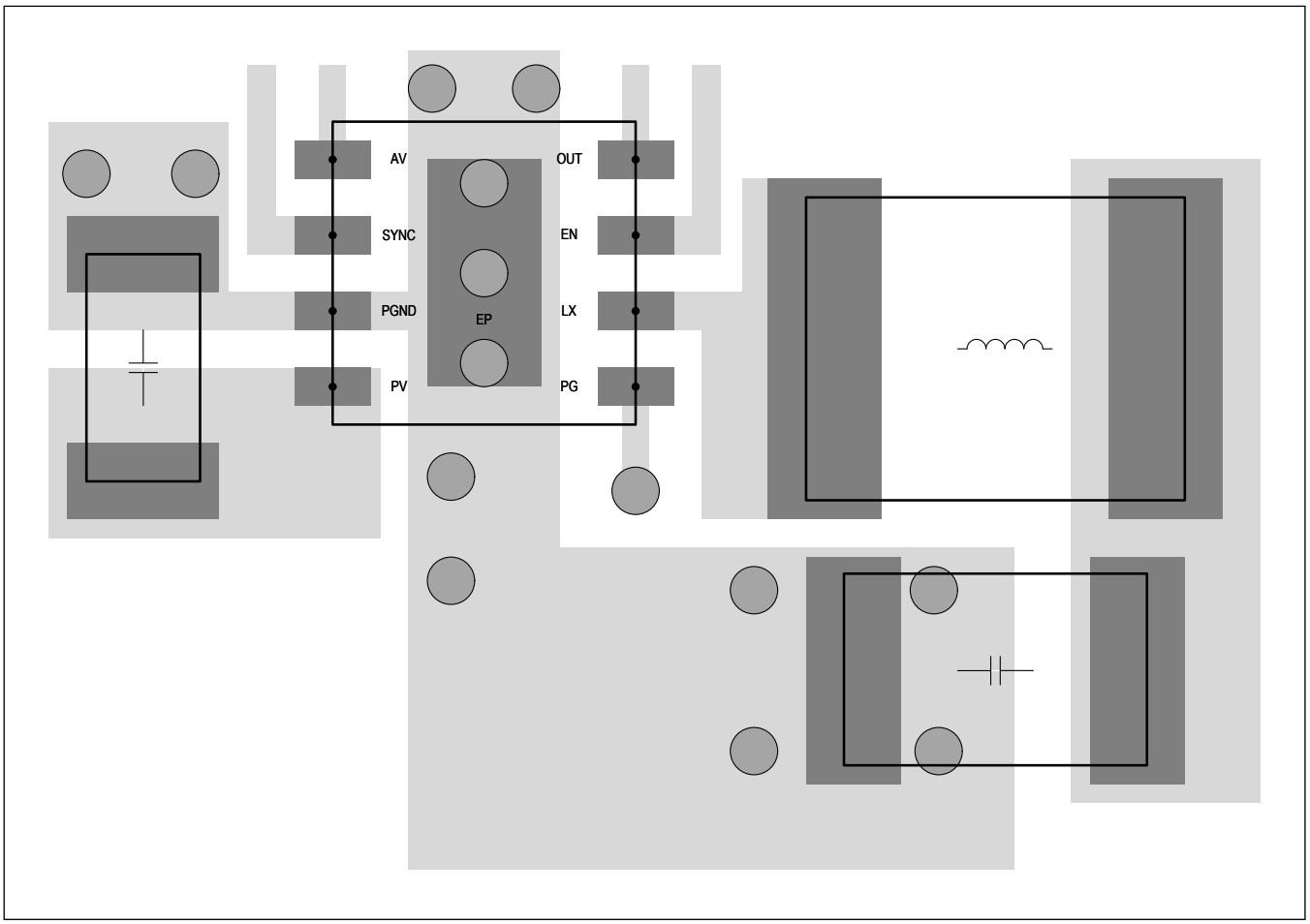


Figure 2. Example Layout of IC and DC-DC Components

Ordering Information

PART	V_{OUT} (V)	I_{OUT} (A)	SPREAD SPECTRUM	PIN-PACKAGE
MAX20071ATAA/V+	Adjustable	0.6	Off	8 TDFN-EP*
MAX20071ATAA/V+T	Adjustable	0.6	Off	8 TDFN-EP*
MAX20071ATAB/V+	Adjustable	0.6	On	8 TDFN-EP*
MAX20072ATAA/V+	Adjustable	1.0	Off	8 TDFN-EP*
MAX20072ATAA/V+T	Adjustable	1.0	Off	8 TDFN-EP*
MAX20072ATAB/V+	1.2V	1.0	On	8 TDFN-EP*
MAX20072ATAC/V+	1.15V	1.0	On	8 TDFN-EP*
MAX20072ATAD/V+	Adjustable	1.0	On	8 TDFN-EP*

/V Denotes automotive-qualified parts.

+Denotes a lead(Pb) free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/16	Initial release	—
1	7/16	Changed UVLO max range from 2.6V to 2.65V in *Electrical Characteristics*	2
2	9/17	Updated *Absolute Maximum Ratings*, Package Thermal Characteristics, pins 1, 7, 8 in *Pin Description*, *Detailed Description*, *Input Capacitors* section, and added *PCB Layout Guidelines* section and Figure 2	2, 5, 7, 8, 9
3	11/17	Added MAX20072ATAB/V+ and MAX20072ATAC/V+ as future products in *Ordering Information* table	10
4	1/18	Added tape-and-reel variants (MAX20071ATAA/V+T and MAX20072ATAA/V+T) to *Ordering Information* table	10
5	2/18	Added new variant (MAX20071ATAB/V+) to *Ordering Information* table	10
6	7/18	Removed future product designation from MAX20072ATAB/V+ and MAX20072ATAC/V+ in the *Ordering Information* table	10
7	9/18	Updated *Ordering Information* table	11
8	7/19	Updated *Absolute Maximum Ratings* and *Package Information*	2
9	1/20	Updated *Detailed Description*	8
10	10/20	Updated *General Description*, *Pin Descriptions*, and *Detailed Description*	1, 7, 9, 11
11	1/22	Updated *Ordering Information* table	14