MPQ5029

USB Charging Port Controller with Integrated Current Limit Switch and Short-to-Battery Protection for Automotive, AEC-Q100 Qualified

DESCRIPTION

The MPQ5029 is a fully integrated, USB Type-C port controller that integrates a low $R_{DS(ON)}$ USB current-limit switch and charging port identification circuits. The MPQ5029 supports 3A of continuous output current.

The output of the USB switch is current-limit programmable. The MPQ5029 supports DCP schemes for battery charging specification (BC1.2), divider mode, 1.2V/1.2V mode, and quick-charge specification (QC3.0) without the need for external user interaction. The MPQ5029 can also support Type-C 5V @ 3A DFP mode.

The MPQ5029 provides programmable linear line drop compensation.

Full protection features include hiccup current limiting, input over-voltage protection (OVP), and thermal shutdown.

The MPQ5029 requires a minimal number of readily available, standard, external components to complete the USB switch and charging mode auto-detection solution. The MPQ5029 is available in a QFN-14 (2mmx3mm) package.

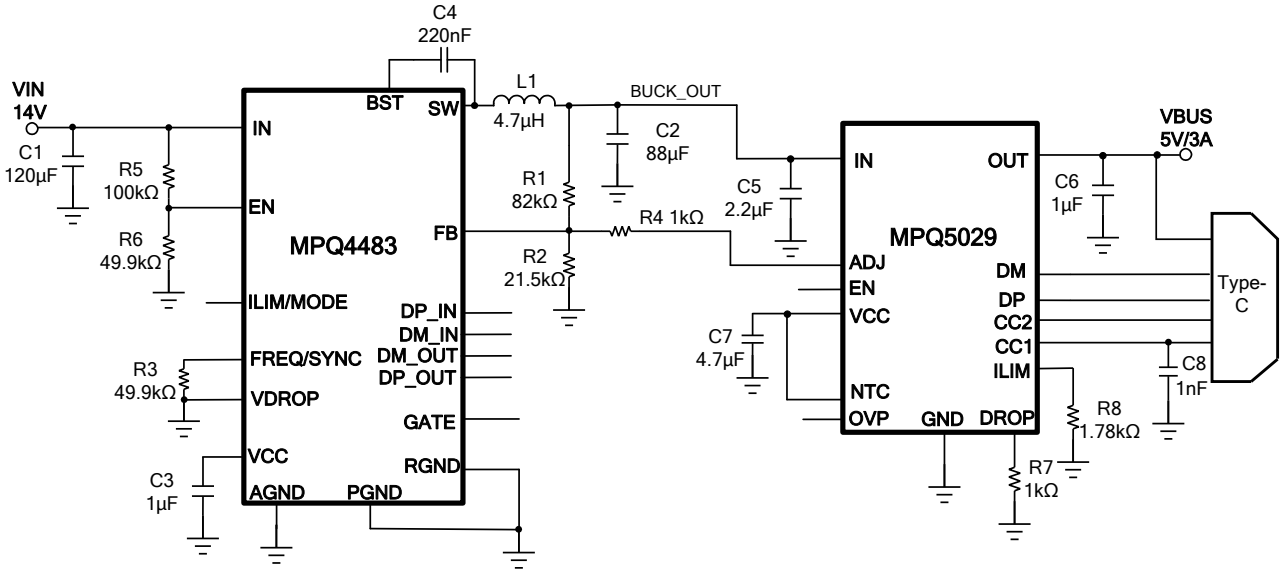
FEATURES

- Up to 22V Voltage Rating for Input and Output
- Supports Type-C 5V @ 3A DFP Mode
- Supports QC3.0 (3.6 - 12V Output) Mode
- Supports 5V DCP Schemes for BC 1.2, Divider Mode, 1.2V/1.2V Mode
- I/O Pins (DP, DM, CC1, and CC2) Support Short-to-Battery Protection
- OUT Short-to-Battery Protection when V_{BUS} is Enabled
- Line Drop Compensation for 5V Output
- Programmable High-Accuracy Current Limit
- 25mΩ Low $R_{DS(ON)}$ Power MOSFET
- NTC Pin for Thermal Management
- OVP Pin to Program Charging Mode
- Input Over-Voltage Discharge
- USB-IF Type-C Certified
- ±4kV HBM ESD Rating for I/O Pins: OUT, DP, DM, CC1, and CC2
- Available in a QFN-14 (2mmx3mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- USB Charging Ports
- Type-A, Type-C, QC Charging Ports,
- Remote Charging Ports

TYPICAL APPLICATION



Type-C and Compatible with Legacy USB2.0 Charging Port

ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ5029GD-AEC1	QFN-14 (2mmx3mm)	*See Below*

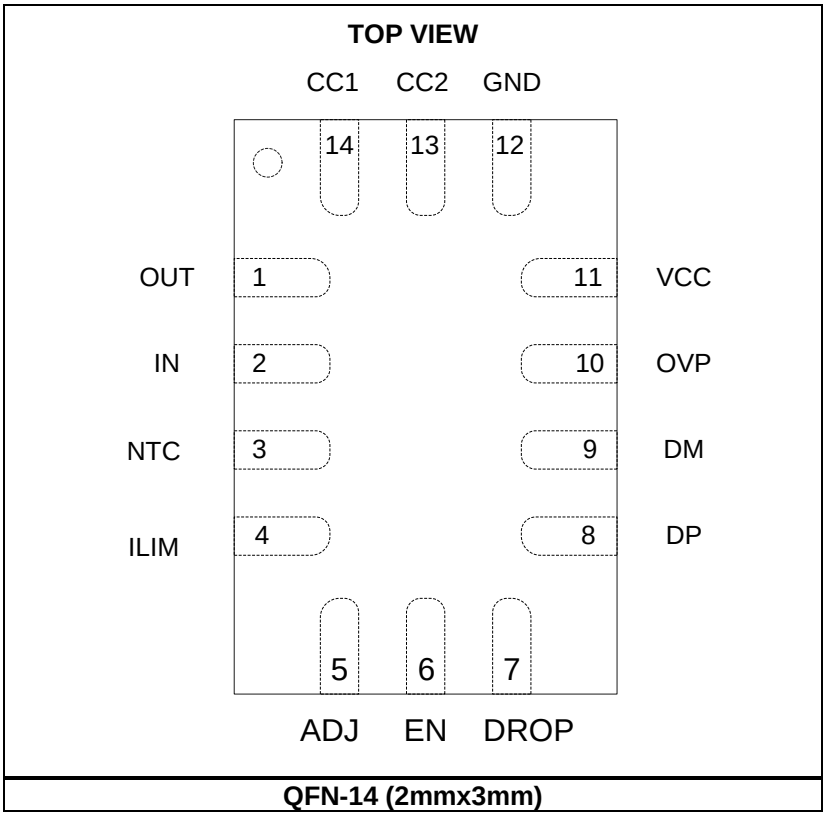
* For Tape & Reel, add suffix –Z (e.g.: MPQ5029GD-AEC1–Z).

TOP MARKING

BDD
YWW
LLL

BDD: Product code of MPQ5029GD-AEC1
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-14 (2mmx3mm)

PIN FUNCTIONS

Package Pin #	Name	Description
1	OUT	**Output of USB current-limit switch.**
2	IN	**Supply voltage.** The MPQ5029 can operate with a 5V typical input voltage for Type-C or USB2.0 applications or a 3.6 - 12V input voltage for QC3.0 applications.
3	NTC	**Thermistor input.** Connect a resistor from NTC to VCC. Connect the thermistor from NTC to ground. Connect NTC to VCC to disable the thermal sense function.
4	ILIM	**Current-limit level set.** Place a resistor between ILIM and GND for a high-accuracy current limit.
5	ADJ	**Output voltage adjustment pin.** ADJ sinks a current from the upstream DC/DC converter's FB pin to ground to regulate the DC/DC converter's output voltage. ADJ also supports a line drop compensation function.
6	EN	**Enable control pin.** Apply a logic high voltage to EN to enable the IC. Pull EN to logic low to disable the IC. EN has an internal 6.5μA auto-pull-up current to the internal 3.5V power supply.
7	DROP	**Line drop amplitude set pin.** Continuous adjustment available via a resistor.
8	DP	**D+ data line to USB connector.** DP is the input/output used for handshaking with portable devices. DP is a high-voltage pin.
9	DM	**D- data line to USB connector.** DM is the input/output used for handshaking with portable devices. DM is a high-voltage pin.
10	OVP	**MPQ5029 OVP and operation mode selection.** Connect OVP to VCC, float OVP, or short OVP to ground to select three different modes.
11	VCC	**Internal 3.5V LDO output.** Bypass VCC with a 4.7μF ceramic capacitor.
12	GND	**Ground pin.**
13	CC2	**Configuration channel.** CC2 is used to detect connections and configure the interface across the USB Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.
14	CC1	**Configuration channel.** CC1 is used to detect connections and configure the interface across the USB Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +24V
Output voltage (V_{OUT}).....-0.3V to +24V
CC1, CC2, DM, DP .....-0.3V to +24V
EN pin ..... -0.3V to +4V or 0.1mA for >4V
All other pins .....-0.3V to +4V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = +25°C) (2)
..... 3.29W

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 5V or 3.6V - 12V (QC3.0) (4)
Output voltage (V_{OUT})..... Follow with V_{IN}
Output current (I_{OUT}).....Up to 3A
Operating junction temp. (T_J).. -40°C to +125°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***	
QFN-14 (2mmx3mm)			
EVQ5029-D-00A (5)	38	12	°C/W
JESD51-7 (6)	70	15	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Measured on a EVQ5029-D-00A, 4-layer PCB, 50mmx50mm, 2Oz outer layer and 1Oz inner layer copper.
3) The device is not guaranteed to function outside of its operating conditions.
4) For lower V_{IN} applications, refer to the Operation section on page 15 for detail.
5) Measured on an EVQ5029-D-00A, 4-layer PCB, 50mmx50mm, 2Oz outer layer and 1Oz inner layer copper.
6) Measured on a JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to 125°C [7], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO1}	ADJ begins working	2.15	2.4	2.65	V
UVLO hysteresis	$V_{UVLOHYS1}$			120		mV
Second V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO2}	Power MOSFET turn-on	2.7	2.85	3	V
Second UVLO hysteresis	$V_{UVLOHYS2}$			300		mV
EN rising threshold	V_{EN_R}		1.9	2.0	2.1	V
EN hysteresis	V_{EN_F}			100		mV
EN auto pull-up current	I_{EN_UP}		4	6.5	9	µA
VCC voltage	V_{VCC}	I_{CC} = 0mA	3.35	3.5	3.65	V
Shutdown current	I_{Q_STD}	EN = 0		22	40	µA
Supply current	I_Q	V_{IN} = 5V, Type-C detach mode, does not contain Type-C pull-up current		155	200	µA
		V_{IN} = 5V, no load, CC1 = 5.1kΩ, does not contain Type-C pull-up current		220	300	
USB Power MOSFET						
On resistance	$R_{DS(ON)}$	V_{IN} = 5V		25	45	mΩ
Input discharge resistance	R_{DIS_IN}	Turn-on during V_{IN} OVP or H to L voltage change period	150	200	250	Ω
Soft-start time	T_{SS}	V_{IN} = 5V, no load, 10% to 90%	200	450	700	µs
Current Limit Set						
USB current limit	I_{LIMIT1}	R_{ILIM} = 1.78kΩ, room temperature, Type-C mode	3.18	3.55	3.93	A
	I_{LIMIT2}	R_{ILIM} = 1.78kΩ, room temperature, Type-A mode	2.5	2.75	3	A
Output Voltage Control						
Default V_{IN} voltage	V_{IN_Def1}	I_{OUT} = 0A, room temperature	-1%	5.1	+1%	V
	V_{IN_Def2}	Full temperature	-2%	5.1	+2%	V
9V_{IN} voltage	V_{IN_9}	Room temperature	-1.5%	9	+1.5%	V
12V_{IN} voltage	V_{IN_12}	Room temperature	-1.5%	12	+1.5%	V
Line drop compensation	$V_{IN\_5\_C}$	I_{OUT} = 3A, R_{DROP} = 1kΩ		260	400	mV
Protection						
V_{IN} OVP threshold @ OVP pin = GND	V_{OV_TH}	V_{IN} rising edge, V_{IN} = 5V	110	115	120	%
		V_{IN} rising edge, V_{IN} = 9V		115		
		V_{IN} rising edge, V_{IN} = 12V		115		
V_{IN} OVP threshold @ OVP pin = high	V_{OV_TH2}		5.5	5.75	6	V
V_{IN} OVP recovery threshold	$V_{OV\_Recovery}$	Reset mode to 5V default	5.25	5.45	5.65	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to 125°C [7], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
OVP deglitch time [8]	T_{OVP_DE}			10		µs
OVP high threshold	V_{MODE_H}		2			V
OVP float threshold	V_{MODE_F}	Internal divider from VCC	1.35		1.65	V
OVP low threshold	V_{MODE_L}				0.7	V
OCP on time of hiccup	T_{HIC_ON}			2		ms
OCP off time of hiccup	T_{HIC_OFF}			2		s
External thermal sense trip threshold	V_{NTC_R}	R3 = 16.6kΩ, R4 = 1.66kΩ (80°C)	6	9	12	%VCC
External thermal sense recovery threshold	V_{NTC_F}	R3 = 16.6kΩ, R4 = 3kΩ (60°C)		16.5		%VCC
Shutdown temperature [8]	T_{STD}			150		°C
Hysteresis [8]	T_{HYS}			25		°C
BC 1.2 DCP Mode						
DP/DM short resistance	R_{DP/DM_Short}	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = 25°C			40	Ω
		V_{DP} = 0.8V, I_{DM} = 1mA, full temperature			45	Ω
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$		1.1	1.2	1.3	V
DP/DM output impedance	$R_{DP/DM\_1.2V}$		200	300	400	kΩ
Divider Mode						
DP/DM output voltage	$V_{DP/DM}$	V_{IN} = V_{OUT} = 5V	2.5	2.7	2.85	V
DP/DM output impendence	$R_{DP/DM}$		20	25	30	kΩ
Quick-Charge 3.0 Mode						
Data detect voltage	V_{DAT_REF}		0.25	0.3	0.4	V
Output voltage select ref	V_{SEL_REF}		1.8	2.0	2.2	V
DP output impendence	R_{DP_QC}		300	400	1500	kΩ
DM output impendence	R_{DM_QC}		15	20	25	kΩ
DM low glitch time [8]	T_{Glitch_DM}			10		ms
DP high glitch time	T_{Glitch_DP}		0.8	1.2	1.6	s
Output voltage change glitch time	$T_{Glitch\_V\_Change}$		20	40	60	ms
Bus voltage step	$V_{BUS\_CONT\_STEP}$		150	200	250	mV
Time for V_{BUS} to discharge to 5V when DP < 0.6V [8]	T_{V_UNPLUG}				500	ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to 125°C [7], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
USB Type-C 5V/3A Mode - Both CC1 and CC2 Pins						
CC resistor to disable Type-C mode	R_A	CC1 pin	90		100	kΩ
CC voltage to enable V_{CONN}	V_{Ra}				0.75	V
CC voltage to enable V_{BUS}	V_{Rd}	Use 0.8V and 2.6V as threshold	0.85		2.45	V
CC detach threshold	V_{OPEN}	Use 2.6V as threshold	2.75			V
CC voltage at 5.1kΩ Rd	V_{CC_Rd}	CC pin pull-down by 5.1kΩ	1.31		2.04	V
CC voltage falling de-bounce timer	$T_{CC\_debounce}$	V_{BUS} enable deglitch	100	150	200	ms
CC voltage rising de-bounce timer	$T_{PD\_debounce}$	V_{BUS} disable deglitch	5	10	20	ms
V_{CONN} output power	P_{VCONN}	V_{CONN} comes from MPQ5029 input with some series resistance	1			W
V_{BUS} to ground impedance	R_{BUS}	Type-C detach, output discharge is turned off in this case	72.4			kΩ

NOTES:

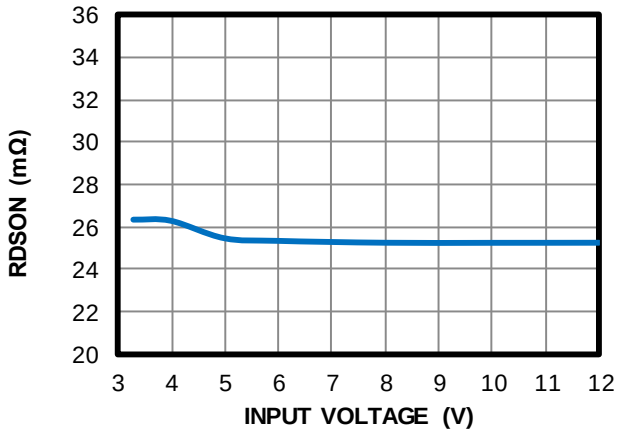
7) Not tested in production. Guaranteed by over-temperature correlation.

8) Guaranteed by engineering sample characterization.

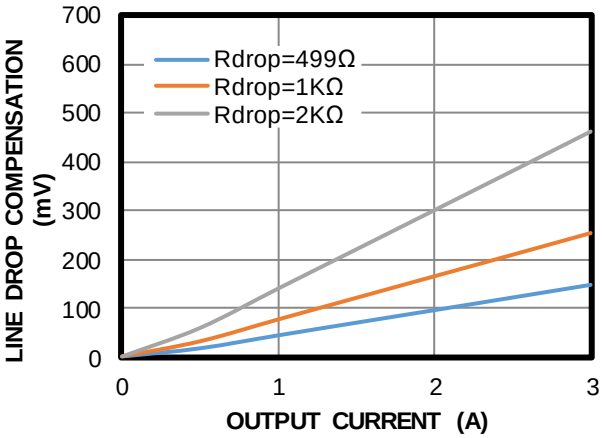
TYPICAL CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.78kΩ, T_A = 25°C, unless otherwise noted.

$R_{DS(ON)}$ vs. Input Voltage

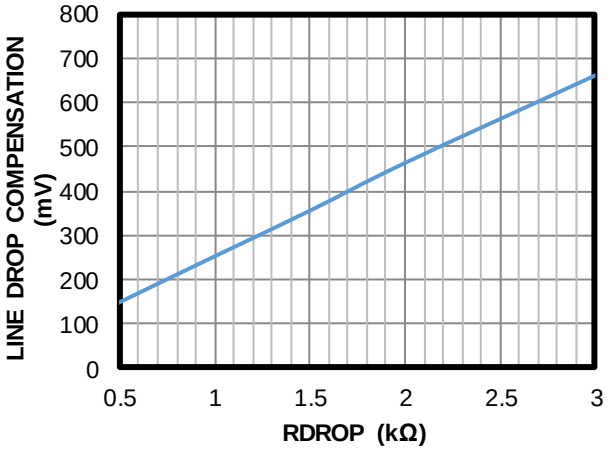


Line Drop Compensation vs. Output Current

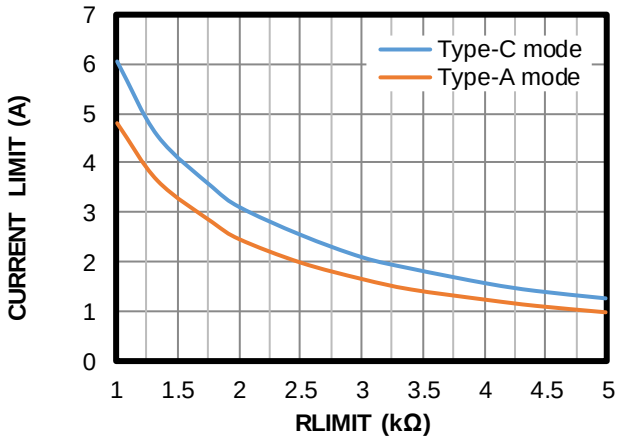


Line Drop Compensation vs. R_{DROP}

V_{IN} = 5V, I_{OUT} = 3A



Current Limit vs. R_{LIMIT}

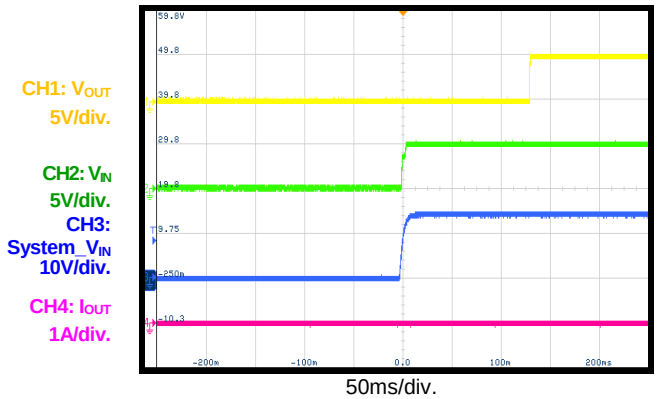


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.78kΩ, T_A = 25°C, unless otherwise noted. Connect MPQ5029 input to MPQ4483 output, System_VIN = 14V is MPQ4483 input voltage.

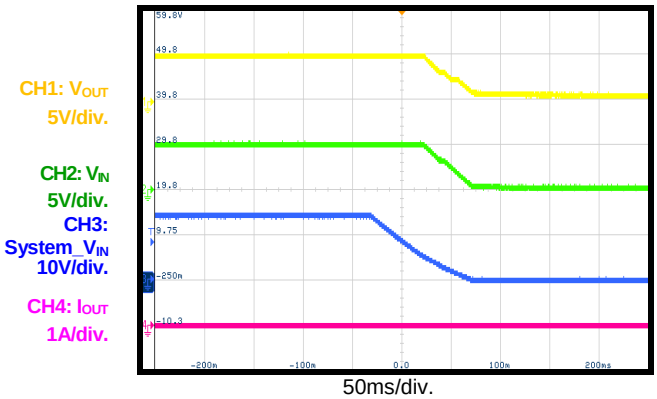
Start-Up through Input Voltage

I_{OUT} = 0A



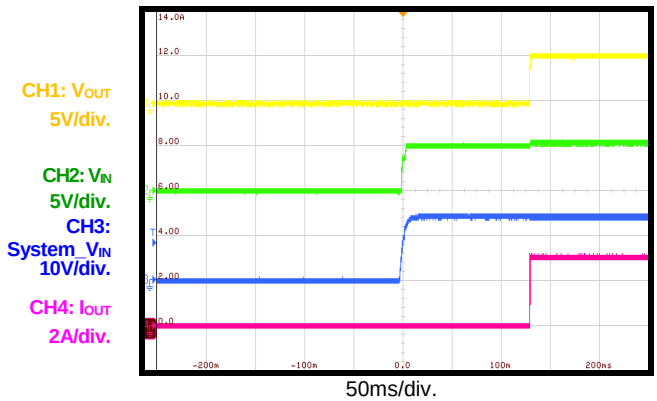
Shutdown through Input Voltage

I_{OUT} = 0A



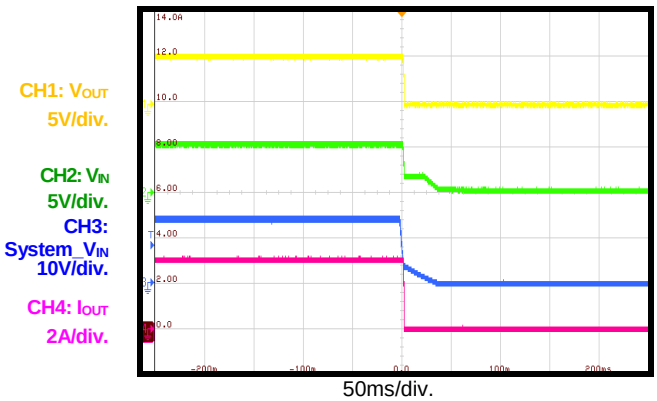
Start-Up through Input Voltage

I_{OUT} = 3A



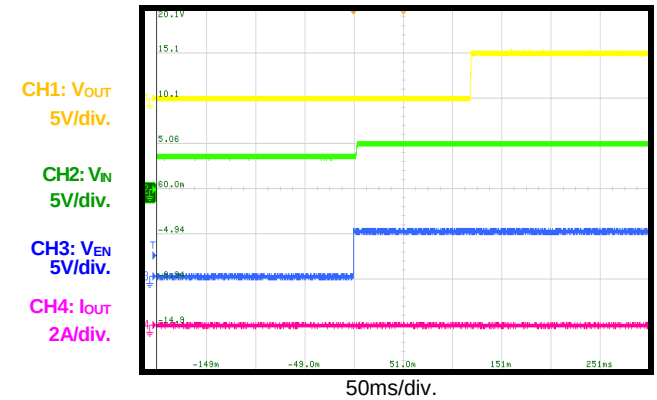
Shutdown through Input Voltage

I_{OUT} = 3A



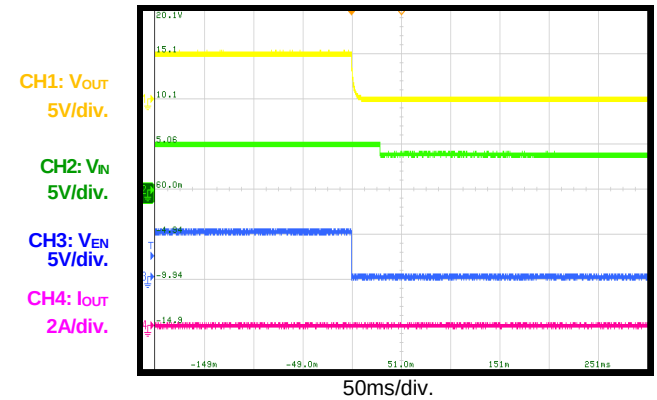
EN Start-Up

I_{OUT} = 0A



EN Shutdown

I_{OUT} = 0A

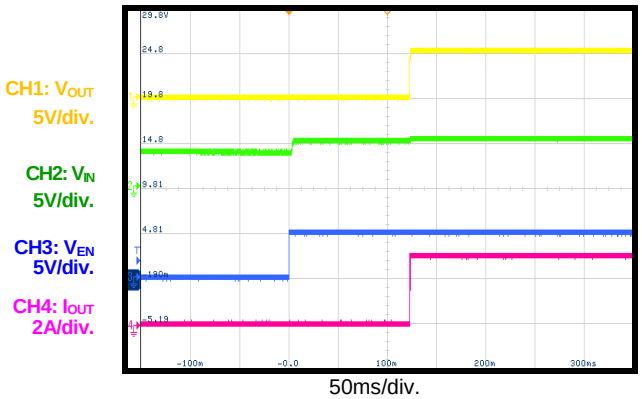


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.78kΩ, T_A = 25°C, unless otherwise noted. Connect MPQ5029 input to MPQ4483 output, System_VIN = 14V is MPQ4483 input voltage.

EN Start-Up

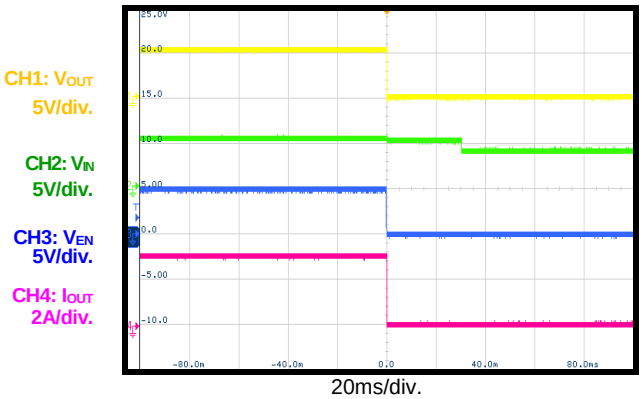
I_{OUT} = 3A



50ms/div.

EN Shutdown

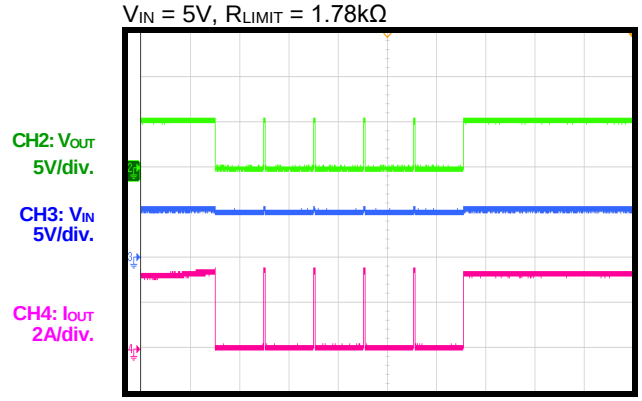
I_{OUT} = 3A



20ms/div.

Over-Current Protection Entry and Recovery

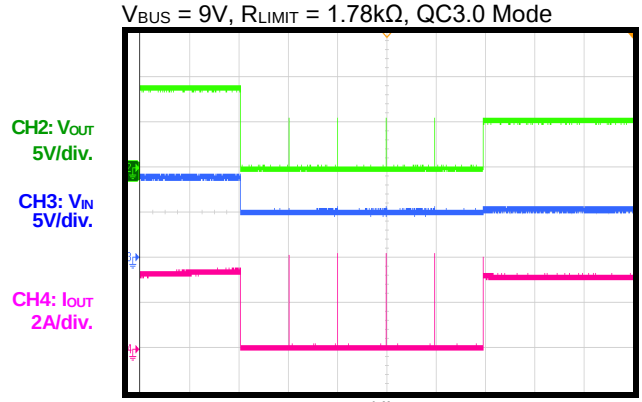
V_{IN} = 5V, R_{LIMIT} = 1.78kΩ



2s/div.

Over-Current Protection Entry and Recovery

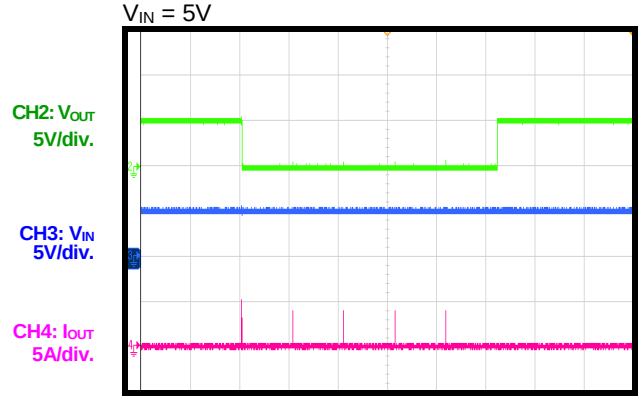
V_{BUS} = 9V, R_{LIMIT} = 1.78kΩ, QC3.0 Mode



2s/div.

Short-Circuit Protection Entry and Recovery

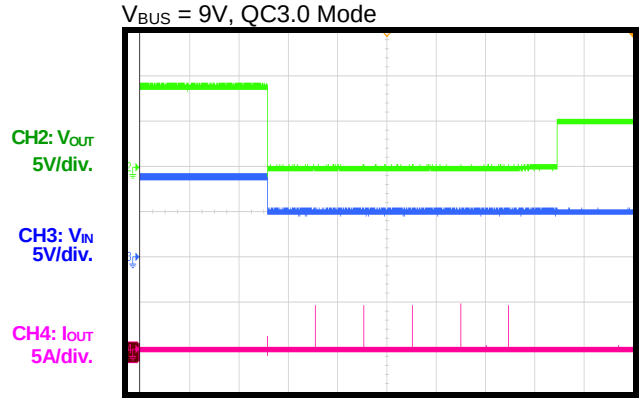
V_{IN} = 5V



2s/div.

Short-Circuit Protection Entry and Recovery

V_{BUS} = 9V, QC3.0 Mode



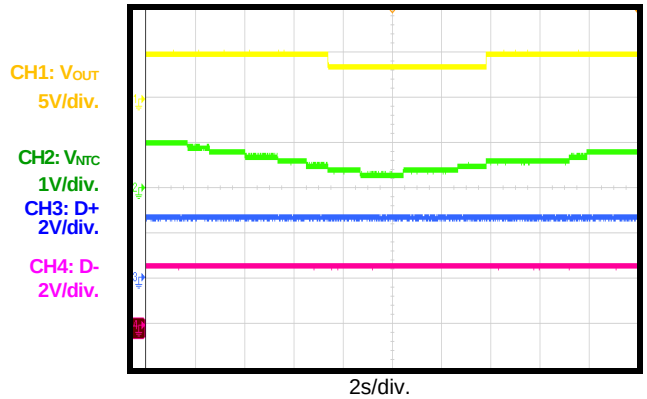
2s/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.78kΩ, T_A = 25°C, unless otherwise noted. Connect MPQ5029 input to MPQ4483 output, System_VIN = 14V is MPQ4483 input voltage.

NTC Entry and Recovery for 5V DCP Mode

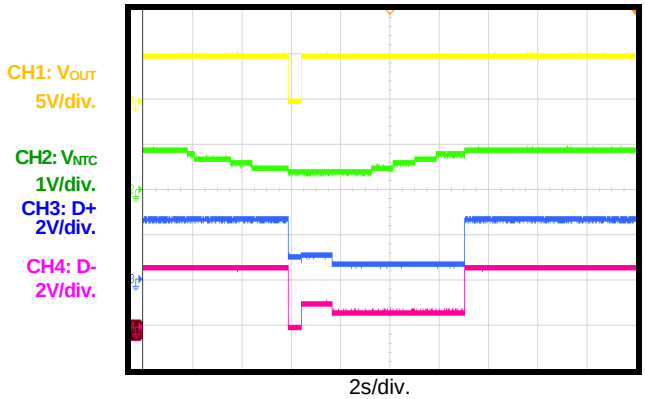
V_{IN} = 5V



2s/div.

NTC Entry and Recovery for DCP Mode w/ QC

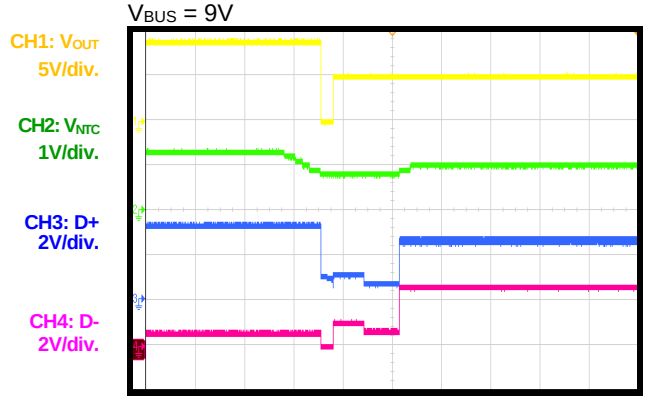
V_{IN} = 5V



2s/div.

NTC Entry and Recovery for DCP Mode w/ QC

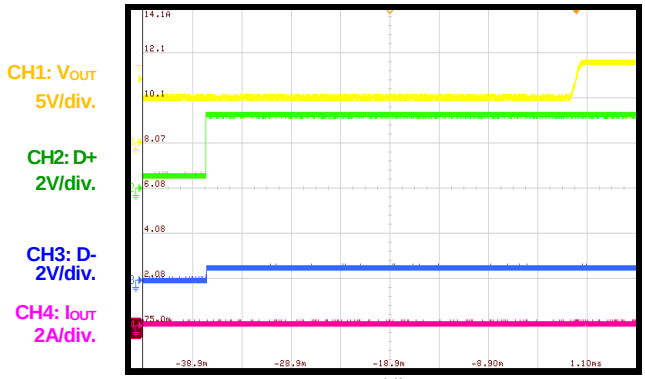
V_{BUS} = 9V



2s/div.

Mode Transition from 5V to 9V

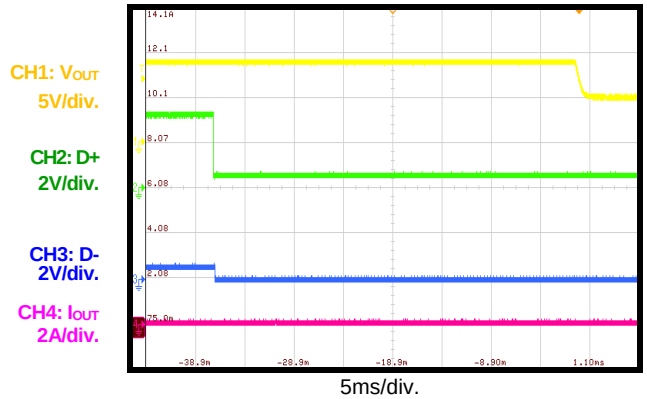
I_{OUT} = 0A, from QC 2.0, 5V to 9V



5ms/div.

Mode Transition from 9V to 5V

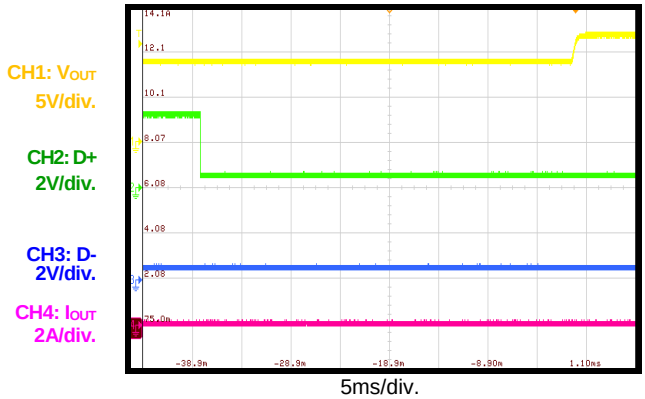
I_{OUT} = 0A, from QC 2.0, 9V to 5V



5ms/div.

Mode Transition from 9V to 12V

I_{OUT} = 0A, from QC 2.0, 9V to 12V



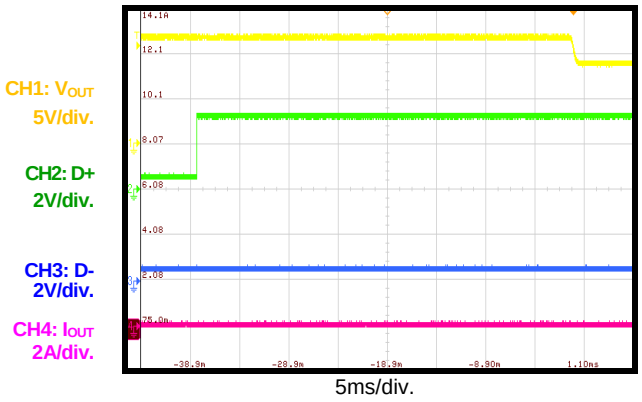
5ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

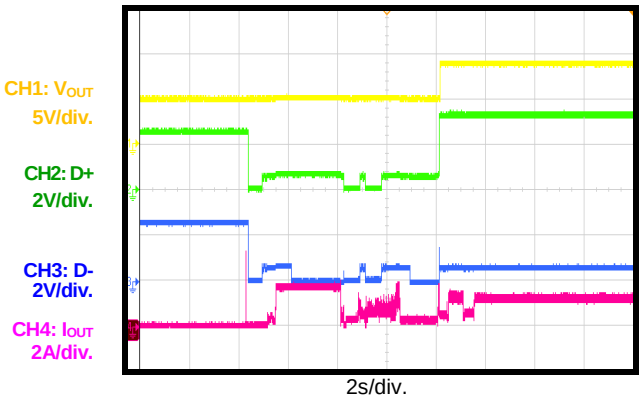
V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.78kΩ, T_A = 25°C, unless otherwise noted. Connect MPQ5029 input to MPQ4483 output, System_VIN = 14V is MPQ4483 input voltage.

Mode Transition from 12V to 9V

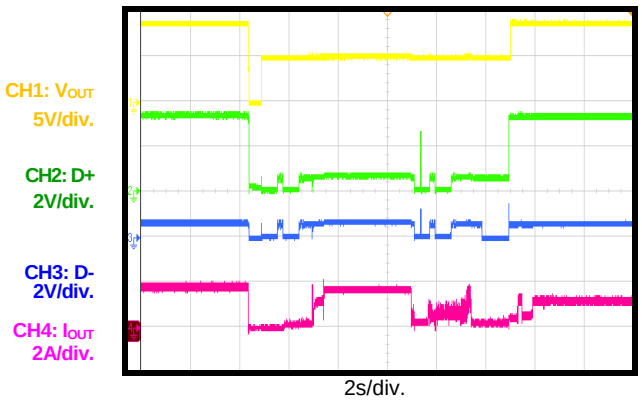
I_{OUT} = 0A, from QC 2.0, 12V to 9V



QC 3.0 Device Charging Test



QC 3.0 Device NTC Entry and Recovery



BLOCK DIAGRAM

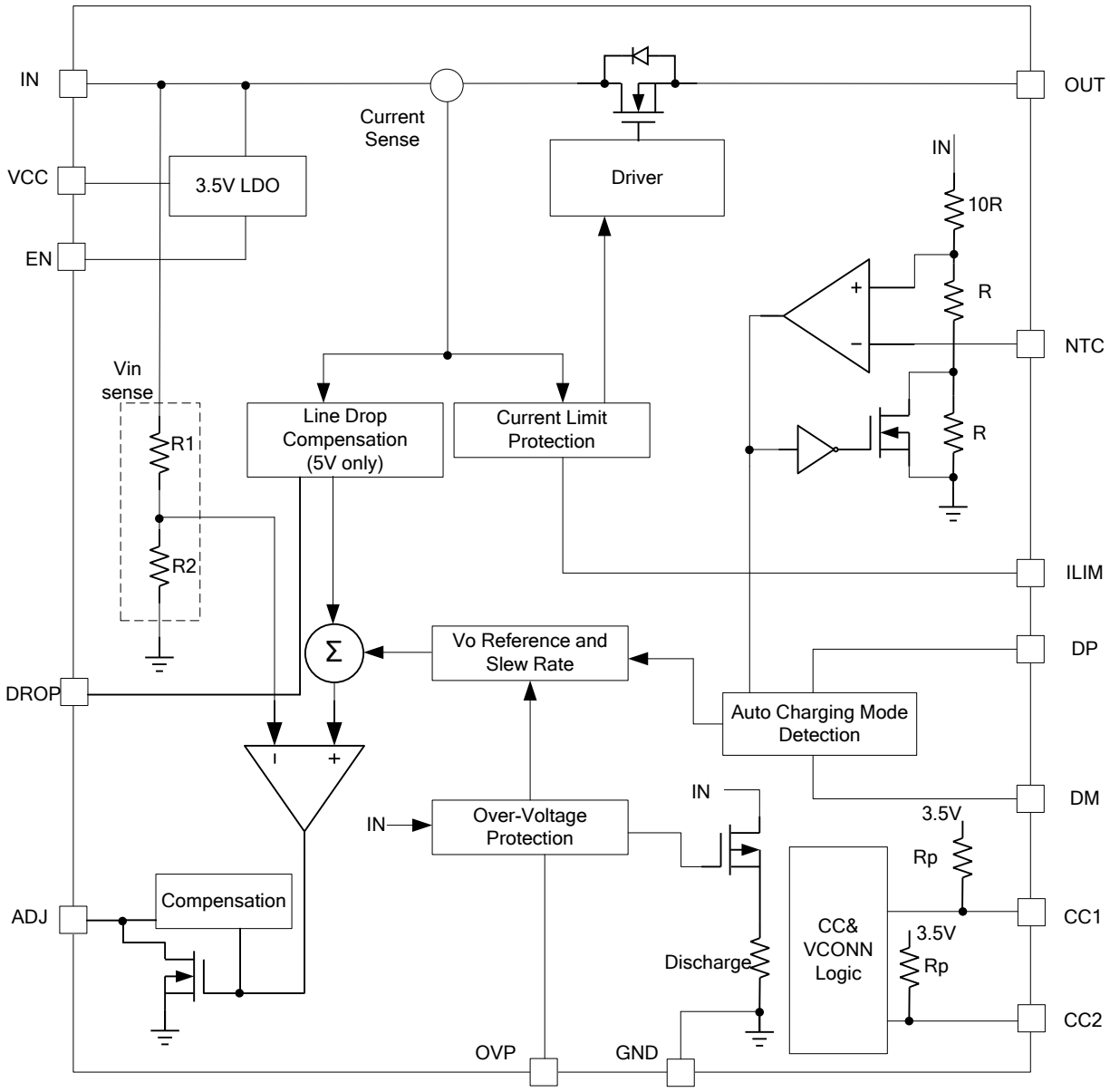


Figure 1: Functional Block Diagram

OPERATION

The MPQ5029 integrates a USB current-limit switch and charging port identification circuits. The MPQ5029 achieves 3A of continuous output current over a wide input supply range.

The output of the USB switch is current-limited with an adjustable current-limit threshold. The MPQ5029 supports the latest quick-charge specification (QC3.0) and is backwards compatible with QC2.0. The MPQ5029 also supports DCP schemes for battery charging specification (BC1.2), divider mode, and 1.2V/1.2V mode without the need for external user interaction.

The MPQ5029 also supports Type-C 5V @ 3A DFP mode.

The MPQ5029 provides line drop compensation for a 5V output. Full protection features include hiccup current limiting, input over-voltage protection (OVP), and thermal shutdown.

Operation Supply Voltage

The MPQ5029 has a two-stage input voltage threshold. The first threshold is around 2.4V, and the second threshold is the under-voltage lockout (UVLO) of the power MOSFET. When V_{IN} is higher than the first threshold, the MPQ5029's ADJ block turns on, which sinks a current to adjust the upstream regulator's output to an accurate 5.1V (typical). Afterward, the MPQ5029 can enable the power MOSFET so it can enter a fully working state.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPQ5029's second UVLO comparator monitors the input voltage. Once the input voltage is higher than the second UVLO threshold (around 2.85V), the power MOSFET starts to turn on at a controlled slew rate after a fixed delay.

Internal Soft Start (SS)

The internal soft start prevents inrush current and keeps the output voltage from overshooting during start-up.

Enable Control (EN)

The MPQ5029 has an enable control pin (EN). The MPQ5029 has an internal 6.5μA pull-up current that allows EN to be floated for auto-start-up. Pull EN high or float EN to enable the IC. Pull EN low to disable the IC.

QC Mode Voltage Transition - Class A

If the downstream device of the MPQ5029 supports a QC specification, the device can support output voltages higher than 5V via DM and DP communication. If a higher USB output voltage is required, use the ADJ pin. ADJ is connected to the feedback pin of the upstream voltage converter, typically. After the handshake, the MPQ5029 sinks a controlled ADJ current gradually to adjust V_{OUT} to 9V/12V or another voltage (i.e.: 200mV) step-by-step. Because of the MPQ5029's smart controller mode, only one ADJ pin is needed to set different high-voltage values and meet the QC specification. The output voltage transition is smooth with no undershoot or overshoot (see Figure 2 and Table 1).

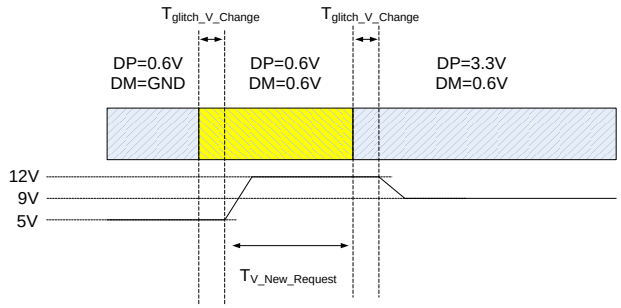


Figure 2: QC Mode Transition

Table 1: QC Mode Definition

Portable Device		USB Output Voltage
DP	DM	
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	3.6 - 12V/200mV step according to QC3.0
3.3V	3.3V	No action
0.6V	GND	5V

When the downstream device is removed, the output voltage returns to the default 5V automatically. The input-to-ground discharge resistor helps perform this procedure quickly.

Line Drop Compensation

The MPQ5029 is can compensate for an output voltage drop, such as high impedance caused by a long trace, to maintain a fairly constant 5V load-side voltage. The line drop compensation is active only at 5V V_{IN}. Line drop compensation is achieved through ADJ. The MPQ5029 increases the input voltage linearly vs. the output current. The R_{DROP} setting can refer to the line drop compensation vs. the R_{DROP} curve (see Figure 3).

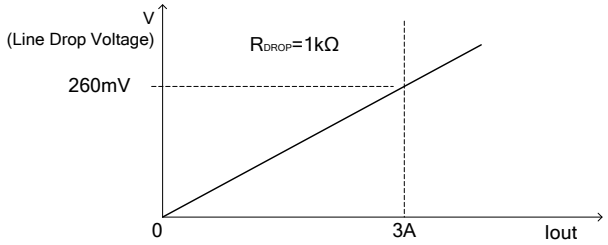


Figure 3: Line Drop Compensation

V_{OUT} with line drop compensation should be less than the OVP threshold.

The ADJ voltage (V_{ADJ}) sinks a controlled current slowly. The line drop compensation amplitude increases linearly as the load current increases.

In no-load condition, if the input voltage is lower than the typical 5.1V, ADJ sinks a current to regulate the upstream regulator's output voltage to 5.1V. If the input voltage is higher than 5.1V, the MPQ5029 no longer regulates the input voltage. For a quick load transient response, ADJ should always be working while the IC is on. Configure R1/R2 to let the default output voltage be less than 5.1V.

Figure 4 shows the typical ADJ usage. The ADJ sink current capability is 500μA. ADJ requires a feedback current through R1 less than 500μA. Calculate R1 with Equation (1):

$$R1(k\Omega) > \frac{\Delta V(V)}{0.5} \quad (1)$$

Where ΔV is the maximum line drop compensation value plus the difference in voltage between 5.1V and the buck voltage.

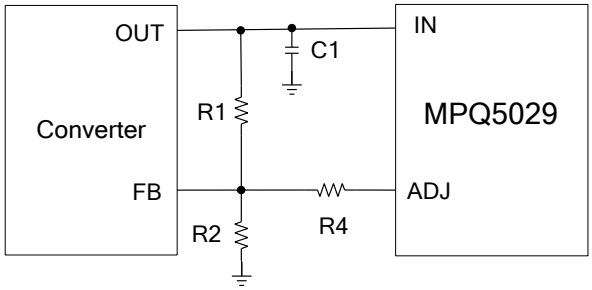


Figure 4: ADJ Configuration

There is another V_{ADJ} configuration to limit the maximum output voltage by inserting a resistor (R4) between FB and V_{ADJ}. With R4, the maximum output voltage can be limited by Equation (2):

$$V_{OUT\_Max}(V) = \frac{R_1 + R_2 // R_4}{R_2 // R_4} \times V_{FB}(V) \quad (2)$$

After adding R4, the maximum ADJ sink current is limited by Equation (3):

$$I_{ADJ\_Max}(\mu A) = \frac{V_{FB} - V_{OFFSET}(mV)}{R_4(k\Omega)} \quad (3)$$

Where V_{OFFSET} is about 100mV.

Input Over Voltage and Discharge

To protect the downstream device over-voltage, the MPQ5029 provides an input OVP discharge function. OVP has three states, which can be set by pulling OVP high, low, or by floating it. These modes can set the MPQ5029's OVP threshold and charging mode at the same time (see Table 2).

Table 2: Input OVP and Charging Mode Setting

OVP State	Charging Mode	OVP Threshold
Logic high	No QC3.0, DCP mode	OVP = 5.75V
Float	No QC3.0, DCP mode	No OVP
GND	QC3.0 and DCP	Automatic OVP

An accurate and fast comparator monitors the over-voltage condition of the input. If the input voltage rises above the threshold, the power MOSFET remains on, while the input-to-ground discharge path is active. When the input voltage falls below the typical 5.45V, the MPQ5029 exits OVP mode.

The input-to-ground discharge resistance is always active during the high-to-low voltage change mode. This resistance is disabled when FB is less than 108% x V_{REF} with a 20ms delay (OV is removed) (see Figure 5).

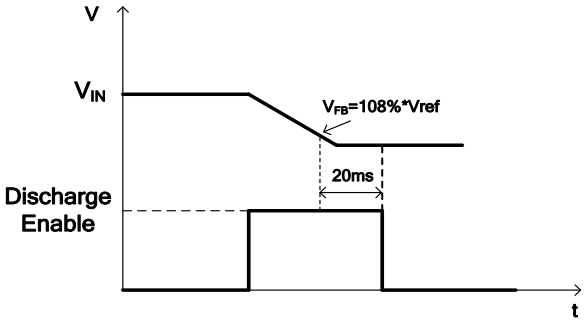


Figure 5: Input Discharge during High Voltage to Low Voltage Transition

QC mode is reset during the OVP rising edge.

Over-Current Protection (OCP)

The MPQ5029 provides a constant current limit. The current limit threshold is adjustable by an external resistor.

Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power MOSFET constant. If the over-current condition lasts longer than 2ms, the MPQ5029 enters hiccup mode.

The current limit setting for Type-A mode and Type-C mode can refer to the current limit vs. the R_{LIMIT} curve.

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit, the current may exceed the current-limit threshold greatly before the control loop can respond. If the current reaches an internal secondary current-limit level (about 6A), a fast turn-off circuit activates to turn off the power MOSFET. This limits the peak current through the switch to limit the input voltage drop. Afterward, the power MOSFET turns on again if the part is still in a short-circuit condition. The MPQ5029 treats this as an over-current condition and enters hiccup or thermal shutdown. After the short-circuit condition is removed, the MPQ5029 recovers automatically.

Note that the MPQ5029 can only support 9V/12V short-circuit protection (SCP) with QC mode and changes to 5.1V (typical) automatically when SCP is triggered.

Short-to-Battery Protection

The MPQ5029 provides CC1, CC2, DP, DM, and OUT short-to-battery protections when the IC is enabled.

The MPQ5029 has a high internal voltage rating. During a CC1/CC2 or DP/DM short-to-battery condition, the MPQ5029 can withstand high voltage on the internal components. Additionally, the ESD breakdown voltage is much larger than the battery voltage.

During a 5V USB output short-to-battery condition, the USB input rises up to trigger OVP. The USB input discharge path will turn on.

When the MPQ4483 is used as a buck regulator, the buck output capacitor should be placed between the buck output and PGND (instead of RGND) (see Figure 6).

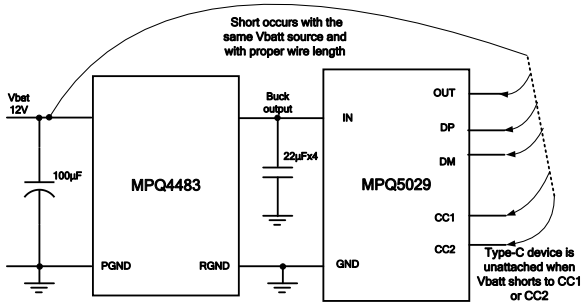


Figure 6: Short to Battery Setup

Negative Thermal Coefficient (NTC) Thermistor

The MPQ5029 has a built-in NTC comparator that allows the external device's temperature to be sensed via the thermistor mounted near the device. This ensures a safe operating environment and prevents any smoke or fire from occurring due to an over-temperature condition. Connect an appropriately valued resistor from IN to NTC, and connect the thermistor from NTC to GND. The resistor divider with a dividing ratio depends on the device temperature and determines the voltage on the NTC. When the NTC low threshold is triggered, the Type-C advised current rating changes from 3A to 1.5A.

If NTC is pulled low before V_{IN} start-up, the MPQ5029 enters Type-C 1.5A mode and DCP BC1.2 short mode directly without a V_{BUS} restart.

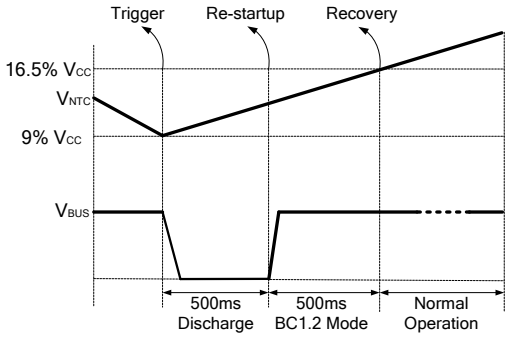
In QC mode, once the NTC voltage falls to 9% of VCC, V_{BUS} is discharged for 500ms, then starts up again with QC3.0 mode disabled.

The MPQ5029 remains at Type-C 1.5A mode, and the DP/DM protocol remains at BC1.2 short mode.

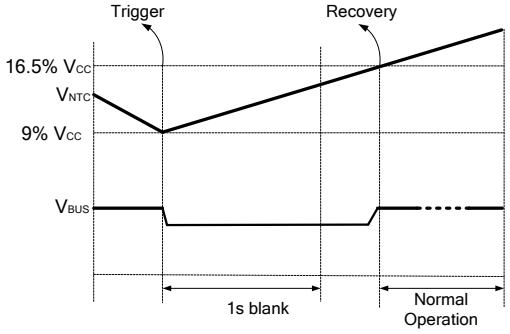
After 500ms, if the voltage rises to 16.5% of VCC, the MPQ5029 resumes normal operation (see Figure 7a).

In DCP mode, once the NTC voltage falls to 9% of VCC, the ADJ function is disabled, and the V_{BUS} changes to the buck regulator default output voltage.

After one second, if the NTC voltage rises to 16.5% of VCC, the MPQ5029 resumes normal operation (see Figure 7b).



a) 5V QC Mode



b) 5V DCP Mode

Figure 7: NTC Trigger and Recovery

Auto-Detection

The MPQ5029 integrates a USB-dedicated charging port auto-detect function that can recognize most mainstream portable devices and supports the following charging schemes:

- USB Battery Charging Specification BC1.2 / Chinese Telecommunications Industry
- Standard YD/T 1591-2009
- Divider mode
- 1.2V/1.2V mode
- Quick-Charge mode 3.0 and 2.0
- Type-C 5V @ 3A DFP mode, Type-C 5V @ 1.5A mode via NTC

USB Type-C Mode

For USB Type-C solutions, two pins on the connector, CC1 and CC2, are used to establish and manage the source-to-sink connection. The general concept for setting up a valid connection between a source and sink is based on being able to detect terminations residing in the product being attached. To aid in defining the functional behavior of CC, a pull-up (Rp) and pull-down (Rd 5.1kΩ) termination model is used based on a pull-up resistor and pull-down resistor (see Figure 8).

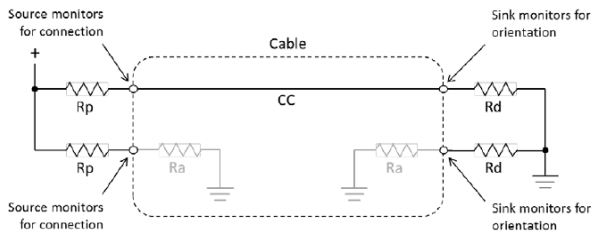


Figure 8: Current Source/Pull-Down CC Model

Initially, a source exposes independent Rp terminations on its CC1 and CC2 pins, and a sink exposes independent Rd terminations on its CC1 and CC2 pins. The source-to-sink combination of this circuit configuration represents a valid connection. To detect this, the source monitors CC1 and CC2 for a voltage lower than its unterminated voltage. The choice of Rp is a function of the pull-up termination voltage and the source's detection circuit. This indicates that either a sink, a powered cable, or a sink connected via a powered cable has been attached.

Two special termination combinations on the CC pins as seen by a source are defined for directly attached accessory modes: Ra/Ra for audio adapter accessory mode and Rd/Rd for debug accessory mode. In both cases, the MPQ5029's V_{OUT} is disabled.

When a Type-C device is unplugged, the output is discharged by a 200Ω resistor for 30ms. VCONN is discharged for 30ms, and then the discharge path is disabled.

Disable Type-C Mode (Type-A Mode)

During the MPQ5029 initial start-up, the IC sources 10μA for 20μs on CC1. If the CC1 voltage falls into the pre-set voltage range, the USB latches in Type-A mode unless the MPQ5029 is re-enabled. Type-C mode is disabled, which means the CC attach and detach logic is disabled, and the V_{BUS} is always enabled. The current limit changes to the Type-A spec.

To trigger this mode, the external pull-down resistor should be 90 - 100kΩ. Do not add an extra capacitor on CC1. In normal Type-C mode applications, a 1nF capacitor should be added on CC1 to avoid falsely triggering Type-A mode.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperature. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 125°C), the chip is enabled again.

APPLICATION INFORMATION

Selecting the Input Capacitor

Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. Ceramic capacitors 2.2 - 22μF in value are recommended for most applications.

When selecting an input capacitor, be sure to consider the pre-stage converter stability. The input capacitor of the MPQ5029 acts as the output capacitor of the converter. Ensure that the converter is stable with an additional output capacitor.

Selecting the Output Capacitor

Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended for their low ESR and small temperature coefficients. A 1μF ceramic capacitor is recommended for most applications.

Selecting ILIM Resistor

The current limit value can be set by an ILIM resistor. The programmable current limit can refer to the current limit vs. R_{LIMIT} curve.

The current-limit threshold should be 20% higher than the maximum load current. For example, if the system's full load is 3A, set the current limit to 3.55A.

Other Considerations

The upstream DC/DC converter should have a higher current-limit threshold than the MPQ5029's current limit.

ESD Protection for I/O Pins

Higher ESD levels should be considered for all USB I/O pins. The MPQ5029 features high ESD protection up to ±4kV human body model on the DP, DM, OUT, CC1, and CC2 pins. The ESD structures withstand high ESD in normal operation and when the device is powered off. To further extend DP and DM's ESD level for covering complicated application environments, additional resistors and capacitors can be added.

Similar R-C networks cannot be added on CC1 or CC2 since the CC line must be able to support 200mA of current and 300kHz of signaling. Additional ESD diodes can be added on the CC pins (see Figure 9).

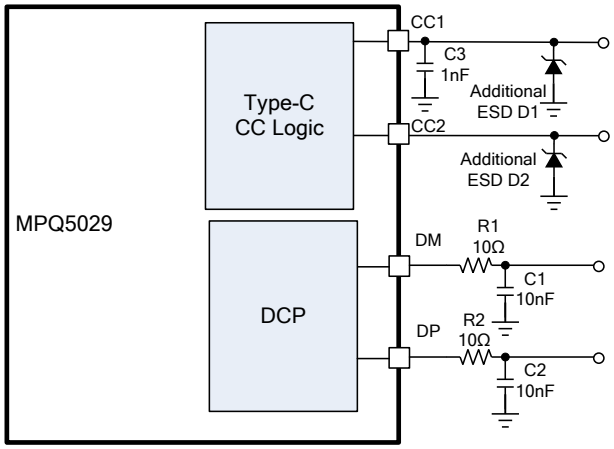


Figure 9: Recommended I/O Pins ESD Enhancing

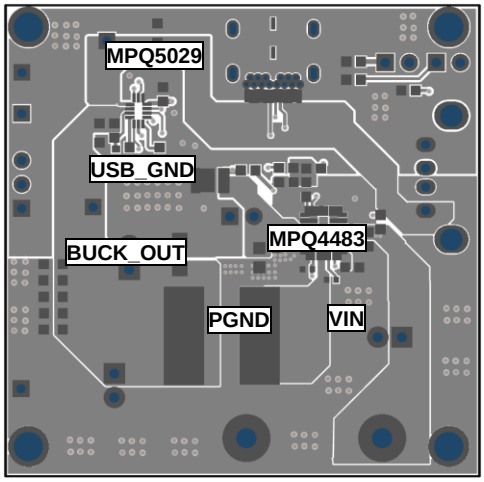
PCB Layout Guidelines [9]

Efficient PCB layout is critical for normal operation and thermal dissipation. For best results, refer to Figure 10 and follow the guidelines below.

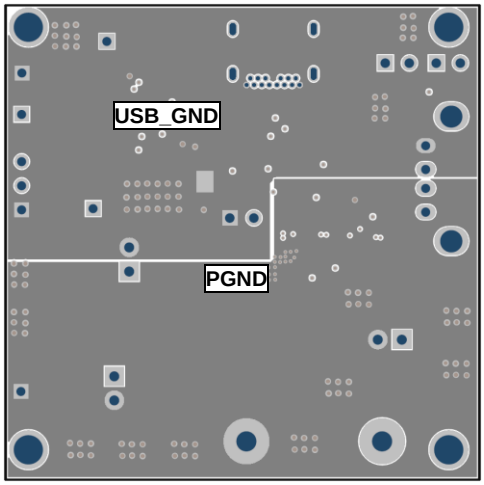
1. Use short, direct, and wide traces to connect the IC's IN/OUT pins.
2. Add vias under the IC.
3. Route the OUT trace on both PCB layers,
4. Place a ceramic input decoupling capacitor as close to IN and GND as possible to improve EMI performance.
5. Keep the V_{ADJ} trace to the pre-side converter FB pin as short as possible to prevent noise injection.

NOTE:

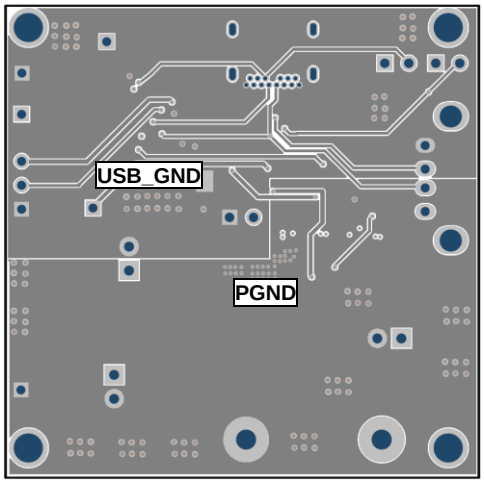
9) The recommended layout is based on the Typical Application Circuit shown in Figure 11 to Figure 14.



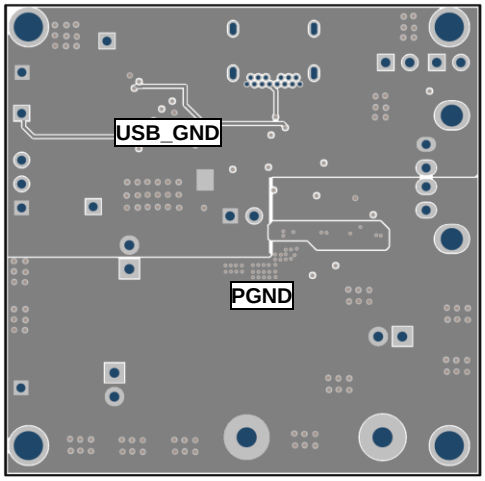
Top Layer



Middle Layer 1



Middle Layer 2



Bottom Layer

Figure 10: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

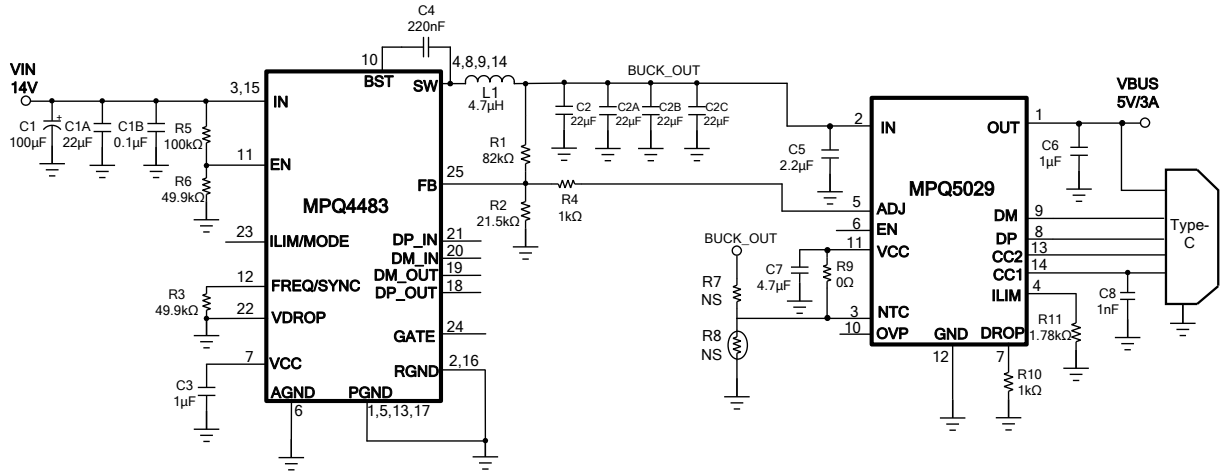


Figure 11: MPQ4483+MPQ5029 for Type-C Mode, DCP Mode without QC (without MPQ4483 GND Short-to-Battery Protection)

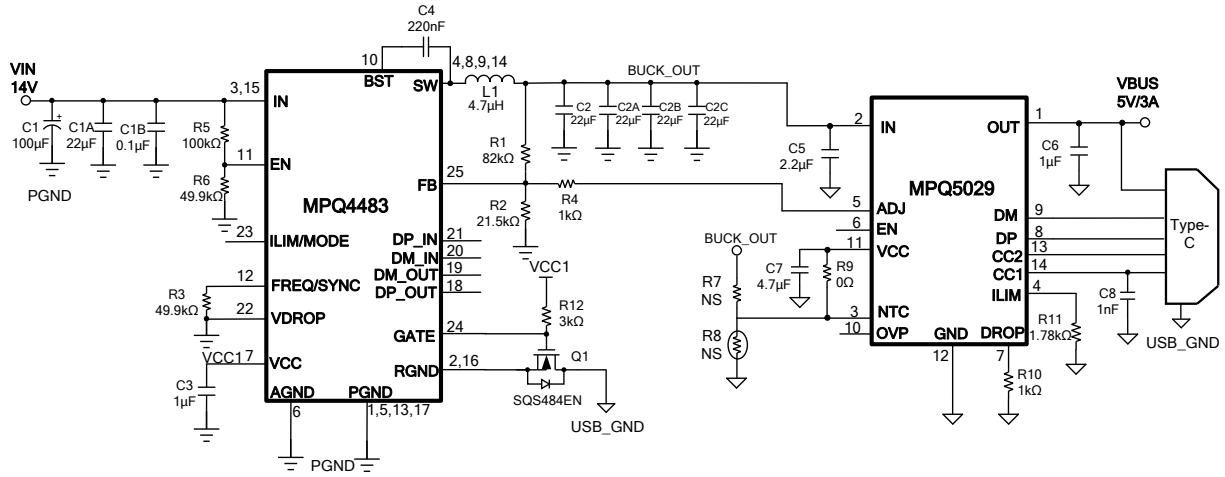


Figure 12: MPQ4483+MPQ5029 for Type-C Mode, DCP Mode without QC (with MPQ4483 GND Short-to-Battery Protection)

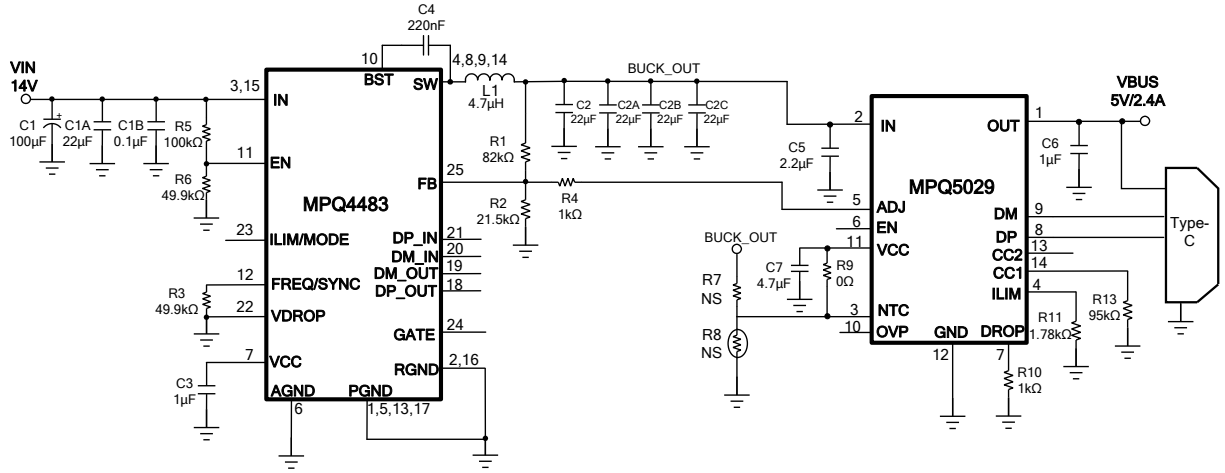


Figure 13: MPQ4483+MPQ5029 for Type-A mode, DCP Mode without QC (without MPQ4483 GND Short-to-Battery Protection)

TYPICAL APPLICATION CIRCUITS *(continued)*

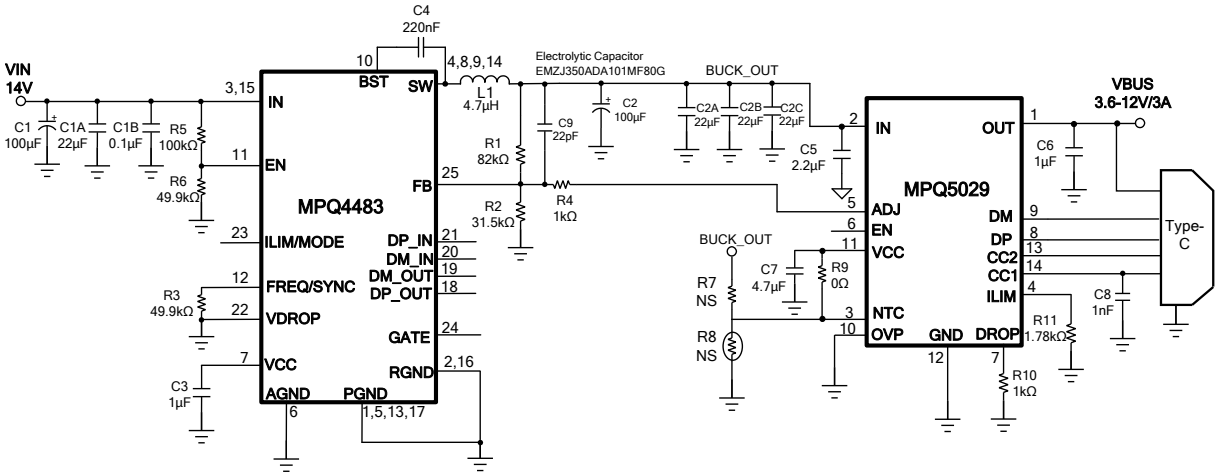
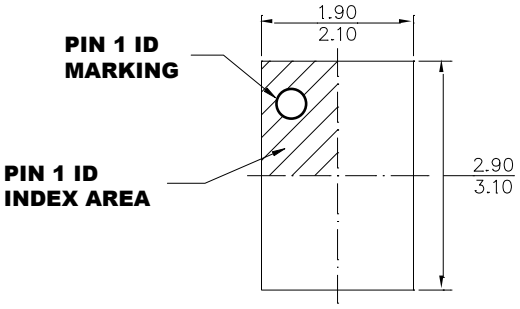


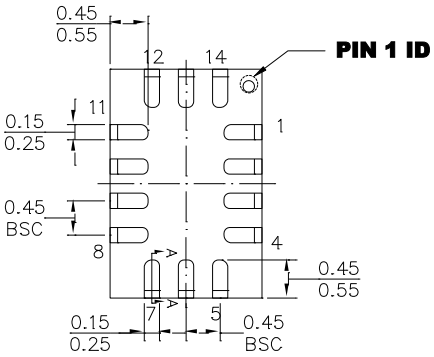
Figure 14: MPQ4483+MPQ5029 for Type-C Mode, DCP Mode w/ QC (without MPQ4483 GND Short-to-Battery Protection)

PACKAGE INFORMATION

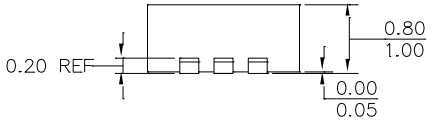
QFN-14 (2mmx3mm)



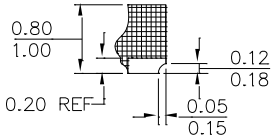
TOP VIEW



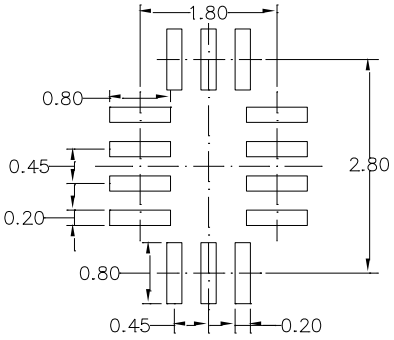
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.