钍地半导体
Tudi Semiconductor

Two-wire Serial EEPROM

256K (32,768 x 8)

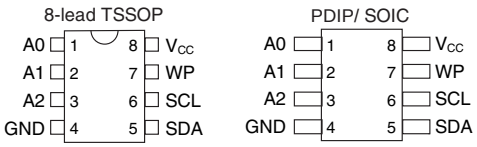
AT24C256
CAT24C256

Features

- **Internally Organized as 32,768 x 8**
- **Two-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **(5.0V, 2.7V, 2.5V), and 400 kHz (1.7V) Compatibility**
- **Write Protect Pin for Hardware and Software Data Protection**
- **64-byte Page Write Mode (Partial Page Writes Allowed)**
- **High Reliability**
  - **Endurance: One Million Write Cycles**
  - **Data Retention: 40 Years**
- **Lead-free/Halogen-free Devices Available**
- **8-lead JEDEC SOIC, 8-lead DIP, 8-lead TSSOP, and 8-ball Packages**
- **Low-voltage and Standard-voltage Operation**
  - **V_{cc} = 1.7V to 5.5V**

Description

AT24C256/CAT24C256 provides 262,144 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 32,768 words of 8 bits each. The device's cascadable feature allows up to eight devices to share a common two-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space-saving 8-lead JEDEC SOIC, 8-lead DIP, 8-lead TSSOP, and 8-ball packages. In addition, this device operates from 1.7V to 5.5V.



Pin Descriptions

Pin Name	Type	Functions
A0-A2	I	Address Inputs
SDA	I/O	Serial Data
SCL	I	Serial Clock Input
WP	I	Write Protect
GND	P	Ground
Vcc	P	Power Supply

Table 1

Examples

型号	封装	私印	工作电压	兼容电压
AT24C256C-SSHL-T-TUDI	SOP8	24C256	1.7-5.5	
CAT24C256WI-GT3-TUDI	SOP8	24256E	1.7-5.5	
AT24C256B-TH-T-TUDI	TSSOP8	24C256B	1.7-5.5	
AT24C256C-XHM-T-TUDI	TSSOP8	24C256C	1.7-5.5	2.7v
AT24C256-10PI-TUDI	DIP8	24C256	1.7-5.5	
CAT24C256LI-G-TUDI	DIP8	24C256LI	1.7-5.5	2.7v
CAT24C256YI-GT3-TUDI	TSSOP8	24C256	1.7-5.5	

Block Diagram

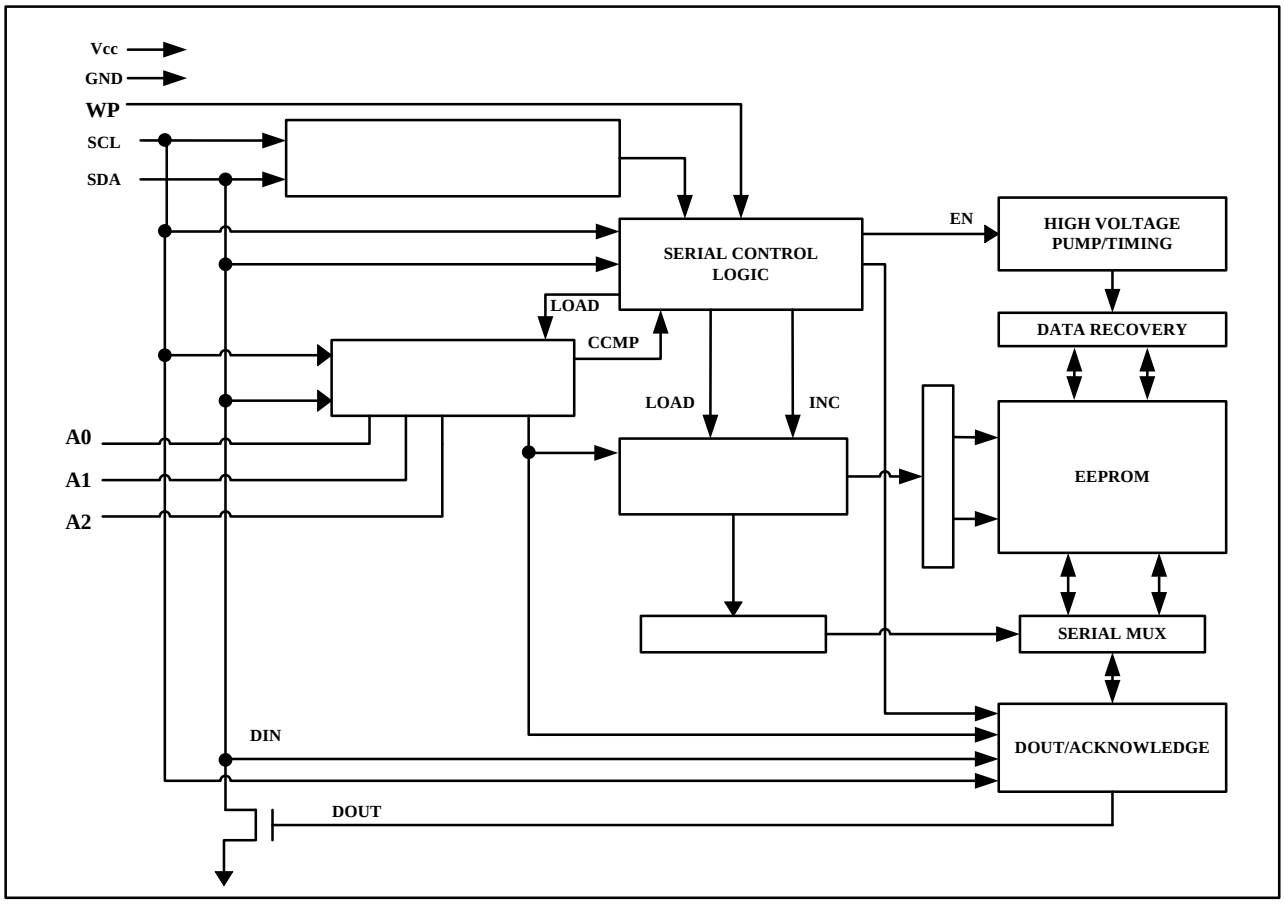


Figure 1

DEVICE/PAGE ADDRESSES (A2, A1 and A0): The A2, A1 and A0 pins are device address inputs that are hard wire for the AT24C256 . Eight 256K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

WRITE PROTECT (WP): The AT24C256 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protection pin is connected to Vcc, the write protection feature is enabled and operates as shown in the following **Table 2**.

WP Pin Status	AT24C256
At VCC	Full(256K)Array
At GND	Normal Read/Write Operations

Table 2

Functional Description

1. Memory Organization

AT24C256 , 256K SERIAL EEPROM: Internally organized with 256 pages of 64 bytes each, the 256K requires a 15-bit data word address for random word addressing.

2. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see **Figure 2**). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see **Figure 3**).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see **Figure 3**).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT24C256 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.

2. Look for SDA high in each cycle while SCL is high.

3. Create a start condition.

(32768×8)**Figure 2. Data**

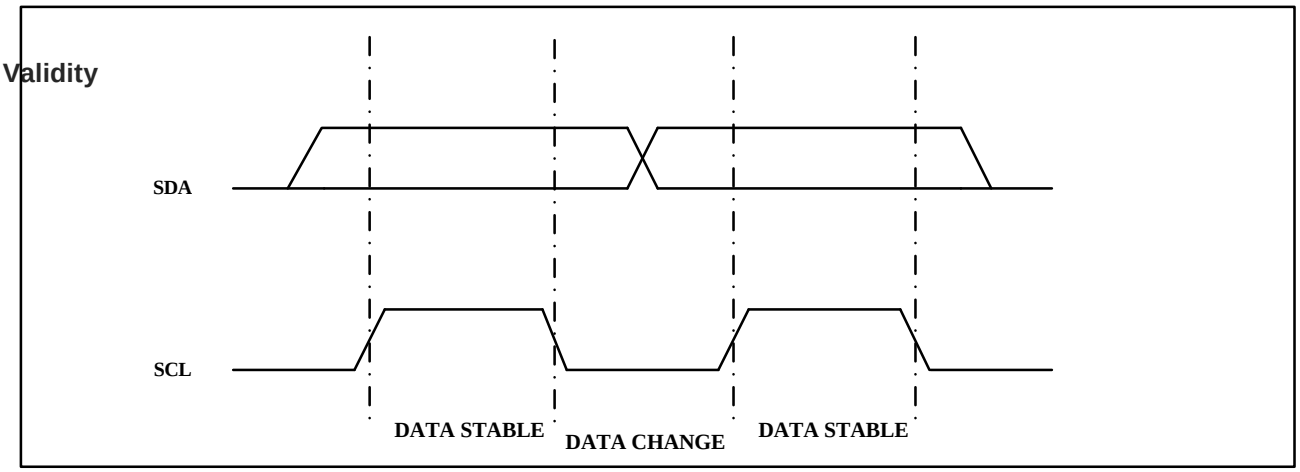


Figure 3. Start and Stop Definition

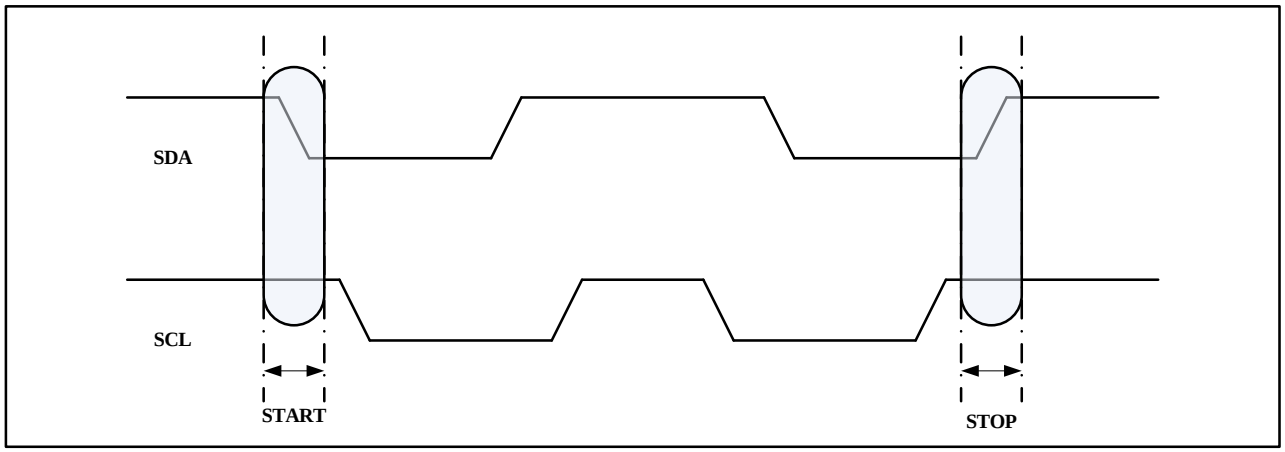
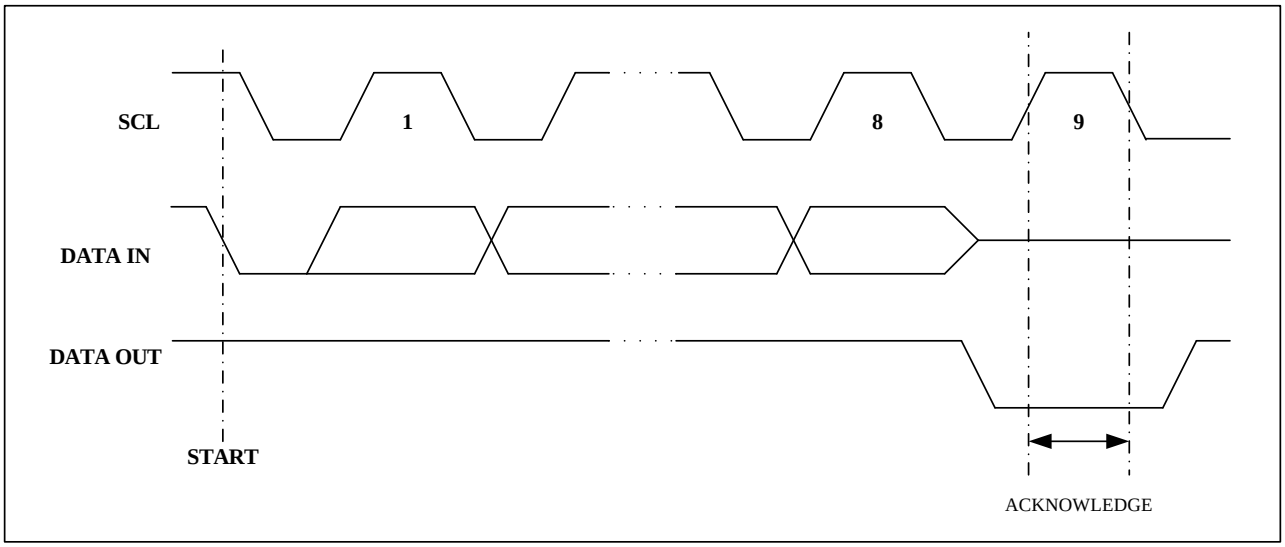


Figure 4. Output Acknowledge



3. Device Addressing

The 256K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see **Figure 5**)

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 256K EEPROM uses A2, A1 and A0 device address bits to allow as much as eight devices on the same bus. These 3 bits must be compared to their corresponding hardwired input pins. The A2, A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

DATA SECURITY: The AT24C256 has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at VCC.

4. Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see **Figure 6**).

PAGE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see **Figure 7**).

The data word address lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

WRITE IDENTIFICATION PAGE:The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write

Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- MSB address bits B15/B6 are don't care except for address bit B10 which must be "0".

LSB address bits B5/B0 define the byte address inside the Identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

5. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ:

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see **Figure 8**).

RANDOM READ:

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 9**)

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the

microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 10**).

READ IDENTIFICATION PAGE: The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

The Identification Page can be read by issuing an Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits B15/B6 are don't care, the LSB address bits B5/B0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g.: when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 22, as the ID page boundary is 64 bytes)

LOCK IDENTIFICATION PAGE: The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

Device type identifier = 1011b

Address bit B10 must be ‘1’ ; all other address bits are don't care

The data byte must be equal to the binary value xxxx xx1x, where x is don't care

Table 3. FIRST WORD ADDRESS

B15	B14	B13	B12	B11	B10	B9	B8

Table 4. SECOND WORD ADDRESS

B7	B6	B5	B4	B3	B2	B1	B0

Figure 5. Device Address

MSB							LSB
1	0	1	0	A2	A1	A0	R/W

Figure 6. Byte Write

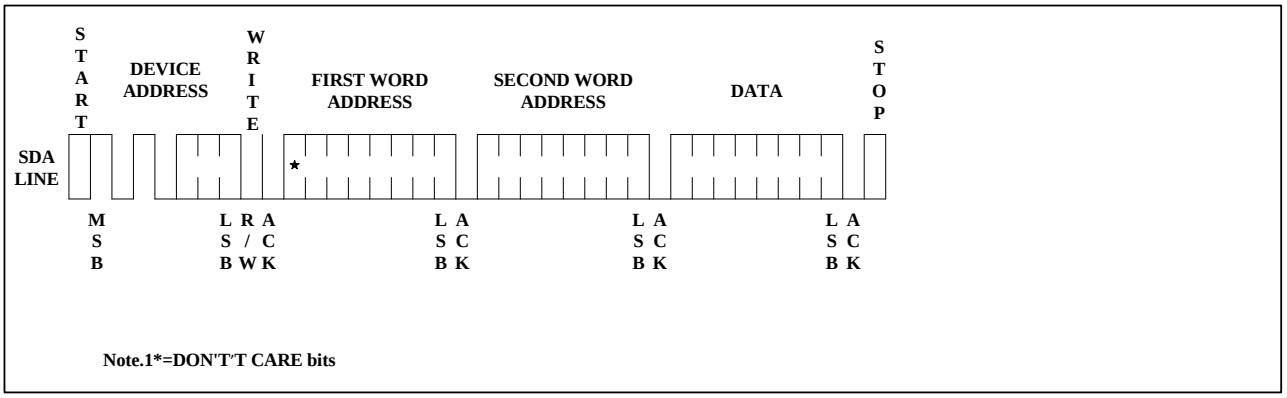


Figure 7. Page Write

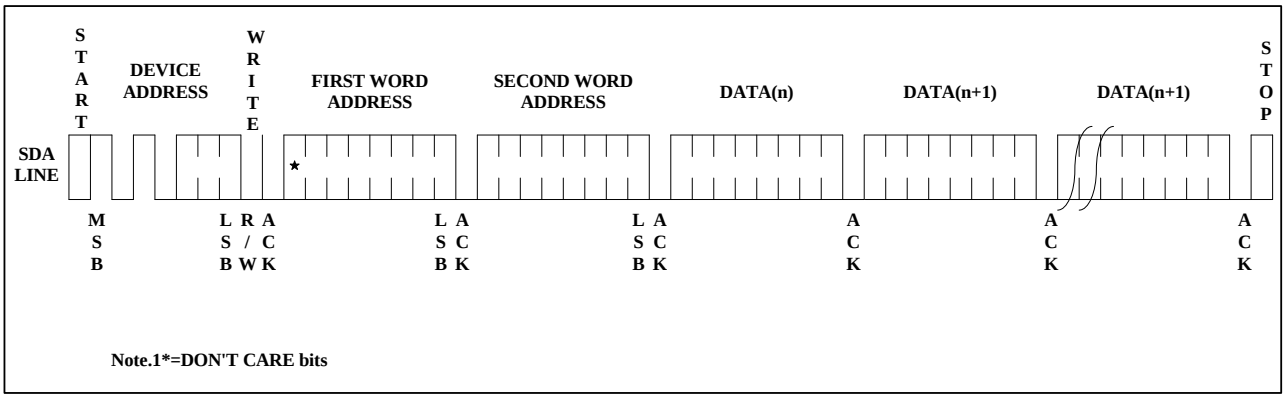


Figure 8. Current Address Read

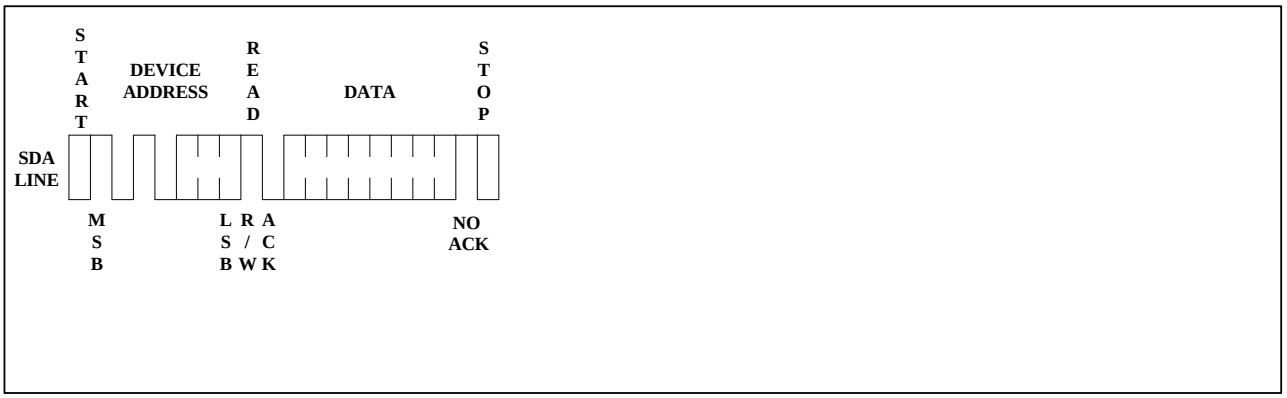


Figure 9. Random Read

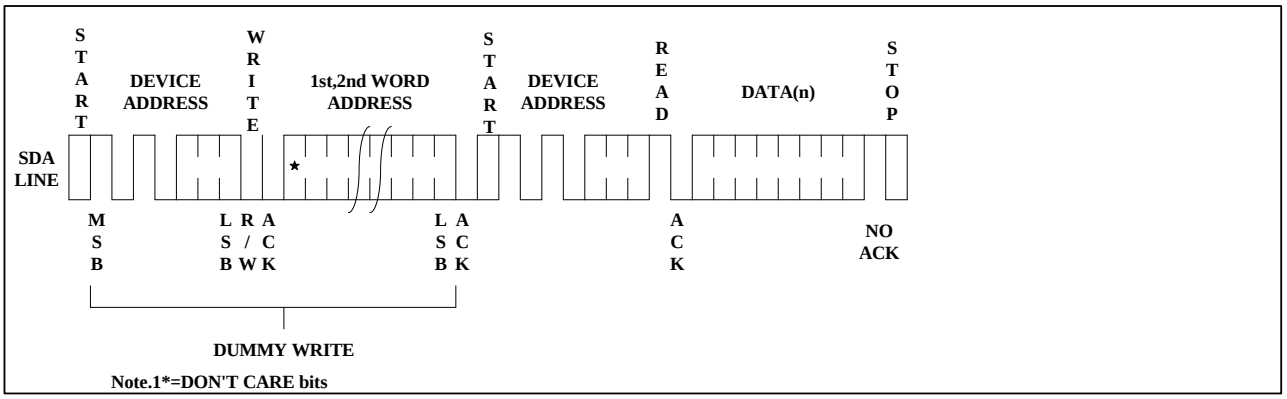
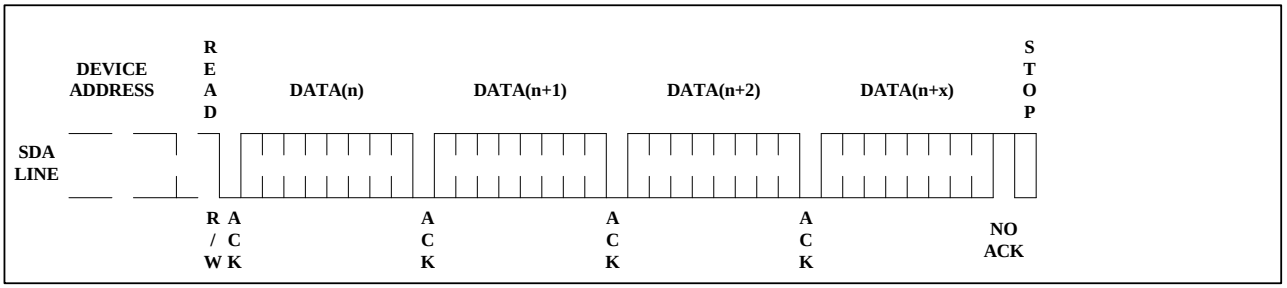


Figure 10. Sequential Read



Electrical Characteristics

Absolute Maximum Stress Ratings：

- DC Supply Voltage . . . . . .-0.3V to +6.5V
- Input / Output Voltage . . . . . .GND-0.3V to VCC+0.3V
- Operating Ambient Temperature . . . . . -40℃ to +85℃
- Storage Temperature . . . . . -65℃ to +150℃
- Electrostatic pulse (Human Body model) 8000V

Comments：

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Applicable over recommended operating range from: TA = -40℃ to +85℃, VCC = +1.7V to +5.5V (unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	V_{CC1}	1.7	-	5.5	V	-
Supply Voltage	V_{CC2}	2.5	-	5.5	V	-
Supply Voltage	V_{CC3}	2.7	-	5.5	V	-
Supply Voltage	V_{CC4}	4.5	-	5.5	V	-
Supply Current VCC=5.0V	I_{CC1}	-	0.4	1.0	mA	READ at 400KHZ
Supply Current VCC=5.0V	I_{CC2}	-	2.0	3.0	mA	WRITE at 400KHZ
Supply Current VCC=1.7V	I_{SB1}	-	0.6	1.0	μA	$V_{IN}=V_{CC}$ or V_{SS}
Supply Current VCC=2.5V	I_{SB2}	-	1.0	2.0	μA	$V_{IN}=V_{CC}$ or V_{SS}
Supply Current VCC=2.7V	I_{SB3}	-	1.0	2.0	μA	$V_{IN}=V_{CC}$ or V_{SS}
Supply Current VCC=5.0V	I_{SB4}	-	2.0	5.0	μA	$V_{IN}=V_{CC}$ or V_{SS}
Input Leakage Current	I_{L1}	-	0.10	3.0	μA	$V_{IN}=V_{CC}$ or V_{SS}
Output Leakage Current	I_{LO}	-	0.05	3.0	μA	$V_{OUT}=V_{CC}$ or V_{SS}
Input Low Level	V_{IL1}	-0.3	-	V_{CC}×0.3	V	V_{CC}=1.8V to 5.5V
Input High Level	V_{IH1}	V_{CC}×0.7	-	V_{CC}+0.3	V	V_{CC}=1.8V to 5.5V
Input Low Level	V_{IL2}	-0.3	-	V_{CC}×0.2	V	V_{CC}=1.7V
Input High Level	V_{IH2}	V_{CC}×0.7	-	V_{CC}+0.3	V	V_{CC}=1.7V
Output Low Level VCC=5.0V	V_{OL3}	-	-	0.4	V	I_{OL}=3.0mA
Output Low Level VCC=3.0V	V_{OL2}	-	-	0.4	V	I_{OL}=2.1mA
Output Low Level VCC=1.7V	V_{OL1}	-	-	0.2	V	I_{OL}=0.15mA

Table 5

Pin Capacitance

Applicable over recommended operating range from TA = 25℃, f = 1.0 MHz, VCC = +1.7V

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input/Output Capacitance(SDA)	$C_{I/O}$	-	-	8	pF	V_{IO}=0V
Input Capacitance(A0,A1,A2,SCL)	C_{IN}	-	-	6	pF	V_{IN}=0V

Table 6

AC Electrical Characteristics

Applicable over recommended operating range from TA = -40℃ to +85℃, VCC = +1.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Parameter	Symbol	1.7V≤Vcc＜2.5V			2.5V≤Vcc＜5.5V			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Frequency,SCL	f_{SCL}	-	-	400	-	-	1000	KHZ
Clock Pulse Width Low	t_{LOW}	1.2	-	-	0.6	-	-	μs
Clock Pulse Width High	t_{HIGH}	0.6	-	-	0.4	-	-	μs
Noise Suppression Time	t_I	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	t_{AA}	0.1	-	0.9	0.05	-	0.9	μs
Time the bus must be free before a new transmission can start	t_{BUF}	1.2	-	-	0.5	-	-	μs
Start Hold Time	$t_{HD:STA}$	0.6	-	-	0.25	-	-	μs
Start Setup Time	$t_{SU:DAT}$	0.6	-	-	0.25	-	-	μs
Data In Hold Time	$t_{HD:DAT}$	0	-	-	0	-	-	μs
Data in Setup Time	$t_{SU:DAT}$	100	-	-	100	-	-	ns
Input Rise Time(1)	t_R	-	-	0.3	-	-	0.3	μs
Input Fall Time(1)	t_F	-	-	300	-	-	300	μs
Stop Setup Time	$t_{Su:STO}$	0.6	-	-	0.25	-	-	μs
Data Out Hold Time	t_{DH}	50	-	-	50	-	-	ns
Write Cycle Time	t_{WR}	-	3.3	5	-	3.3	5	ms
5.0V,25℃,Byte Mode(1)	Endurance	1M	-	-	-	-	-	Write Cycle

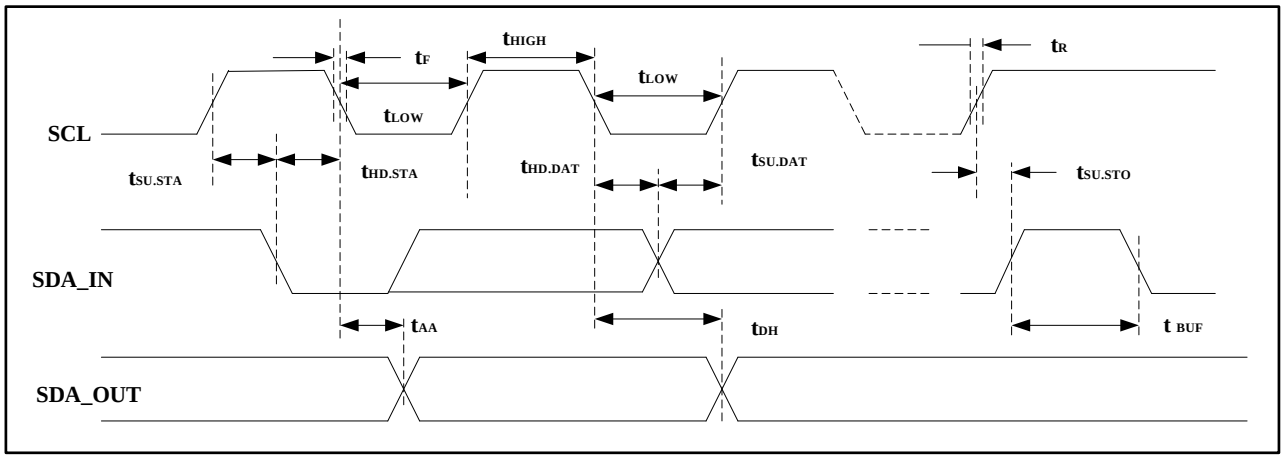
Table 7

Notes:

1. This parameter is characterized and is not 100% tested.
2. AC measurement conditions:
   RL (connects to VCC): 1.3 k
   Input pulse voltages: 0.3 VCC to 0.7 VCC
   Input rise and fall time: 50 ns
   Input and output timing reference voltages: 0.5 VCC
   The value of RL should be concerned according to the actual loading on the user's system.

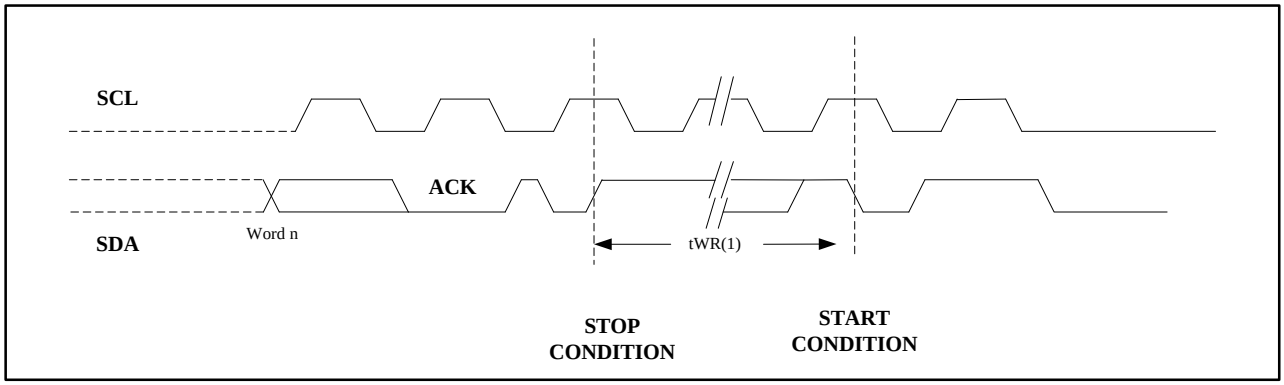
Bus Timing

Figure 11. SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

Figure 12. SCL: Serial Clock, SDA: Serial Data I/O

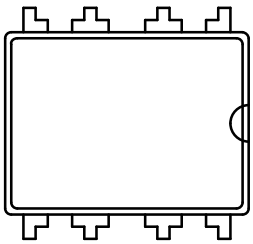


Notes:

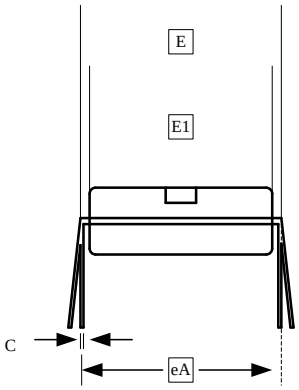
The write cycle time tWR is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Package Information

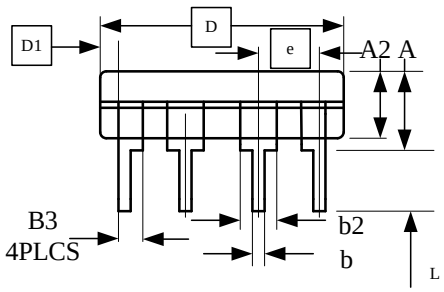
PDIP Outline Dimensions



Top View



End View



Side View

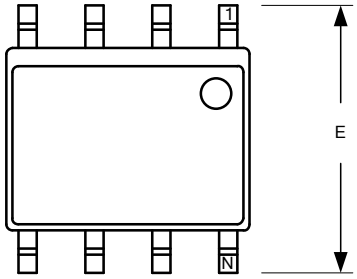
COMMON DIMENSIONS
(Unit of Measure=inches)

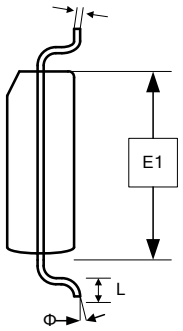
SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100BSC			
eA	0.300BSC			4
L	0.115	0.130	0.150	2

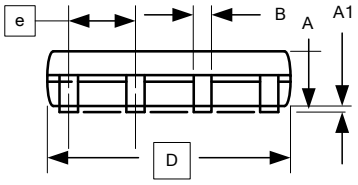
Notes:

1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

SOP



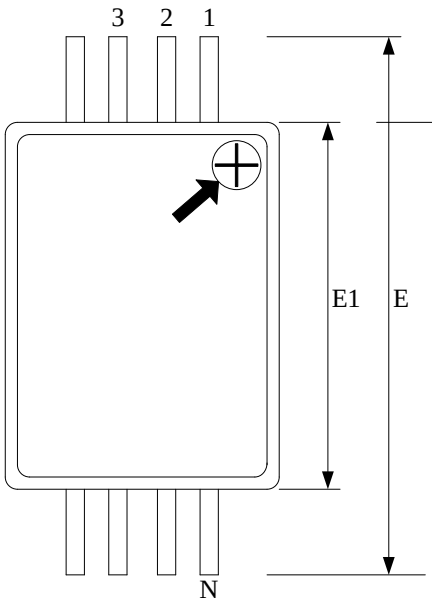




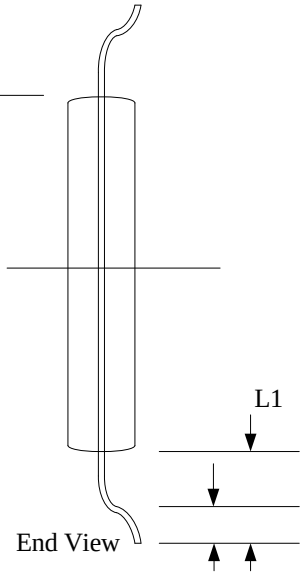
COMMON DIMENSIONS
(Unit of Measure=mm)

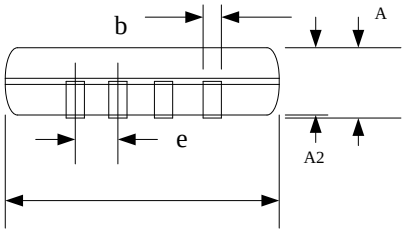
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	-	1.75	
A1	0.10	-	0.25	
b	0.31	-	0.51	
C	0.17	-	0.25	
D	4.80	-	5.00	
E1	3.81	-	3.99	
E	5.79	-	6.20	
e	1.27BSC			
L	0.40	-	1.27	
Φ	0°	-	8°	

TSSOP



Top View





Side View

COMMON DIMENSIONS
Unit of Measure=mm

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2,5
E		6.40BSC		
E1	4.30	4.40	4.50	3,5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65BSC		
L	0.45	0.60	0.75	
L1		1.00REF		