TS01S

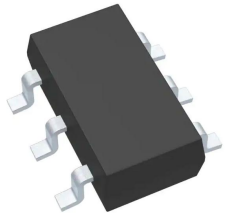
1-CH Differential Sensitivity Calibration Capacitive Touch Sensor

General Description

The TS01S is a single channel capacitive touch control switch IC can replace traditional mechanical switches.

The TS01S is fabricated by CMOS process, with simple structure and stable performance.

TS01S is available in the SOT23-6 package.



SOT23-6

Features

- 1-Channel capacitive touch sensor with differential sensitivity calibration
- Uniformly adjustable sensitivity
- Three steps sensitivity available without external component
- Sync function for parallel operation
- Low current consumption
- Embedded common and normal noise elimination circuit
- Open-drain digital output
- Internal power on reset

Package Information

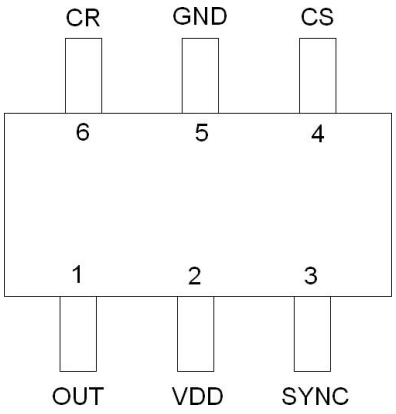
Part NO.	Package Description	Package Marking	Package Option
TS01S	SOT23-6	.SXXX	3000/Reel

S：Part NO. TS01S XXX: LOT NO.

Applications

- Home appliance
- Membrane switch replacement
- Sealed control panels, keypads
- Human interface for toys & interactive games
- Mobile application (PMP, Navigation, MP3 etc)

Pin Configuration



TS01S(SOT23-6)

Pin Descriptions

Pin No.	Name	Function Description	I/O	Protection
1	OUT	Touch detect output	Digital Output	VDD/GND
2	VDD	Power (2.5V ~ 5.0V)	Power	GND
3	SYNC	Self operation signal output Peripheral operation signal input Sensitivity selection input [Note1]	Analog Input / Output	VDD/GND
4	CS	Capacitive sensor input	Analog Input	VDD/GND
5	GND	Supply ground	Ground	VDD
6	CR	Reference capacitive sensor input for differential sensitivity calibration	Analog Input	VDD/GND

Note1 : Refer to chapter 6.4 SYNC implementation for sensitivity selection.

Absolute Maximum Ratings

Parameter Name	Symbol	Value	Unit
Supply Voltage	VDD	5.5	V
Maximum Voltage on Any Pin	I/O	VDD+0.3	V
Continuous Power Dissipation	Po	200	mW
Storage Temperature	Tst	-50 ~ 150	℃
Operating Temperature	Top	-20 ~ 75	℃
Junction Temperature	Tj	150	℃

Note2 : Unless any other command is noted, all above are operated in normal temperature.

ESD & Latch-up Characteristics

ESD Characteristics

Mode	Polarity	Minimum Level	Reference
H.B.M	Positive/Negative	2000V	VDD
		2000V	VSS
		2000V	P to P
M.M	Positive/Negative	200V	VDD
		200V	VSS
		200V	P to P

Latch-up Characteristics

Mode	Polarity	Minimum Level	Test Step
I Test	Positive	200mA	25mA
	Negative	-200mA	
V Supply Over 5.0V	Positive	8.0V	1.0V

Electrical Characteristics (unless otherwise specified: VDD=3.3V, Ta=25°C)

Parameter Name	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Supply Voltage	V_{DD}		2.5	3.3	5.0	V
Current Consumption	I_{DD}	V_{DD} =3.3V		25	40	μA
		V_{DD} =5.0V		40	70	μA
Output Maximum Sink Current	I_{OUT}	Ta=25°C			4.0	mA
Internal Reset Criterion V_{DD} Voltage	V_{DD_RST}	Ta=25°C			0.3 *V_{DD}	V
Sense Input Capacitance Range [Note3]	C_S			10	100	pF
Reference Input Capacitance Range [Note4]	C_R			12	100	pF
Sense Input Resistance Range	R_S			200	1000	Ω
Minimum Detectable Capacitance Variation	ΔC_S	C_S =10pF	0.2			pF
Output Impedance (Open Drain)	Z_O	ΔC_S >0.2pF		12		Ω
		ΔC_S <0.2pF		30		MΩ
Self Calibration time after V_{DD} Setting	T_{CAL}			200		ms
Maximum Supply Voltage Rising Time	T_{R_VDD}				100	ms
Recommended Sync Resistance Range	R_{SYNC}		1	2	20	MΩ

Note 3: The sensitivity can be increased with lower C_S value.

The recommended value of C_S is 10pF when using 3T PC (Poly Carbonate) cover and 10mm x 7mm touch pattern and middle normal(middle) sensitivity selection.

Note 4: C_R value is recommended as same that of C_{S_TOT} as possible for effective differential Sensitivity calibration.

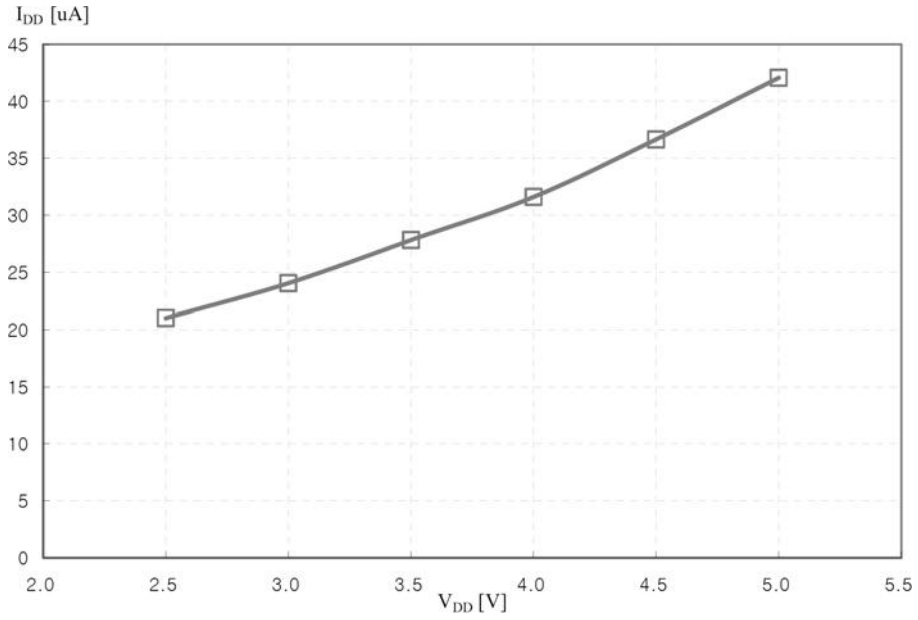
$C_{S\_TOT} = C_S + C_{PARA}$ (C_{PARA} is parasitic capacitance of CS pin)

If proper CR capacitor value is used, CR pin has almost same frequency as that of CS pin.

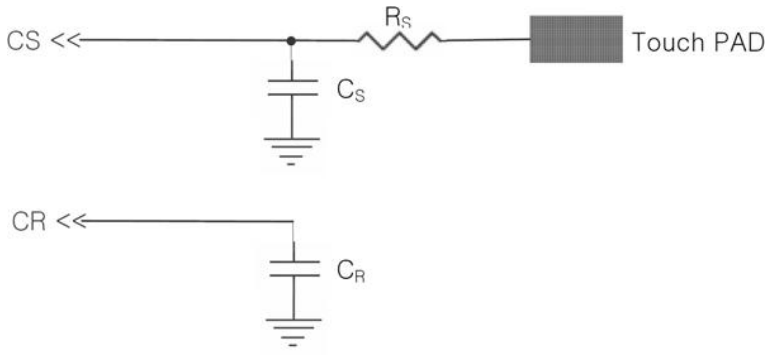
Application Summary

Current consumption

TS01S uses internal bias circuit, so internal clock frequency and current consumption is not adjusted. Only the VDD voltage affects internal clock frequency and current consumption. The current consumption curve of TS01S is represented in accordance with VDD voltage as below. The higher VDD requires more current consumption.
Internal clock frequency deviation is within ±20% range from typical value.
Internal bias circuit can make the circuit design simple and reduce external components.

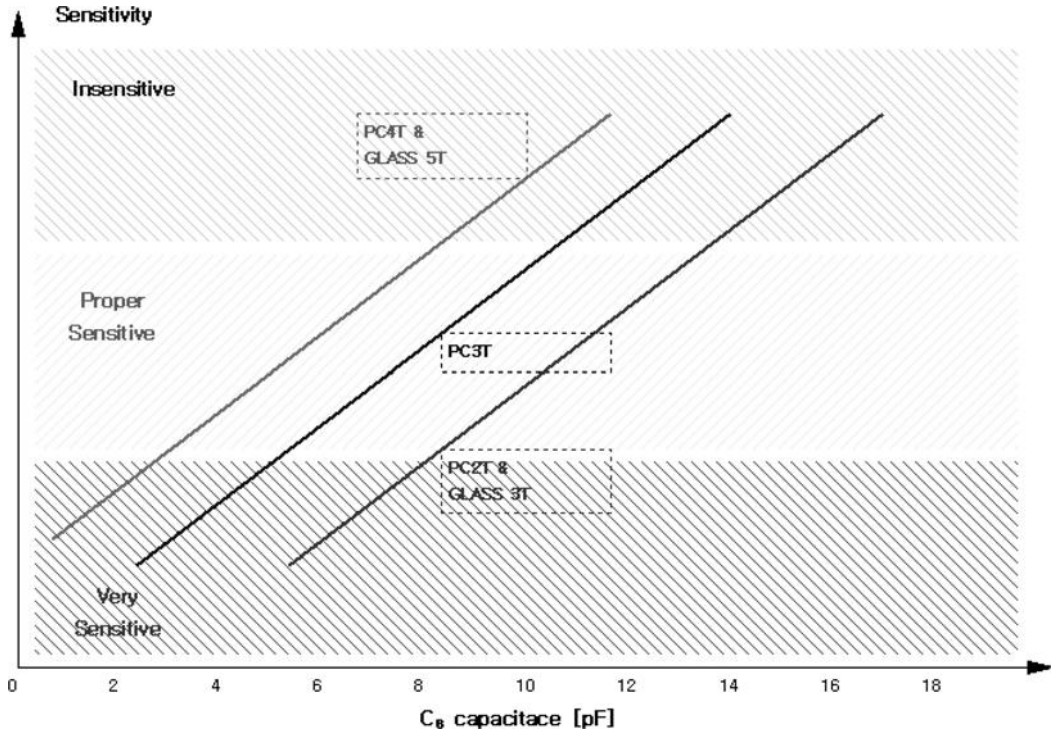


CS and CR Implementation



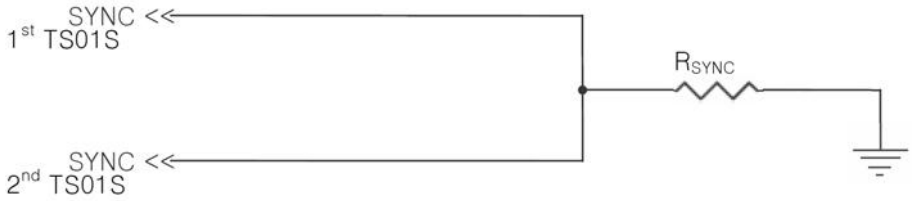
The parallel capacitor C_S is added to CS and C_R to CR to adjust the sensitivity. The major factor of the sensitivity is C_S. The sensitivity would be increased when smaller C_S value is used. (Ref. below Sensitivity Example Figure) The C_R value should be almost the same as the total CS capacitance (C_{S_TOT}) for effective differential sensitivity calibration. The total CS capacitance is composed of C_S which is set for optimal sensitivity and parasitic capacitance of CS pattern (C_{PARA}). The parasitic capacitance of CS pattern is about 2pF if normal touch pattern size is used. But in the case of using larger touch pattern, C_{PARA} is bigger than normal value. The RS is serial connection resistor to avoid malfunction from external surge and ESD. (It might be optional.) From 200Ω to 1kΩ is recommended for R_S. The size and shape of touch PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10mm x 7mm).

The connection line of CS to the touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detection caused by connection line.



Normal sensitivity selection selected

SYNC Implementation



From two TS01S to ten TS01S can work on the one application at the same time thanks to the SYNC function in this pin. The SYNC pulse prevents over two sensing signal from interfering with each other. During the sense disenable period and SYNC input high internal clock is suspended. The RSYNC is pull-down resistor of SYNC pin. Too big value of R_{SYNC} makes the SYNC pulse falling delay, and too small value of R_{SYNC} makes rising delay. The typical value of R_{SYNC} is 2MΩ. The SYNC pin should be implemented as above.

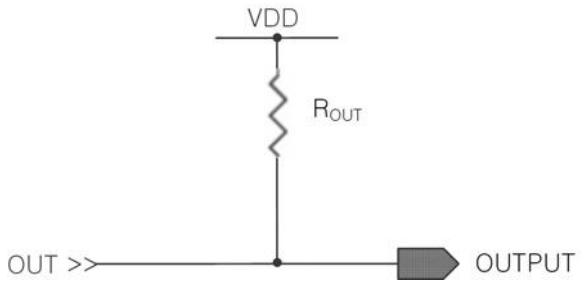
When SYNC is implemented as above figure (connect R_{SYNC} between SYNC and GND) TS01S has high sensitivity.

SYNC Implementation for Sensitivity Selection

Another function of SYNC pin of TS01S is the selection of sensitivity without any additional external component. Except using R_{SYNC} case (has high sensitivity), TS01S can't operate with SYNC function.
SYNC implementation for sensitivity selection is informed as below chart.

SYNC Connection	Using R_{SYNC} Connection	Connection to VDD	Connection to GND
Sensitivity	High	Middle	Low

OUTPUT Implementation



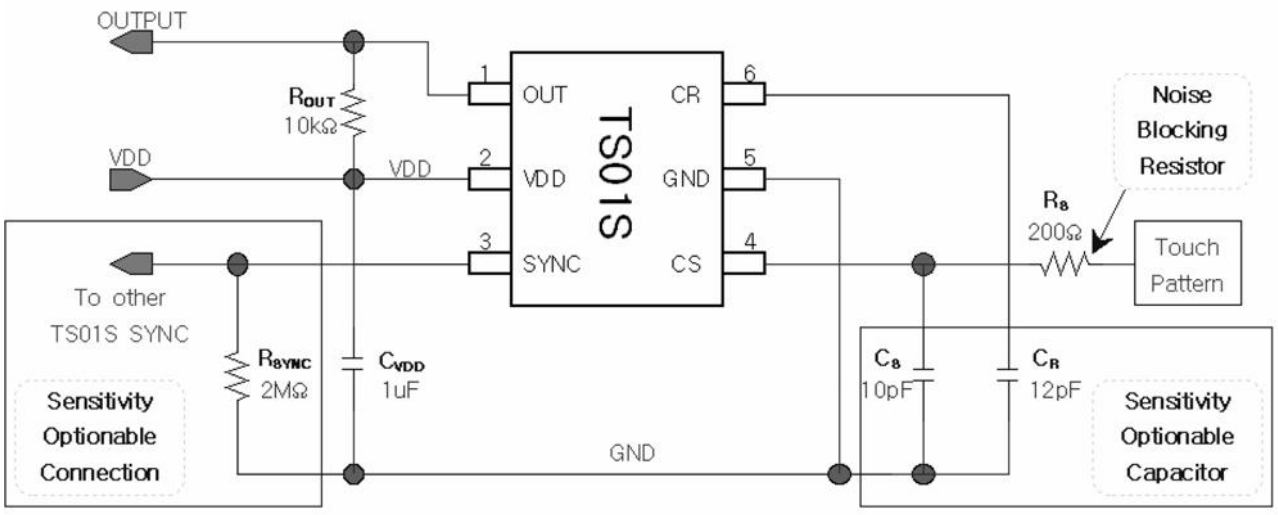
The OUT is an open drain structure. For this reason, the connection of pull-up resistor R_{OUT} is required between OUT and VDD or another lower voltage node. When R_{OUT} is connected to higher voltage node than VDD, the output current passes through protection diode to VDD and abnormal operation may be occurred. The OUT pin may be used as D/A (Digital to Analog) output port of multi-key application thanks to open drain structure.

The maximum output sink current is 4mA, so over a few kΩ must be used as R_{OUT}. Normally 10kΩ is used as R_{OUT}. The OUT is high in normal situation, and the value is low when a touch is detected on CS.

Internal Reset Operation

The TS01S has stable internal reset circuit that offers reset pulse to digital block. The supply voltage for a system start or restart should be under 0.3·VDD of normal operation VDD. No external components required for TS01S power reset, thus it helps simple circuit design and minimize the cost of application.
(Note: The VDD rising time should be less then 100ms for proper power on reset.)

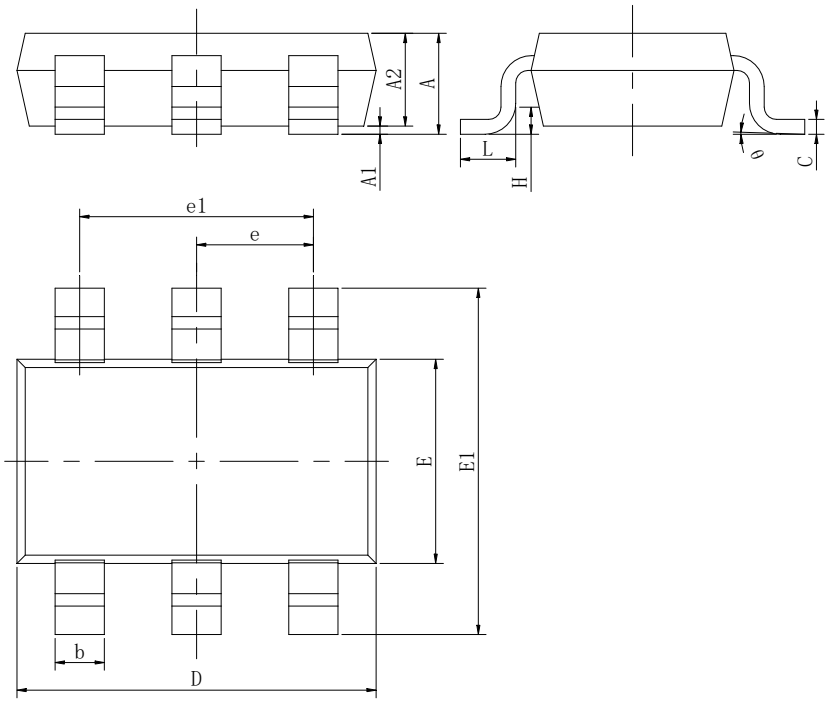
Application Example



- The capacitor and resistor might be connected with CS (pin4) for getting a stable sensitivity.
- The capacitor value which is connected to CR pin (C_R) should be almost the same as the total CS capacitance (C_{S_TOT}) for an effective differential sensitivity calibration.
- TS01S is reset by internal reset circuit. VDD voltage rising time should be shorter than 100msec for proper operation.
- The sensitivity can be adjusted through a connection of SYNC pin.
- From two TS01S to ten TS01S can work on the one application at the same time thanks to SYNC function.
- TS01S OUT port has an open drain structure. The pull-up resistor should therefore be needed as above figure.
- VDD periodic voltage ripples over 50mV or the ripple frequency which is lower than 10 kHz it can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from the other circuit. Especially the LED driver power line or digital switching circuit power line should be certainly treated to be separated from touch circuit.
- The C_S pattern should be routed as short as possible and the width of the line should be around 0.25mm.
- The C_S pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- The capacitor which is between VDD and GND is an obligation. It should be placed as close as possible from TS01S.
- The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise that causes interference with the sensing frequency.

Outline Dimensions

SOT23-6 Unit: mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.130	0.000	0.005
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.95（BSC）		0.037(BSC)	
e1	1.90（BSC）		0.075(BSC)	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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