

0.85V Minimum Input and 5.5V Maximum Output High Efficiency 700nA Ultra Low I_Q, 1A Synchronous Boost Advanced Design Specification

General Description

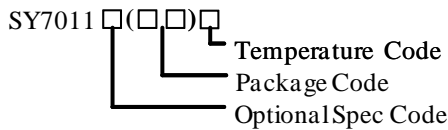
SY7011A is a high efficient, 700nA low I_Q, synchronous, Boost converter designed for one-cell Li-Ion or Li-polymer, or a two to three-cell alkaline Ni-Cd or Ni-MH battery powered applications. It can convert down to 0.85V input voltage. It adopts NMOS for the main switch and PMOS for the synchronous switch.

SY7011A can disconnect the output from input during the shutdown mode. When input voltage exceeds the regulated output voltage, SY7011A enters bypass mode automatically.

Features

- 0.85V Minimum Input Voltage
- Adjustable Output Voltage From 1.8V to 5.5V
- Min 1A Valley Current Limit
- 700nA Low Quiescent Current
- 5V/0.5A Output Capability
- Load Disconnect During Shutdown
- Low R_{DS(ON)} (Main Switch/Synchronous Switch) at 3.3V Output: 120/200mΩ
- Output OVP
- RoHS Compliant and Halogen Free
- Auto Bypass Mode When V_{IN} ≥ V_{OUT}
- Compact Package SOT23-6

Ordering Information



Ordering Number	Package type	Note
SY7011AABC	SOT23-6	----

Applications

- All Single Cell Li or Dual Cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment

Typical Applications

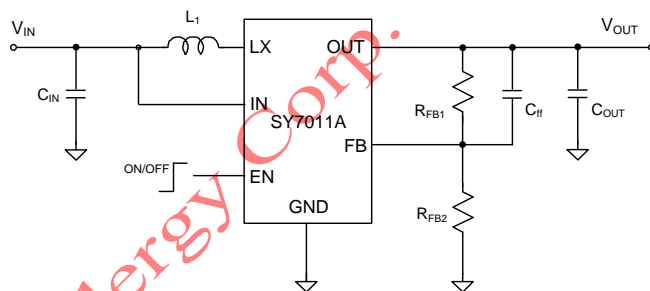


Figure 1. Schematic Diagram

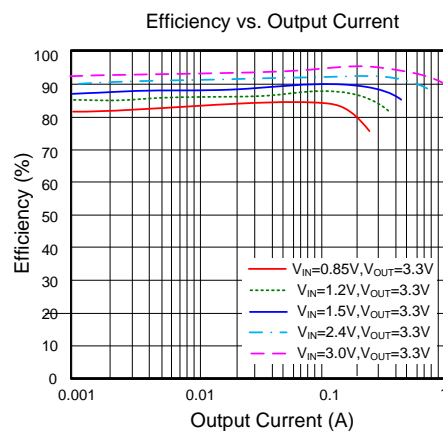
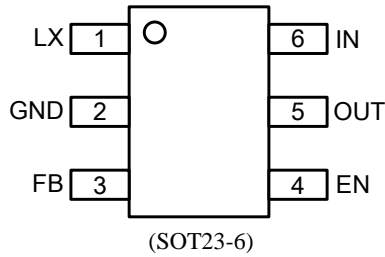


Figure 2. Efficiency vs. Load Current

Pinout (top view)



Top mark: **F2**xyz, for SY7011AABC (Device code: **F2**, x=year code, y=week code, z=lot number code)

Pin Name	Pin Number	Pin Description
LX	1	Inductor node. Connect an inductor between the IN pin and the LX pin.
GND	2	Ground pin.
FB	3	Feedback pin. Connect a resistor R_{FB1} between OUT and FB, and a resistor R_{FB2} between FB and GND to program the output voltage. $V_{OUT} = 1.2V \times (R_{FB1}/R_{FB2} + 1)$.
EN	4	Enable pin. Pull high to turn on. Do not leave it floating.
OUT	5	Output pin. Decouple this pin to the GND pin with a minimum of 22 μ F ceramic capacitor.
IN	6	Input pin.

Block Diagram

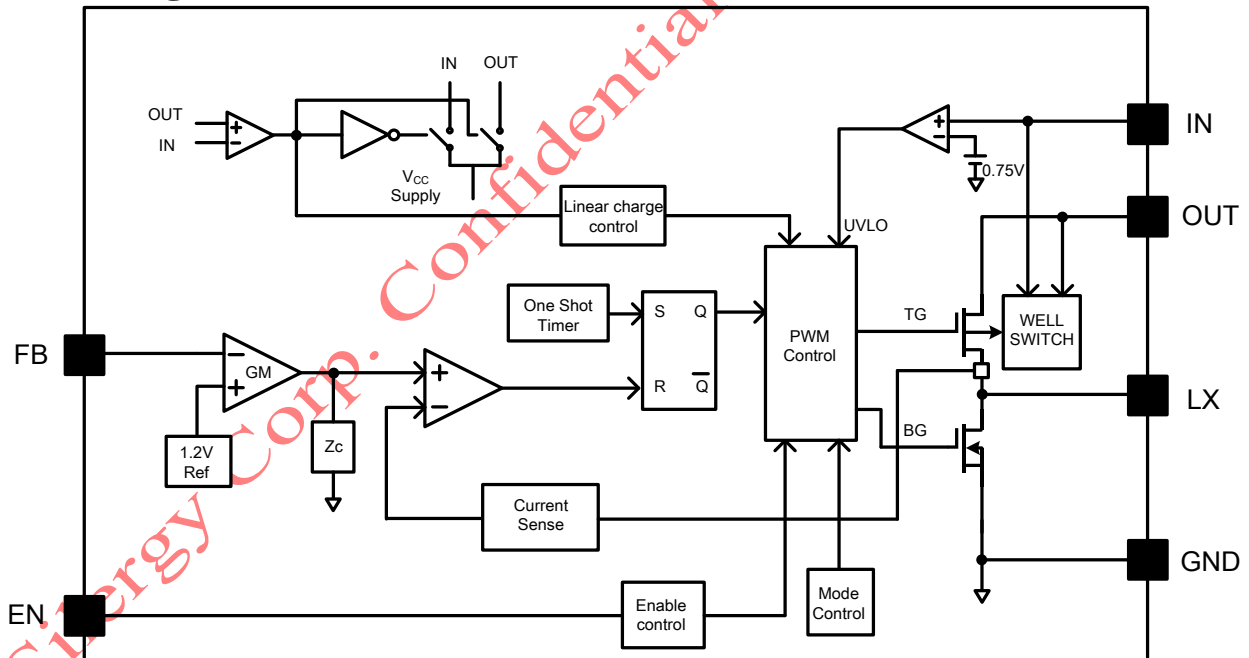


Figure3. Block Diagram



Absolute Maximum Ratings (Note 1)

FB, IN, OUT, EN	-0.3V to 6.0V
LX	-0.3V ^(*1) to 6.0V ^(*2)
Power Dissipation, P _D @ T _A =25 °C SOT23-6	1W
Package Thermal Resistance (Note 2)	
θ _{JA}	100 °C/W
θ _{JC}	30 °C/W
Junction Temperature Range	-40 °C to 150 °C
Lead Temperature (Soldering, 10 sec.)	260 °C
Storage Temperature Range	-65 °C to 150 °C

(*1) LX Voltage tested down to -3V < 20ns

(*2) LX Voltage tested up to +7V < 20ns

Recommended Operating Conditions (Note 3)

IN	0.85V to 5.5V
OUT	1.8V to 5.5V
EN	0V to V _{OUT} +0.3V
All Other Pins	0-5.5V
Junction Temperature Range	-40 °C to 125 °C
Ambient Temperature Range	-40 °C to 85 °C

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Electrical Characteristics

($V_{IN}=2.4V$, $V_{OUT}=3.3V$, $I_{OUT}=500mA$, $T_A = 25^\circ C$, unless otherwise specified)

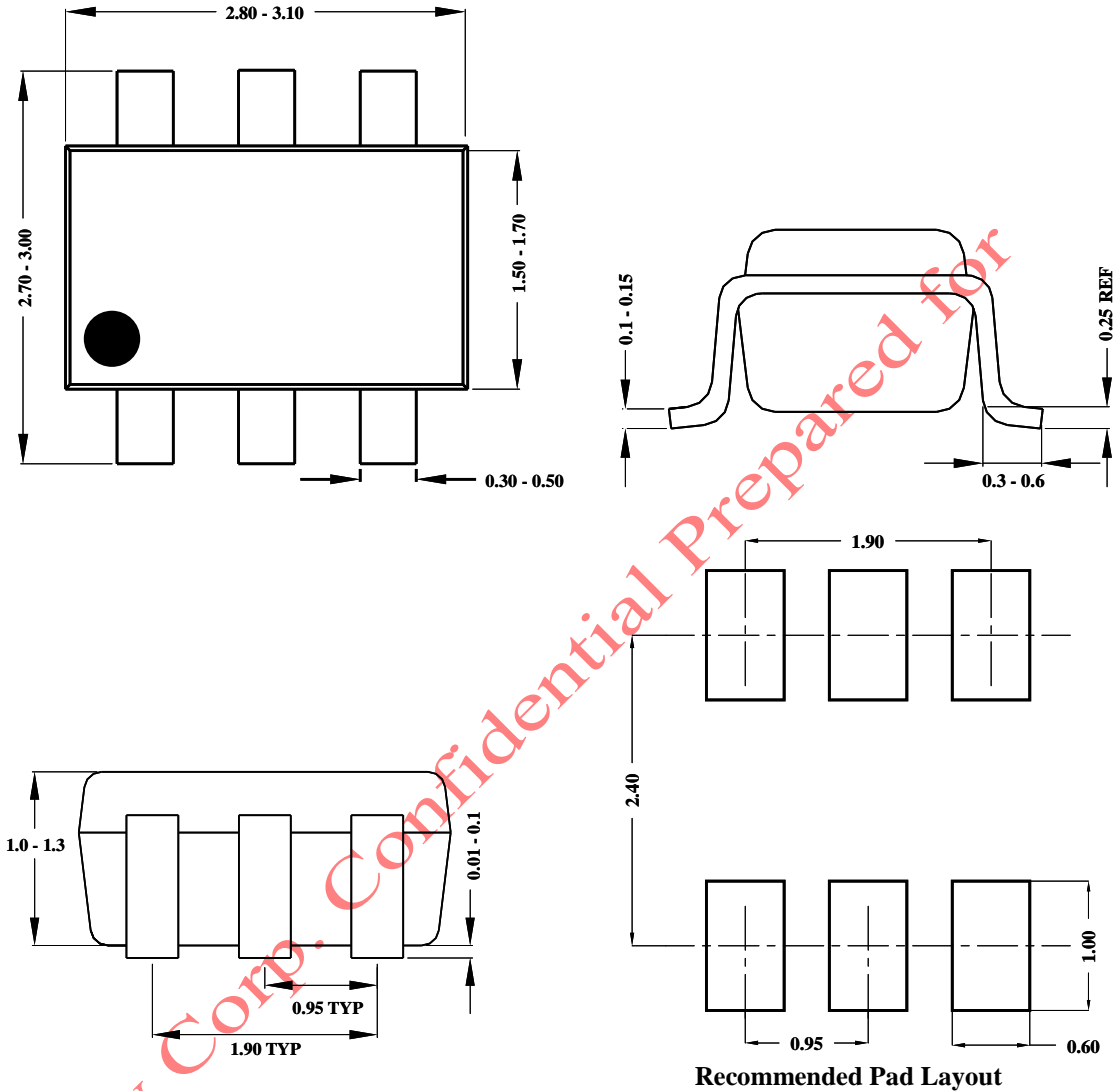
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		0.85		5.5	V
Input UVLO Threshold	V_{UVLO}			0.7	0.85	V
Input UVLO Hysteresis	V_{HYS}			0.04		V
Input Quiescent Current	I_Q	$V_{FB}=1.3V, V_{EN}=V_{IN}=1V,$ $V_{OUT}=3.4V$		700		nA
Shutdown Current	I_{SHDN}	$V_{EN}=0V, V_{IN}=2.4V$		0.1	1	μA
Linear Charge Current	I_{CHARGE}	$V_{OUT}<0.5V_{IN}$		1		A
Feedback Reference Voltage	V_{REF}		1.182	1.2	1.218	mV
Low Side Main FET R_{ON}	$R_{DS(ON)1}$			120		m Ω
Synchronous FET R_{ON}	$R_{DS(ON)2}$			200		m Ω
EN Input Voltage High	$V_{EN,H}$	$V_{IN}\leq 1.6V$ and $V_{OUT}\leq 1.6V$	0.7			V
		$V_{IN}>1.6V$ or $V_{OUT}>1.6V$	1.2			V
EN Input Voltage Low	$V_{EN,L}$	$V_{IN}\leq 1.6V$ and $V_{OUT}\leq 1.6V$			0.25	V
		$V_{IN}>1.6V$ or $V_{OUT}>1.6V$			0.4	V
EN Leakage Current	$I_{EN,LK}$	$V_{EN}=3.3V$	-1		1	μA
Min ON Time	$t_{ON,MIN}$			60		ns
Min OFF Time	$t_{OFF,MIN}$			140		ns
Soft-start Time	t_{SS}			1		ms
Switching Frequency	F_{SW}	$V_{OUT}=3.3V, CCM$		1		MHz
Valley FET Current Limit	$I_{LMT,VAL}$		1			A
Output Over Voltage Threshold	V_{OVP}			5.8		V
Output Over Voltage Hysteresis	$V_{OVP,HYS}$			0.3		V
Thermal Shutdown Temperature	T_{SD}			150		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYS}			20		$^\circ C$

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at $T_A = 25^\circ C$ on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

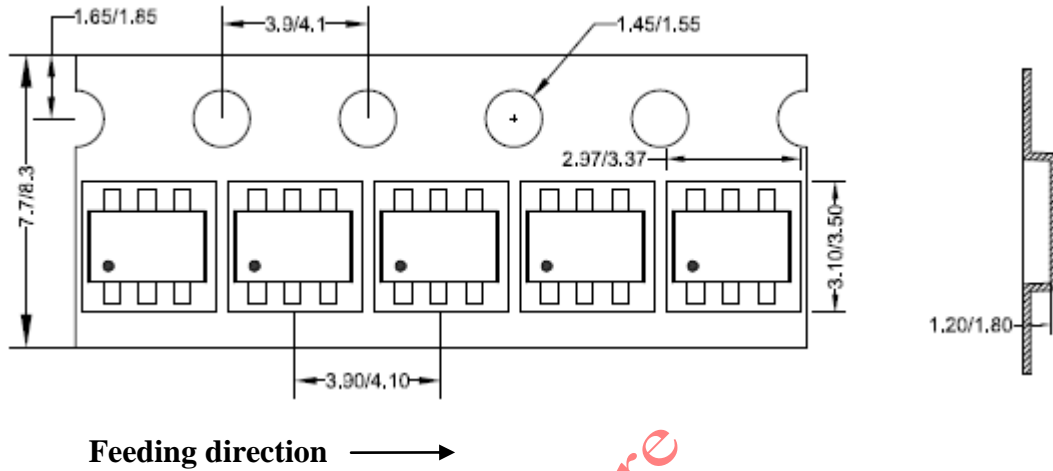
SOT23-6 Package Outline & PCB Layout Design



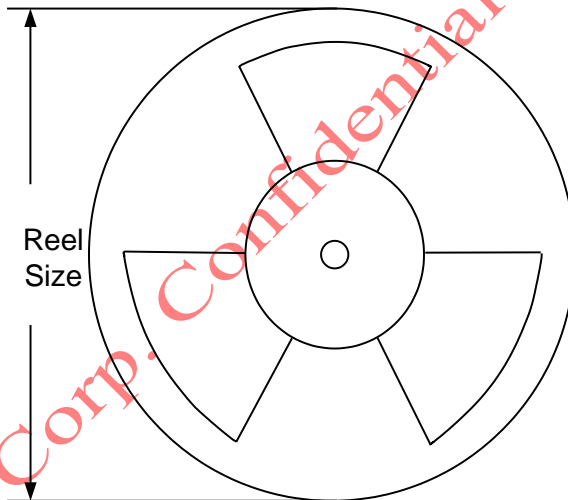
Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

Taping & Reel Specification

1. Taping orientation for packages (SOT23-6)



2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	280	160	3000

3. Others: NA