

# FDMA507PZ-VB Datasheet

## P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
- 20	0.030 at V <sub>GS</sub> = - 4.5 V	-10 <sup>a</sup>	18 nC
	0.040 at V <sub>GS</sub> = - 2.5 V	-9 <sup>a</sup>	

### FEATURES

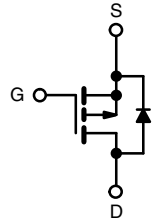
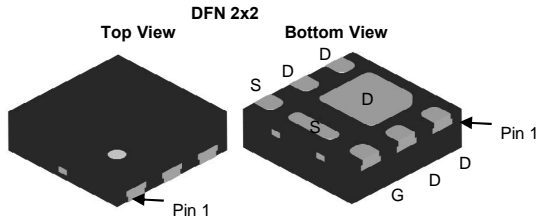
- TrenchFET<sup>®</sup> Power MOSFET
- Thermally Enhanced DFN2X2 Package
- Small Footprint Area
- Low On-Resistance



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Load Switch, PA Switch, and Battery Switch for Portable Devices



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	- 20	V
Gate-Source Voltage	V <sub>GS</sub>	± 12	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	- 10 <sup>a</sup>
		T <sub>C</sub> = 70 °C	- 8 <sup>a</sup>
		T <sub>A</sub> = 25 °C	- 10 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	- 8 <sup>b, c</sup>
Pulsed Drain Current (t = 300 μs)	I <sub>DM</sub>	- 30	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	- 2.5 <sup>b, c</sup>
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	17
		T <sub>C</sub> = 70 °C	11
		T <sub>A</sub> = 25 °C	3.3 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	2.1 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		250	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 5 s	R <sub>thJA</sub>	28	38	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	5.6	7.5	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile The DFN2X2 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 80 °C/W.

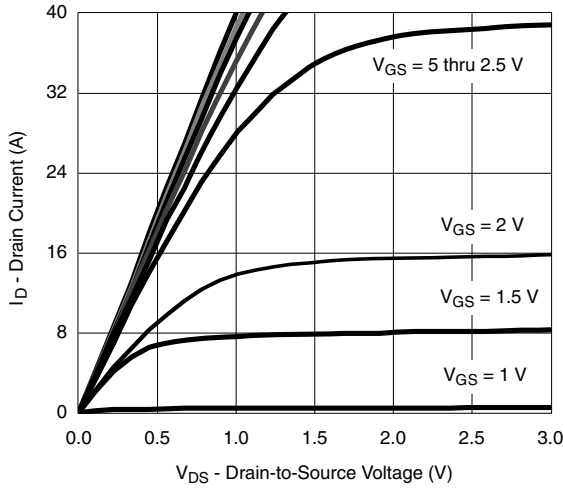
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-11		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.7		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.4		-1	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-20			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -6.7\text{ A}$		0.030		$\Omega$
		$V_{GS} = -2.5\text{ V}, I_D = -6.2\text{ A}$		0.040		
		$V_{GS} = -1.8\text{ V}, I_D = -2.3\text{ A}$		0.042		
		$V_{GS} = -1.5\text{ V}, I_D = -1\text{ A}$		0.050		
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -10\text{ V}, I_D = -6.7\text{ A}$		30		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1600		pF
Output Capacitance	$C_{oss}$			430		
Reverse Transfer Capacitance	$C_{rss}$			370		
Total Gate Charge	$Q_g$	$V_{DS} = -6\text{ V}, V_{GS} = -8\text{ V}, I_D = -10\text{ A}$		38	54	nC
				23	33	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -6\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$		3		nC
Gate-Drain Charge	$Q_{gd}$			6.5		
Gate Resistance	$R_g$		$f = 1\text{ MHz}$		7	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}, R_L = 0.75\text{ }\Omega$ $I_D \cong -8\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		20	30	ns
Rise Time	$t_r$			40	60	
Turn-Off Delay Time	$t_{d(off)}$			65	100	
Fall Time	$t_f$			40	60	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}, R_L = 0.75\text{ }\Omega$ $I_D \cong -8\text{ A}, V_{GEN} = -8\text{ V}, R_g = 1\text{ }\Omega$		10	15	ns
Rise Time	$t_r$			12	20	
Turn-Off Delay Time	$t_{d(off)}$			70	105	
Fall Time	$t_f$			40	60	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			-10	A
Pulse Diode Forward Current	$I_{SM}$				30	
Body Diode Voltage	$V_{SD}$	$I_S = -8\text{ A}, V_{GS} = 0\text{ V}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = -8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		40	60	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			20	30	nC
Reverse Recovery Fall Time	$t_a$			14		ns
Reverse Recovery Rise Time	$t_b$			26		

Notes:

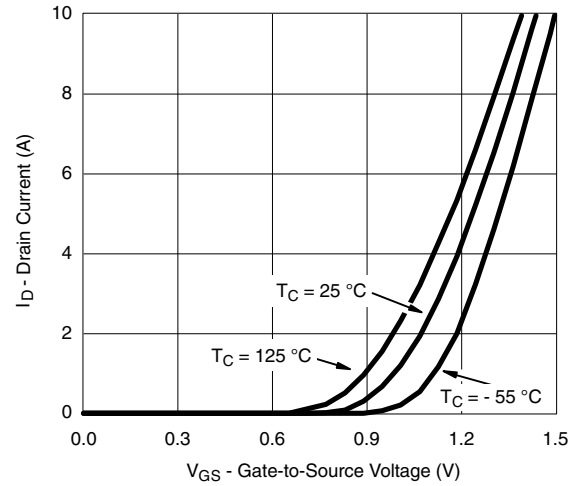
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

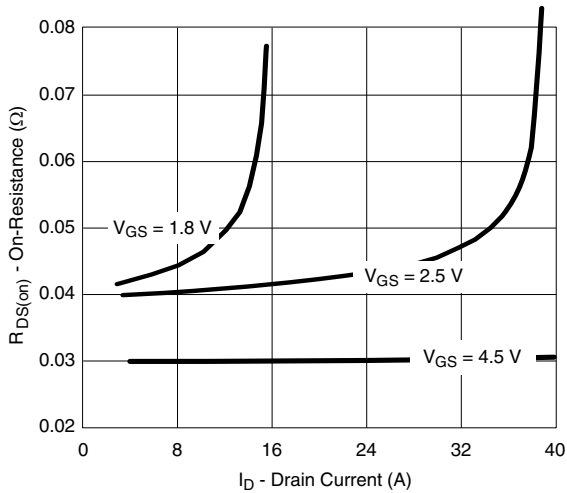
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



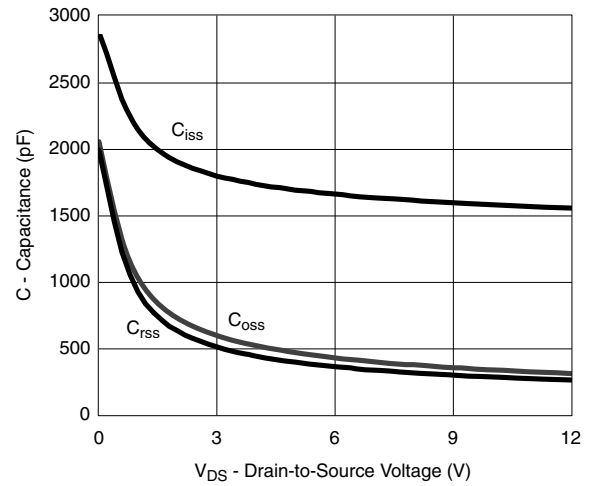
**Output Characteristics**



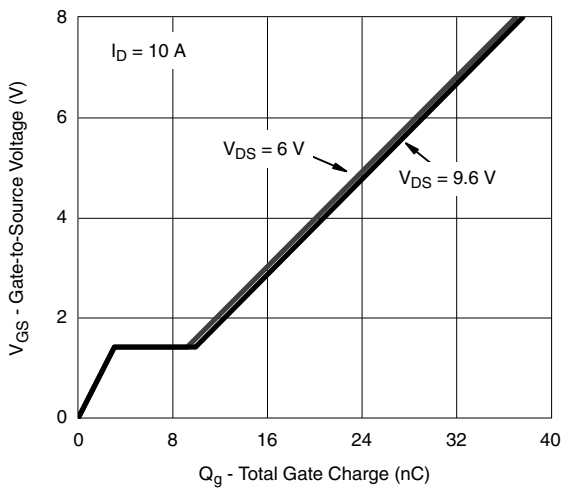
**Transfer Characteristics**



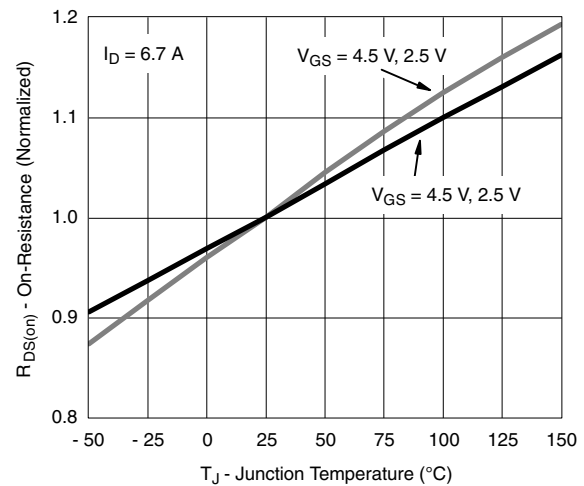
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**

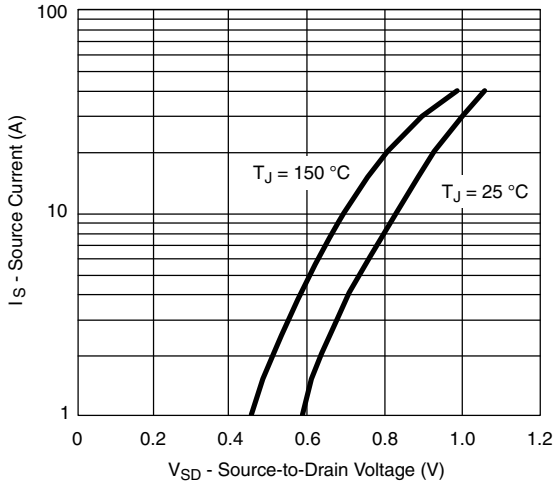


**Gate Charge**

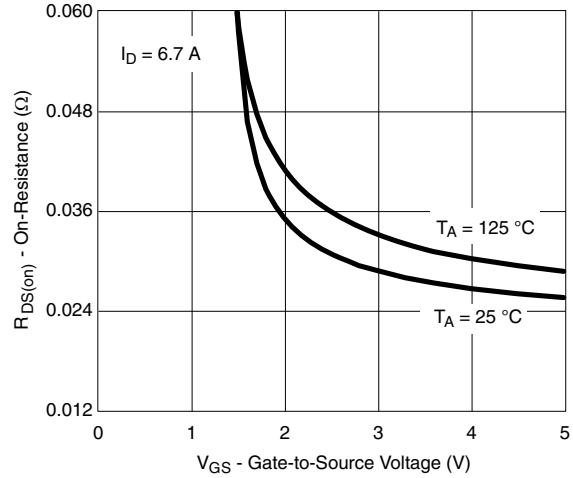


**On-Resistance vs. Junction Temperature**

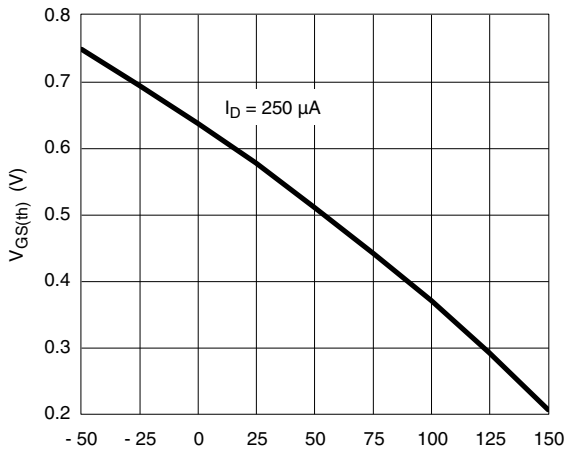
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



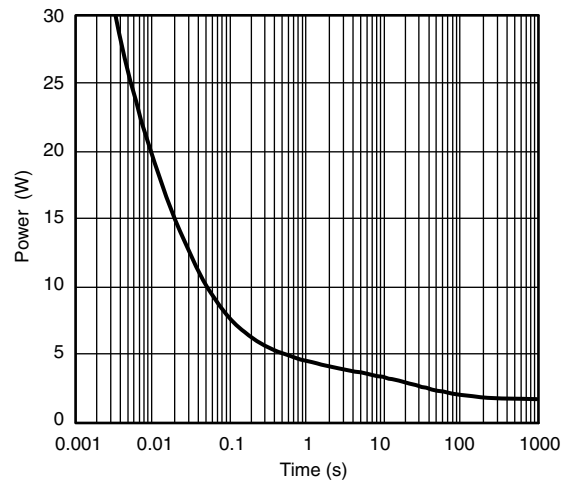
**Source-Drain Diode Forward Voltage**



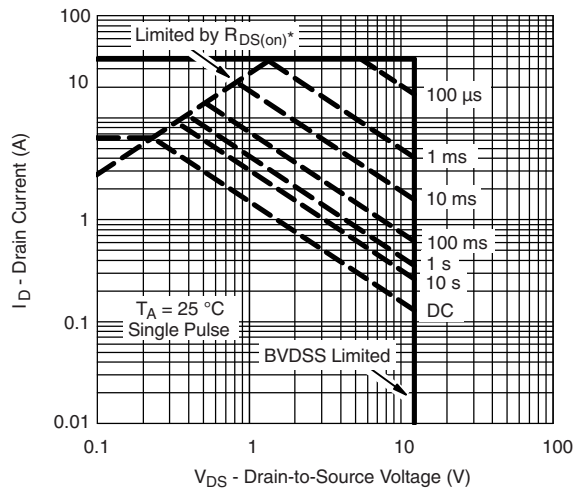
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**

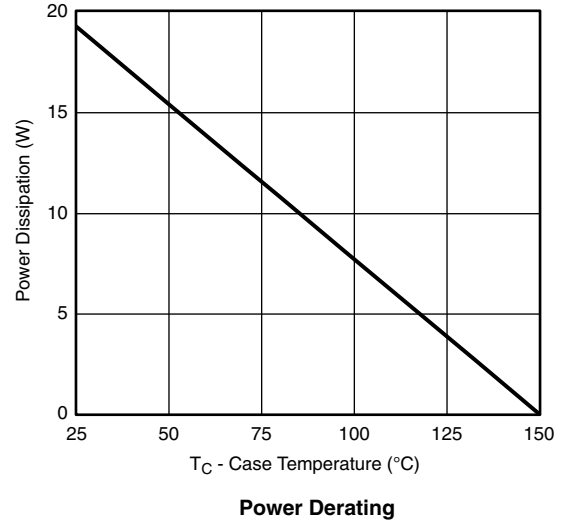
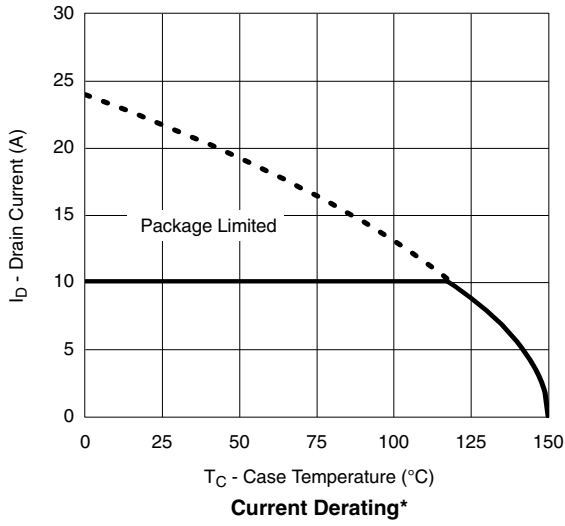


**Single Pulse Power, Junction-to-Ambient**



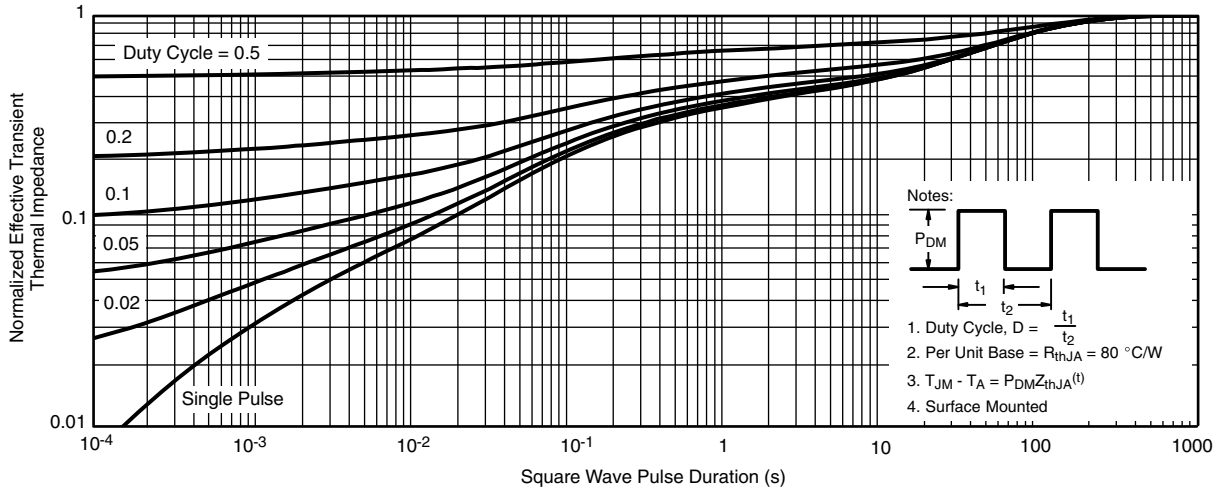
**Safe Operating Area, Junction-to-Ambient**  
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

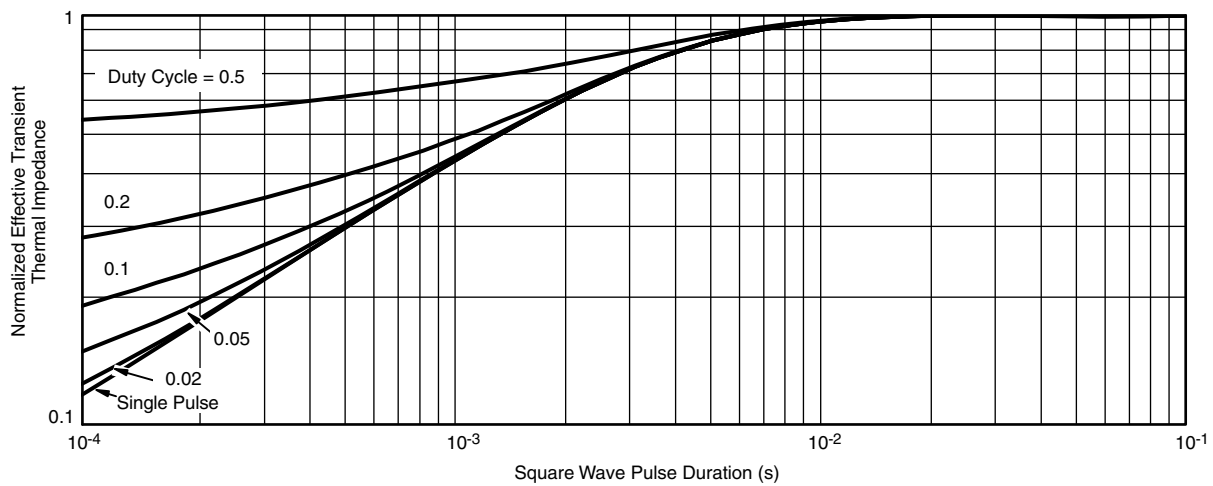


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

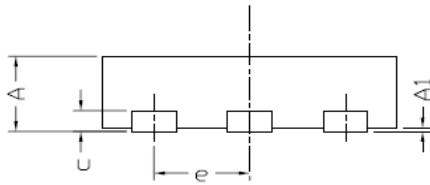
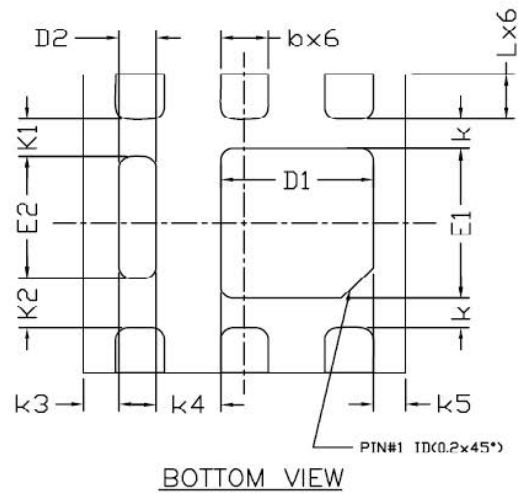
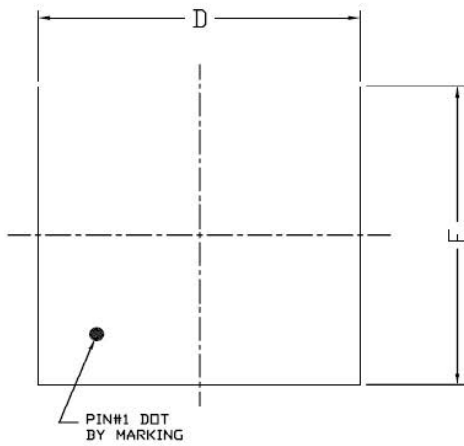


**Normalized Thermal Transient Impedance, Junction-to-Ambient**

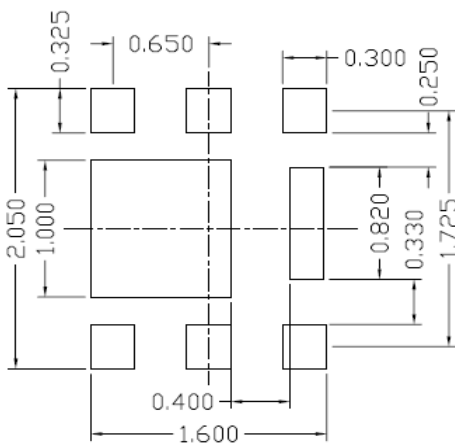


**Normalized Thermal Transient Impedance, Junction-to-Case**

DFN2x2 \_6L\_EP1\_S PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



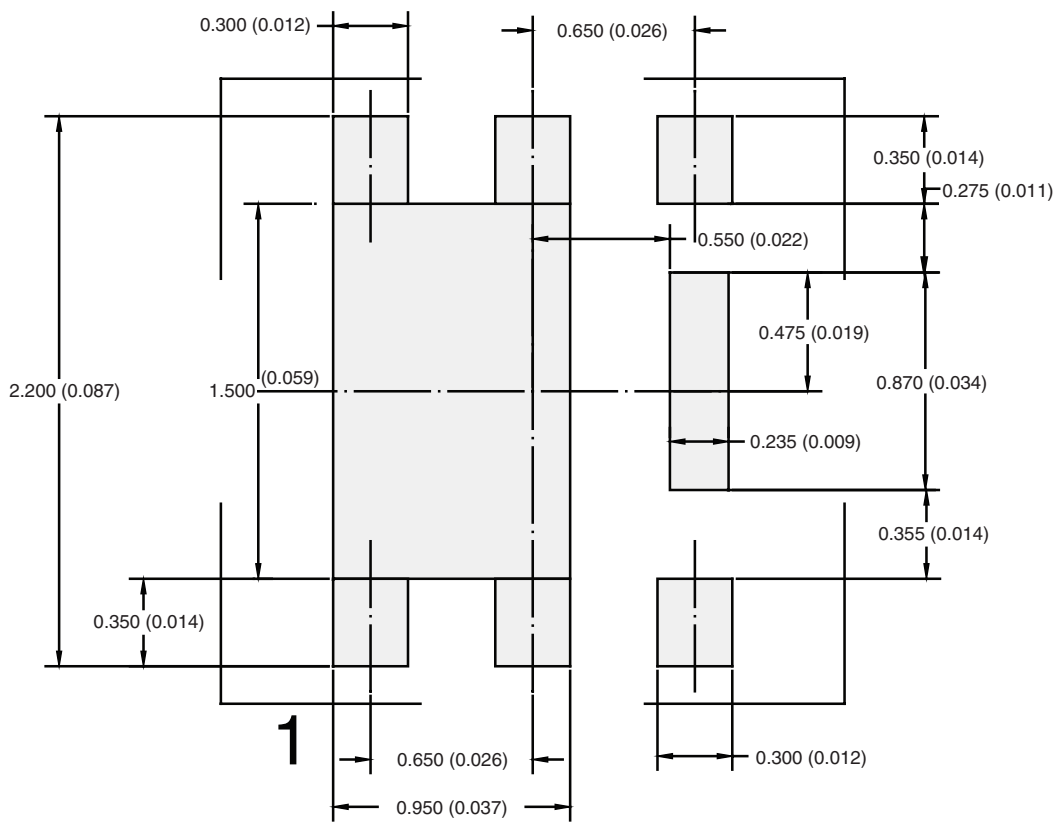
UNIT: mm

NOTE

1. CONTROLLING DIMENSION IS MILLIMETER.  
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	—	0.05	0.000	—	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.152 REF			0.006 REF		
D	1.90	2.00	2.10	0.075	0.079	0.083
D1	0.85	0.95	1.05	0.033	0.037	0.041
D2	0.13	0.23	0.33	0.005	0.009	0.013
E	1.90	2.00	2.10	0.075	0.079	0.083
E1	0.90	1.00	1.10	0.035	0.039	0.043
E2	0.72	0.82	0.92	0.028	0.032	0.036
e	0.65 BSC			0.026 BSC		
K	0.20 BSC			0.008 BSC		
K1	0.25 BSC			0.010 BSC		
K2	0.33 BSC			0.013 BSC		
K3	0.22 BSC			0.009 BSC		
K4	0.40 BSC			0.016 BSC		
K5	0.20 BSC			0.008 BSC		
L	0.25	0.30	0.35	0.010	0.012	0.014

RECOMMENDED PAD LAYOUT FOR DFN2X2



Dimensions in mm/(Inches)



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