

# IRFZ48NPBF-VB Datasheet

## N-Channel 60 V (D-S) MOSFET

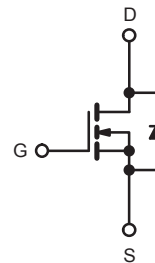
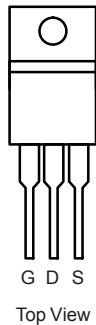
PRODUCT SUMMARY		
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>
60	0.024 at V <sub>GS</sub> = 10 V	50
	0.028 at V <sub>GS</sub> = 4.5 V	40

**FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Logic-Level Gate Drive
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



TO-220AB



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>		60	V
Gate-Source Voltage	V <sub>GS</sub>		± 20	
Continuous Drain Current <sup>f</sup>	V <sub>GS</sub> at 10 V	I <sub>D</sub>	T <sub>C</sub> = 25 °C	A
Continuous Drain Current			T <sub>C</sub> = 100 °C	
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>		200	W/°C
Linear Derating Factor			1.0	
Linear Derating Factor (PCB Mount) <sup>e</sup>			0.025	
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>		400	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		150	W
Maximum Power Dissipation (PCB Mount) <sup>e</sup>	T <sub>A</sub> = 25 °C		3.7	
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt		4.5	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>		- 55 to + 175	°C
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s		300 <sup>d</sup>	

**Notes**

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V<sub>DD</sub> = 25 V, starting T<sub>J</sub> = 25 °C, L = 179 μH, R<sub>θ</sub> = 25 Ω, I<sub>AS</sub> = 51 A (see fig. 12).
- I<sub>SD</sub> ≤ 51 A, di/dt ≤ 250 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 175 °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).
- Current limited by the package, (die current = 51 A).

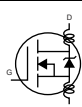
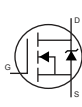
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	40	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

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**SPECIFICATIONS** ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	60	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.070	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	-	2.5		
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 10\text{ V}$	-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$	
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 21\text{ A}^b$	-	0.024	-	$\Omega$
		$V_{GS} = 4.5\text{ V}$	$I_D = 15\text{ A}^b$	-	0.028	-	
Forward Transconductance	$g_{fs}$	$V_{DS} = 25\text{ V}, I_D = 21\text{ A}^b$	23	-	-	S	
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz, see fig. 5}$	-	190	-	pF	
Output Capacitance	$C_{oss}$		-	920	-		
Reverse Transfer Capacitance	$C_{rss}$		-	170	-		
Total Gate Charge	$Q_g$	$V_{GS} = 5.0\text{ V}$	$I_D = 51\text{ A}, V_{DS} = 48\text{ V},$ see fig. 6 and 13 <sup>b</sup>	-	-	66	nC
Gate-Source Charge	$Q_{gs}$			-	-	12	
Gate-Drain Charge	$Q_{gd}$			-	-	43	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, I_D = 51\text{ A},$ $R_g = 4.6\text{ }\Omega, R_D = 0.56\text{ }\Omega,$ see fig. 10 <sup>b</sup>	-	17	-	ns	
Rise Time	$t_r$		-	230	-		
Turn-Off Delay Time	$t_{d(off)}$		-	2	-		
Fall Time	$t_f$		-	110	-		
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	50°	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	200	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 51\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	2.5	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 51\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	130	180	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	0.84	1.3	$\mu\text{C}$	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- c. Current limited by the package, (Die Current = 51 A).

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$

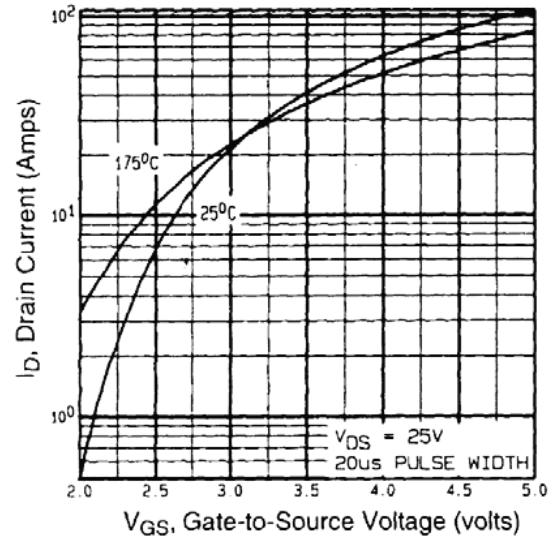


Fig. 3 - Typical Transfer Characteristics



Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$

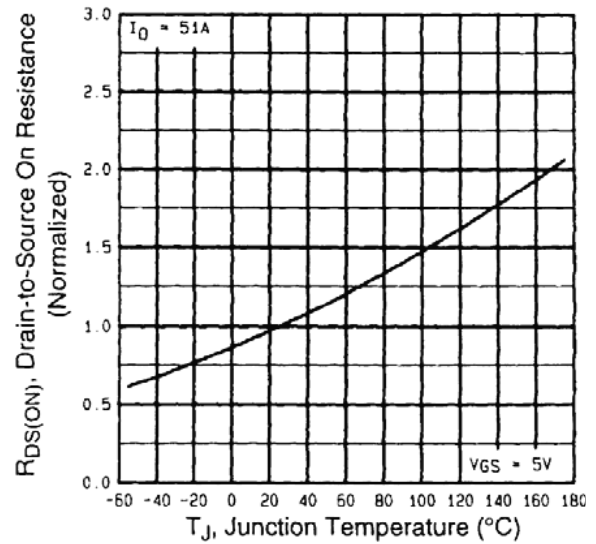


Fig. 4 - Normalized On-Resistance vs. Temperature

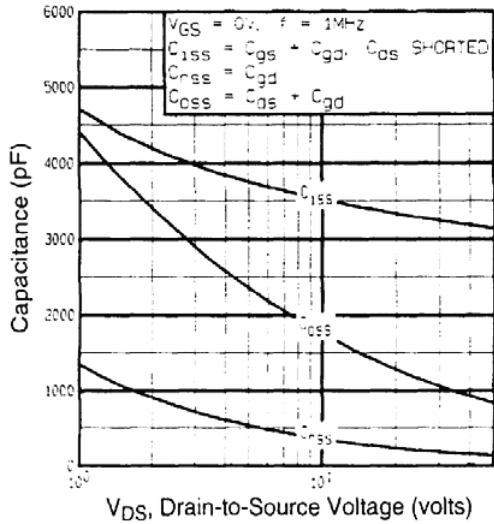


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 8 - Maximum Safe Operating Area

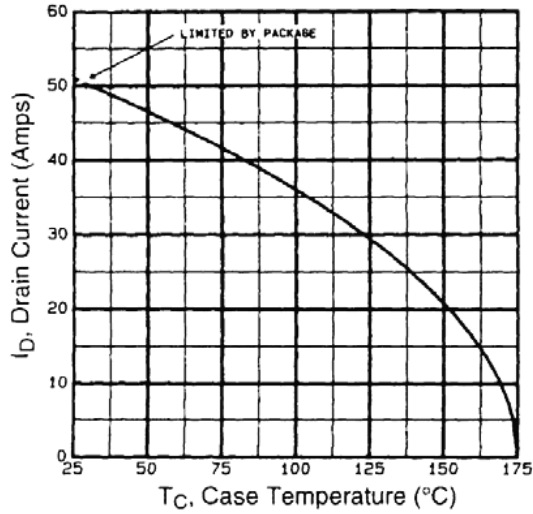


Fig. 9 - Maximum Drain Current vs. Case Temperature

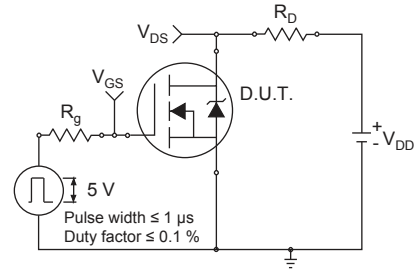


Fig. 10a - Switching Time Test Circuit

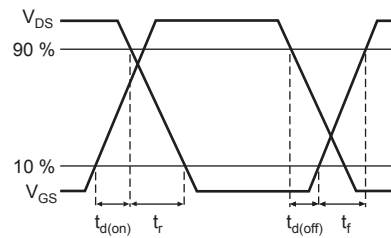


Fig. 10b - Switching Time Waveforms

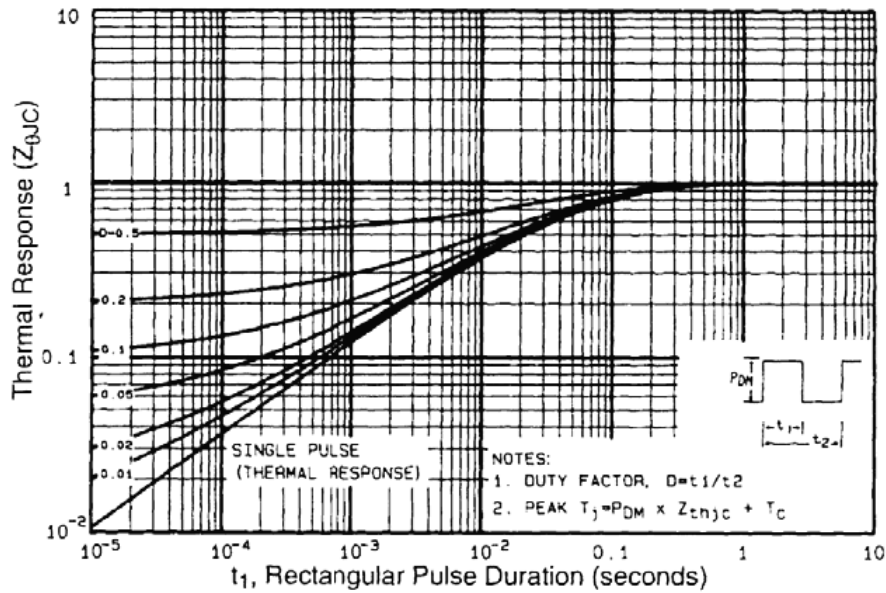


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

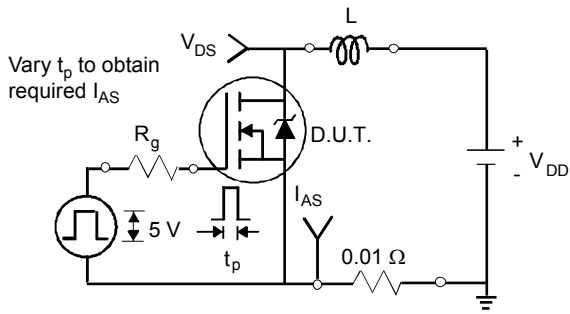


Fig. 12a - Unclamped Inductive Test Circuit

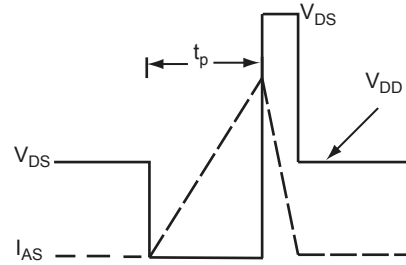


Fig. 12b - Unclamped Inductive Waveforms



Fig. 12c - Maximum Avalanche Energy vs. Drain Current

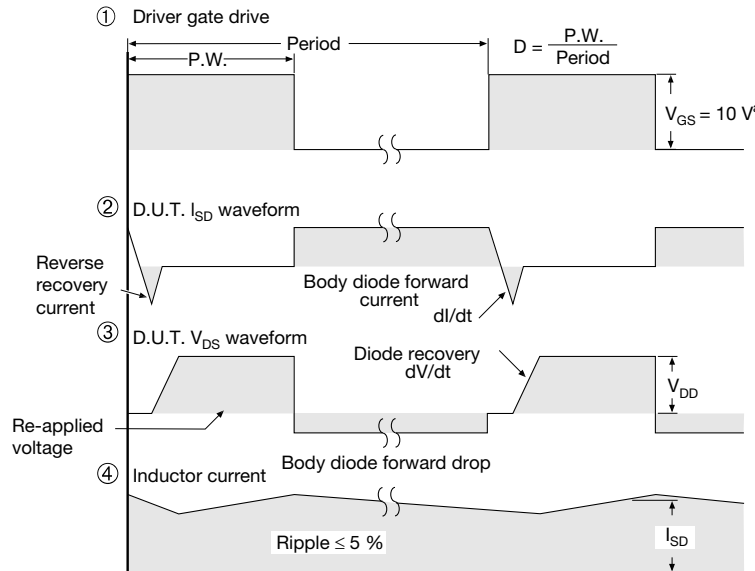


Fig. 13a - Basic Gate Charge Waveform



Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

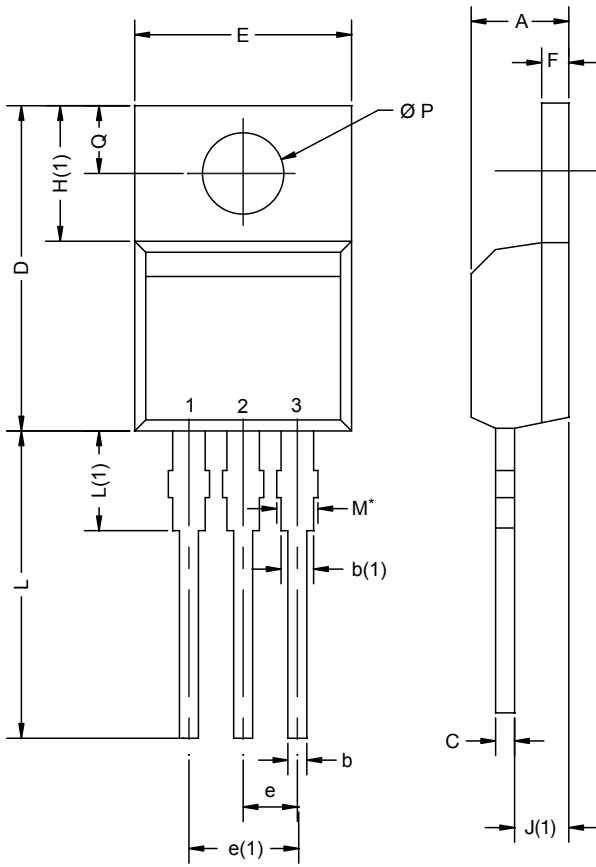


Note

a.  $V_{GS} = 5 V$  for logic level devices

Fig. 14 - For N-Channel

TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12  
DWG: 5471

**Notes**  
\* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
Heatsink hole for HVM



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