NCA1021

LIN Transceiver with multiple modes

Datasheet (EN) 1.0

Product Overview

The NCA1021 is a LIN (Local Interconnect Network) transceiver with a low-power mode and multiple wake-up methods. Support up to 20kbps for sending and receiving communication.

The NCA1021 has a sleep mode with extremely low power consumption. Support remote wake-up and local wake-up via LIN bus or other pins. The device can also use the INH output pin as a flag to control the working status of other devices in the local system to achieve low-power operation of the system.

The NCA1021 converts the signal received by TXD into a LIN bus signal through waveform shaping and slew rate adjustment to reduce Electro Magnetic Emission (EME). TXD has a fault timeout protection function to prevent the LIN bus from being occupied.

Key Features

- Fully compatible with the ISO 17987-4 standard
- Very low Electro Magnetic Emission (EME)
- High Electro Magnetic Immunity (EMI)
- Support for 12-V applications
- Input levels compatible with 3.3 V and 5 V devices
- Bus fault protection of -40V to +40V
- Wake-up source recognition (local or remote)
- Integrated LIN pull-up resistor
- Transmit data (TXD) dominant time out function
- K-line
- AEC-Q100
- Over temperature protection
- Date rate: up to 20Kbps
- Junction temperature: -40℃~150℃
- RoHS-compliant packages:

  SOP8

  DFN8

Applications

- Body sensor and module control
- Car steering wheel and instrument cluster
- Powertrain system and electric engine

Device Information

Part Number	*Package*	*Body Size*
NCA1021-Q1SPR	SOP8	4.90mm × 3.90mm
NCA1021-Q1DNR	DFN8	3.00mm × 3.00mm

Pins Diagram

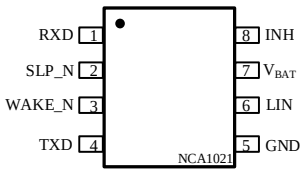


Figure 1. NCA1021 Block Diagram

INDEX

1. Pin Configuration and Functions

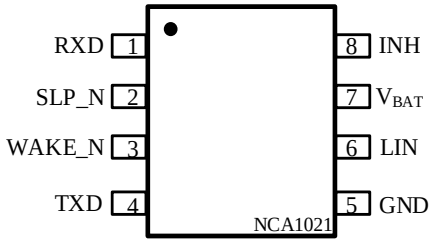


Figure 1.1 NCA1021 Package

Table1.1 NCA1021 Pin Configuration and Description

NCA1021-DSPR PIN NO.	*SYMBOL*	*FUNCTION*
1	RXD	receive data output (open-drain); active LOW after a wake-up event
2	SLP_N	sleep control input (active LOW); controls inhibit output; resets wake-up source flag on TXD and wake-up request on RXD
3	WAKE_N	local wake-up input (active LOW); negative edge triggered
4	TXD	transmit data input; active LOW output after a local wake-up event
5	GND	ground
6	LIN	LIN bus line input/output
7	V_{BAT}	battery supply voltage
8	INH	battery related inhibit output for controlling an external voltage regulator; active HIGH after a wake-up event

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
battery supply voltage	V_{BAT}	-0.3		40	V	
voltage on pin TXD	V_{TXD}	-0.3		6	V	I_{TXD} no limitation
		-0.3		7	V	I_{TXD} < 500 uA
voltage on pin RXD	V_{RXD}	-0.3		6	V	I_{RXD} no limitation
		-0.3		7	V	I_{RXD} < 500 uA
voltage on pin SLP_N	V_{SLP_N}	-0.3		6	V	I_{SLP_N} no limitation
		-0.3		7	V	I_{SLP_N} < 500 uA
voltage on pin LIN	V_{LIN}	-40		40	V	Limiting value with respect to GND, VBAT and VWAKE_N
voltage on pin WAKE_N	V_{WAKE_N}	-0.3		40	V	
current on pin WAKE_N	I_{WAKE_N}	-15			mA	only relevant if V_{WAKE_N} < V_{GND}-0.3 current will flow into pin GND
voltage on pin INH	V_{INH}	-0.3		V_{BAT}+0.3	V	
output current on pin INH	$I_{O(INH)}$	-50		15	mA	
electrostatic discharge voltage	V_{ESD}	-6		6	kV	on pins WAKE_N, LIN and VBAT,according to IEC 61000-4-2
	HBM	-6		6	kV	HBM,on pins WAKE_N, LIN, VBAT and INH
		-8		8	kV	HBM on pins RXD, SLP_N and TXD
	CDM	-2		2		All pins
virtual junction temperature	Tvj	-40		150	℃	
Storage Temperature	Tstg	-55		150	℃	

3. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
battery Supply Voltage	V_{BAT}	5.5		27	V
LIN Bus input voltage	V_{LIN}	0		27	V
TXD High level input voltage	V_{IH}	2		7	V
TXD Low level input voltage	V_{IL}	-0.3		0.8	V

4. Thermal Characteristics

Parameters	Symbol	SOP8	DFN8	Unit
Junction-to-Air Thermal Resistance	θ_{JA}	125.3	53.3	℃/W
Junction-to-case (top) thermal resistance	$\theta_{JC\ (top)}$	65.4	60	℃/W
Junction-to-board thermal resistance	θ_{JB}	68.7	25.6	℃/W

5. Specifications

5.1.Electrical Characteristics

(V_{BAT} = 5.5 V to 27 V, Tj=-40℃ to 150℃. Unless otherwise noted, Typical values are at V_{BAT} =12V, Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
battery supply current	I_{BAT}			20	uA	Sleep mode, V_{LIN} = V_{BAT} = V_{WAKE_N}, V_{TXD} = V_{SLP_N} = 0
				150	uA	Standby mode; bus recessive V_{INH} = V_{LIN} = V_{WAKE_N} = V_{BAT}; V_{TXD} = V_{SLP_N} = 0 V
				1200	uA	Standby mode; bus dominant V_{BAT} = V_{INH} = V_{WAKE_N} = 12V; V_{LIN} = 0V V_{TXD} = 0V; V_{SLP_N} = 0V
				1600	uA	Normal mode; bus recessive V_{INH} = V_{LIN} = V_{WAKE_N} = V_{BAT} V_{TXD} = 5 V, V_{SLP_N} = 5 V
				4	mA	Normal mode; bus dominant V_{BAT} = V_{INH} = V_{WAKE_N} = 12 V V_{TXD} = 0V, V_{SLP_N} = 5 V
Power on reset	$V_{th(POR)L}$	1.6	3.1	3.9	V	Low-level power-on reset threshold voltage
	$V_{th(POR)H}$	2.3	3.4	4.3	V	High-level power-on reset threshold voltage
	$V_{hys(POR)}$	0.01	0.3	1	V	power-on reset hysteresis voltage
	$V_{th(VBATL)L}$	3.9	4.4	4.7	V	Low-level V_{BAT} LOW threshold voltage
	$V_{th(VBATL)H}$	4.2	4.7	4.9	V	High-level V_{BAT} LOW threshold voltage
	$V_{hys(VBATL)}$	0.01	0.3	1	V	V_{BAT} LOW hysteresis voltage
TXD						
High level input voltage	V_{IH}	2		7	V	
Low level input voltage	V_{IL}	-0.3		0.8	V	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
hysteresis voltage	Vhys	50		400	mV	
Low level input current	I_{IL}	-5		5	uA	
Output Low current	I_{OL}	1.5			mA	local wake-up request; Standby mode; V_{WAKE_N} = 0 V; V_{LIN} = V_{BAT}; V_{TXD} = 0.4 V
pull-down resistance on pin	$R_{PD(TXD)}$	140		1200	kΩ	
SLP_N						
High level input voltage	V_{IH}	2		7	V	
Low level input voltage	V_{IL}	-0.3		0.8	V	
hysteresis voltage	Vhys	50		400	mV	
Low level input current	I_{IL}	-5		5	uA	V_{SLP_N} = 0 V
pull-down resistance on pin	$R_{PD(SLP\_N)}$	140		1200	kΩ	V_{SLP_N} = 5 V
RXD (Open drain)						
High level input current	I_{LH}	-5		5	uA	Normal mode; V_{LIN} = V_{BAT}; V_{RXD} = 5 V
Output Low current	I_{OL}	1.5			mA	Normal mode; V_{LIN} = 0 V; V_{RXD} = 0.4 V
WAKE_N						
High level input voltage	V_{IH}	V_{BAT}-1		V_{BAT}+0.3	V	
Low level input voltage	V_{IL}	-0.3		V_{BAT}-3.3	V	
High level input current	I_{IH}	-5		5	uA	V_{WAKE_N} = 27 V; V_{BAT} = 27 V
Low level input current	I_{IL}	-30		-1	uA	V_{WAKE_N} = 0 V
INH						
switch-on resistance between pins VBAT and INH	$R_{sw(VBAT-INH)}$		20	50	Ω	switch-on resistance between pins V_{BAT} and INH. Standby; Normal and Power-on modes; I_{INH} = -15 mA, VBAT = 12 V
HIGH-level leakage current	I_{IH}	-5		5	uA	Sleep mode; V_{INH} = 27 V; V_{BAT} = 27 V
LIN						
current limitation for driver dominant state	I_{BUS_LIM}	40		100	mA	V_{BAT} = 18 V; V_{LIN} = 18 V V_{TXD} =0V
pull-up resistance	Rpu	50		250	kΩ	Sleep mode; V_{SLP_N} = 0 V
receiver recessive input leakage current	$I_{BUS\_PAS\_rec}$			1	uA	V_{LIN} = 27 V; V_{BAT} = 5.5 V V_{TXD} =5V
receiver dominant input leakage current including	$I_{BUS\_PAS\_dom}$	-600			uA	Normal mode; V_{TXD} =5V V_{LIN} = 0 V; V_{BAT} = 12 V

Parameters	Symbol	Min	Typ	Max	Unit	Comments
pull-up resistor						
voltage drop at the serial diode	$V_{SerDiode}$	0.4		1	V	in pull-up path with R_{slave} , $I_{SerDiode}$ = 10 uA Not tested in production guaranteed by design
loss-of-ground bus current	$I_{BUS\_NO\_GND}$	-750		10	uA	V_{BAT} = 27 V; V_{LIN} =0V
loss-of-battery bus current	$I_{BUS\_NO\_BAT}$			1	uA	V_{BAT} = 0 V; V_{LIN} = 27 V
receiver dominant state	V_{BUSdom}			0.4V_{BAT}		
receiver recessive state	V_{BUSrec}	0.6V_{BAT}				
receiver center voltage	V_{BUS_CNT}	0.475V_{BAT}		0.525V_{BAT}	V	V_{BUS_CNT} = (V_{BUSrec} + V_{BUSdom})/2 V_{BAT} = 7V - 27V
receiver hysteresis voltage	V_{HYS}			0.175V_{BAT}		V_{HYS} = V_{BUSrec} - V_{BUSdom}
slave resistance	Rslave	20		47	kΩ	connected between pins LIN and V_{BAT}; V_{LIN} = 0 V; V_{BAT} = 12 V
capacitance on pin LIN	C_{LIN}			30	pF	
dominant output voltage	$V_{o(dom)}$			1.4	V	Normal mode; V_{TXD} = 0 V, V_{BAT} = 7 V
				2.0	V	Normal mode; V_{TXD} = 0 V, V_{BAT} = 18 V

5.2.Switching Electrical Characteristics

(V_{BAT} = 5.5 V to 18 V, Tj=-40℃ to 150℃. Unless otherwise noted, Typical values are at V_{BAT} =12V, Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Duty cycles(bus load conditions (CBUS; RBUS): 1 nF; 1 kΩ/6,8 nF; 660 Ω/10 nF; 500 Ω)						
Duty Cycle 1	D1	0.396				Vth(rec)(max) = 0.744 × V_{BAT} Vth(dom)(max) = 0.581 × V_{BAT} V_{BAT} = 7 V to 18 V; t_{bit} = 50 us
		0.396				Vth(rec)(max) = 0.76 × V_{BAT} Vth(dom)(max) = 0.593 × V_{BAT} V_{BAT} = 5.5 V to 7 V; t_{bit} = 50 us
Duty Cycle 2	D2				0.581	Vth(rec)(min) = 0.422 × V_{BAT} Vth(dom)(min) = 0.284 × V_{BAT} V_{BAT} = 7.6 V to 18 V; t_{bit} = 50 us
					0.581	Vth(rec)(min) = 0.41 × V_{BAT} Vth(dom)(min) = 0.275 × V_{BAT} V_{BAT} = 6.1 V to 7 V; t_{bit} = 50 us

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Duty Cycle 3	D3	0.417				Vth(rec)(max) = 0.778 × V_{BAT} Vth(dom)(max) = 0.616 × V_{BAT} V_{BAT} = 7 V to 18 V; t_{bit} = 96 us
		0.417				Vth(rec)(max) = 0.797 × V_{BAT} Vth(dom)(max) = 0.63 × V_{BAT} V_{BAT} = 5.5 V to 7 V; t_{bit} = 96 us
Duty Cycle 4	D4				0.59	Vth(rec)(min) = 0.389 × V_{BAT} Vth(dom)(min) = 0.251 × V_{BAT} V_{BAT} = 7.6 V to 18 V; t_{bit} = 96 us
					0.59	Vth(rec)(min) = 0.378 × V_{BAT} Vth(dom)(min) = 0.242 × V_{BAT} V_{BAT} = 6.1 V to 7 V; t_{bit} = 96 us
Timing characteristics						
fall time	t_f			22.5	us	20%-80% C_{BUS} = 1 nF and R_{BUS} = 1 kΩ C_{BUS} = 6.8 nF and R_{BUS} = 660 Ω C_{BUS} = 10 nF and R_{BUS} = 500 Ω
rise time	t_r			22.5	us	
difference between rise and fall time	$t_{(r-f)}$	-6		6	us	
transmitter propagation delay	t_{tx_pd}			10	us	rising and falling
transmitter propagation delay symmetry	t_{tx_sym}	-4		4	us	
receiver propagation delay	t_{rx_pd}			6	us	rising and falling C_{RXD} = 20 pF and R_{RXD} = 2.4 kΩ
receiver propagation delay symmetry	t_{rx_sym}	-2		2	us	
LIN dominant wake-up time	$t_{wake(dom)LIN}$	30		150	us	Sleep mode
dominant wake-up time on pin WAKE_N	$t_{wake(dom)WAKE\_N}$	7		80	us	Sleep mode
go to normal time	$t_{gotonorm}$	2		15	us	time period for mode change from Sleep, Power-on or Standby mode into Normal mode
normal mode initialization time	$t_{init(norm)}$			20	us	normal mode, initialization time
go to sleep time	$t_{gotosleep}$	2		30	us	time period for mode change from Normal mode into Sleep mode
TXD dominant time-out time	$t_{to(dom)TXD}$	27		90	ms	V_{TXD} = 0 V

5.3.Parameter Measurement Information

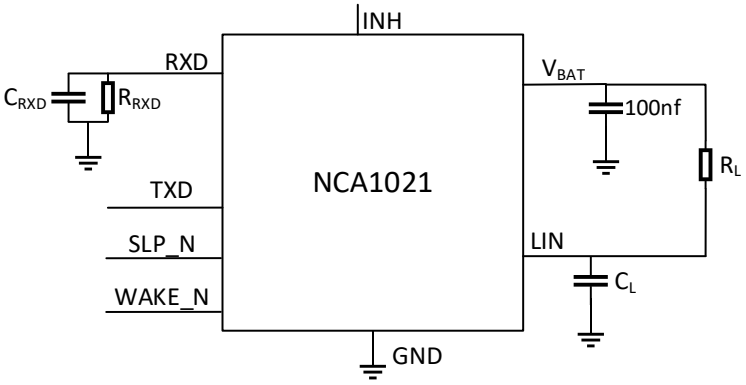


Figure 5.1. Timing test circuit for LIN transceiver

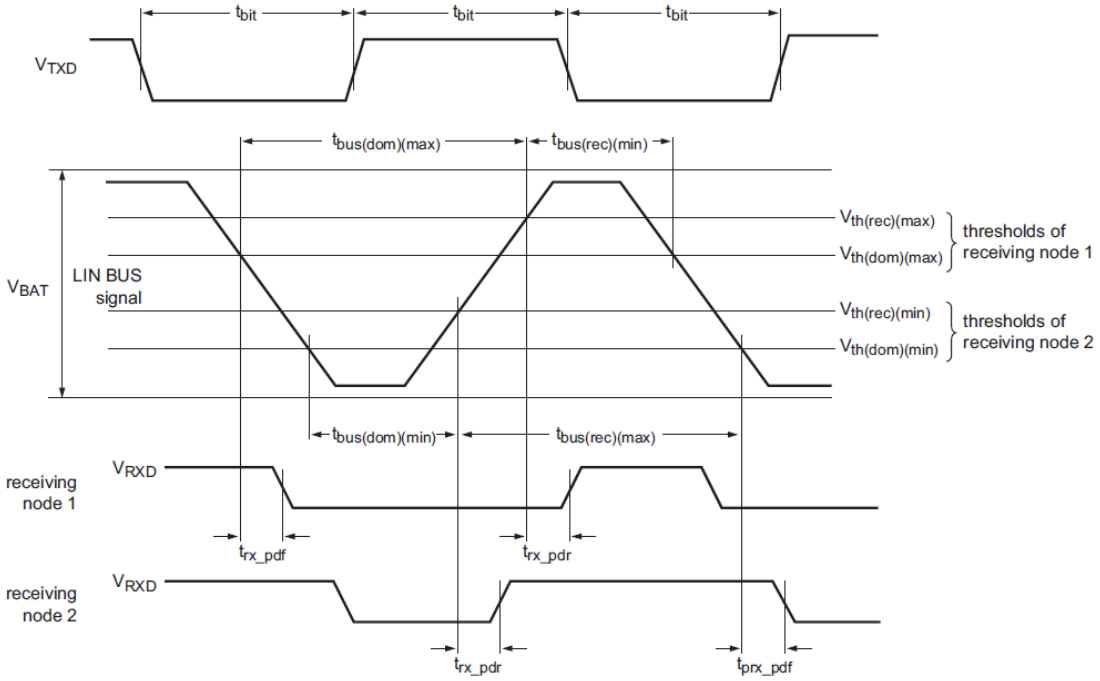


Figure 5.2. Timing diagram LIN transceiver

6. Function Description

6.1. Overview

The NCA1021 is a LIN transceiver with a low-power mode and multiple wake-up methods. The NCA1021 is fully compatible with the ISO 17987-4 standard. The NCA1021 is providing high electromagnetic immunity and low emissions. The data rate of the NCA1021 is up to 20Kbps. The NCA1021 provides thermal protection and transmit data dominant time out function.

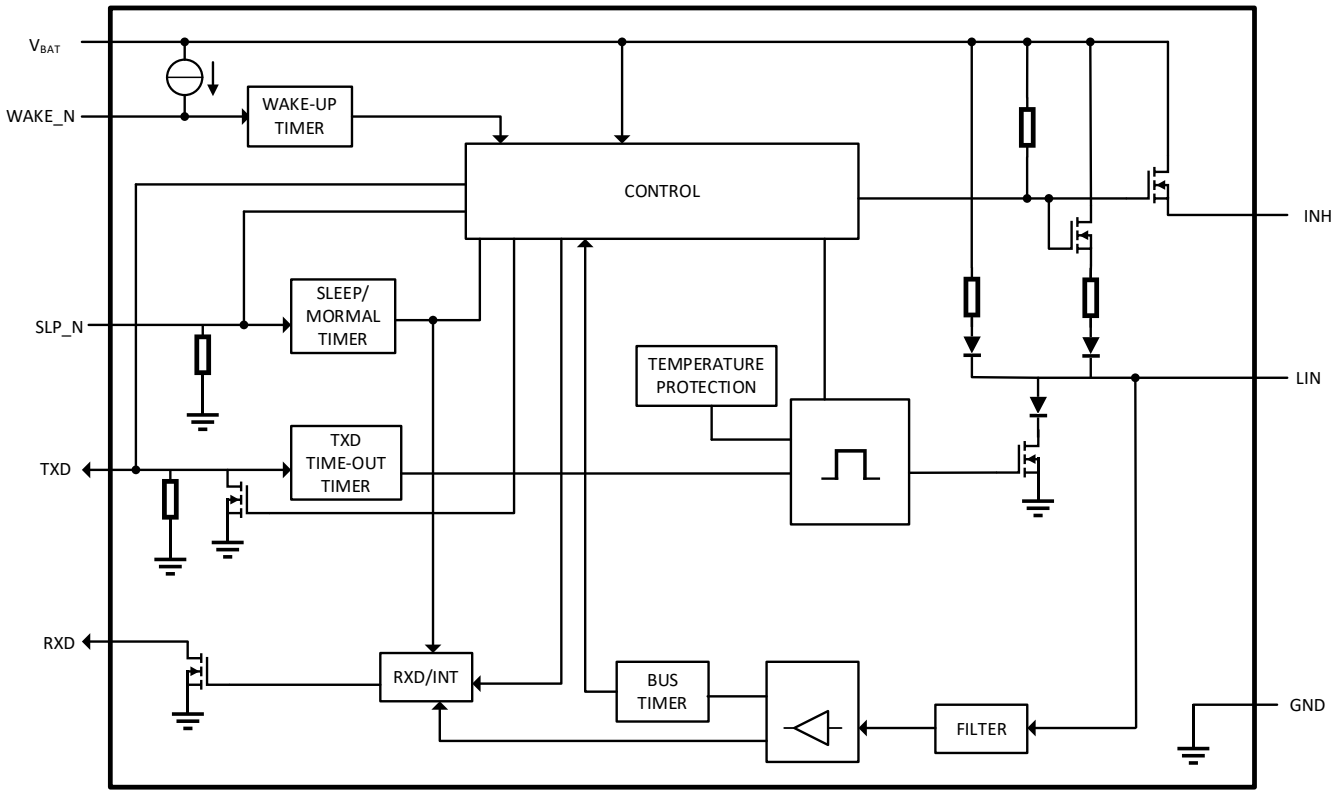


Figure6.1 Block diagram of NCA1021

6.2. Device Functional Modes

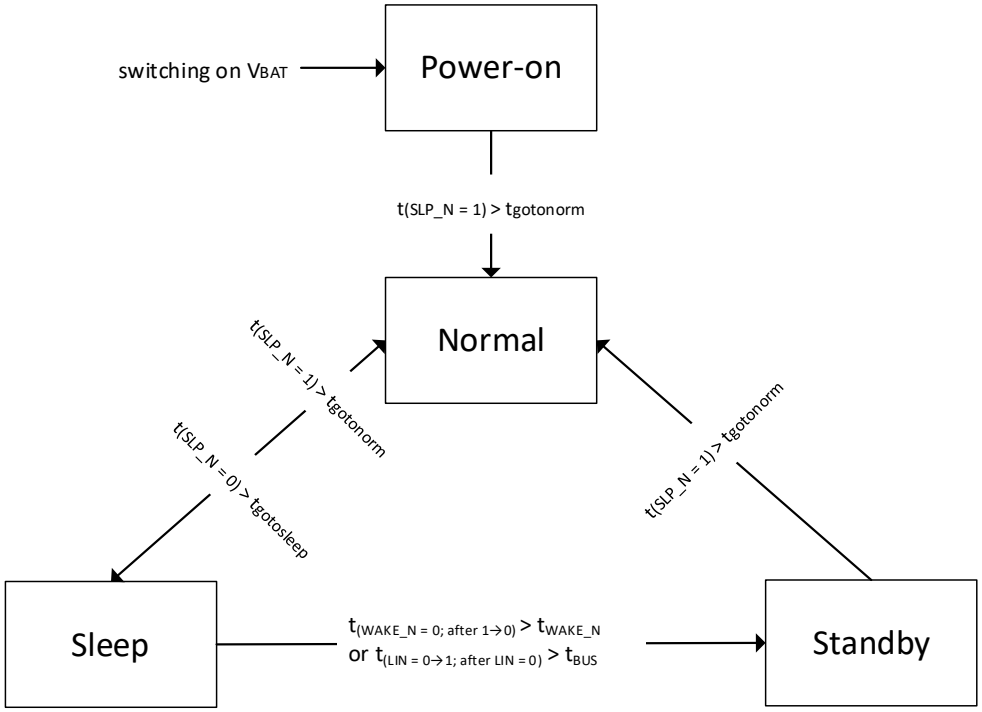


Figure 6.2 State diagram of NCA1021

Table 6.1. Function Table

Mode	*SLP_N*	*LIN*	*TXD (output)*	*RXD*	*INH*	*Transmitter*
Power-on	0	pull up by 30kohm	weak pull-down	floating	HIGH	Off
Normal[3]	1	pull up by 30kohm	HIGH: recessive state LOW: dominant state	HIGH: recessive state LOW: dominant state	HIGH	ON
Sleep	0	weak pull up	weak pull-down	floating	floating	Off
Standby	0	pull up by 30kohm	weak pull-down if remote wake-up strong pull-down if local wake-up[1]	LOW[2]	HIGH	Off

[1] The internal wake-up source flag (set if a local wake-up did occur and fed to pin TXD) will be reset after a positive edge on pin SLP_N.

[2] The wake-up interrupt (on pin RXD) is released after a positive edge on pin SLP_N.

[3] Normal mode is entered after a positive edge on SLP_N. If TXD is LOW, the transmitter is off. In the event of a short-circuit to ground on pin TXD, the transmitter will be disabled.

6.3. Normal mode

Under the normal mode of NCA1021, it can receive and send Normally on the LIN bus. In the Normal mode, the transmitter receives the signal from the MCU via the TXD, and first determines the dominant timeout, and then converts it into an optimized bus signal slew rate and waveform shaping to minimize EME. The LIN bus output is pulled HIGH via an internal slave termination resistor. The receiver detects the signal on the LIN bus input and transmits it to the microcontroller through the RXD. The recessive level on the bus is high and the dominant level is low.

After NCA1021 is powered on and $t_{(SLP\_N=1)} > t_{gotonorm}$, it will enter the Normal mode. If SLP_N=0, it will remain in Power-on mode. In Sleep mode or Standby mode, when $t_{(SLP\_N=1)} > t_{gotonorm}$, the Normal mode can be entered.

6.4. Sleep mode

Sleep mode is the lowest power consumption mode of NCA1021. In Sleep mode the transmitter is disabled, releasing the INH to floating state. LIN is in a weak current pull-up state, which can prevent false remote wake-up events. The only way to enter sleep mode is to make $t_{(SLP\_N=0)} > t_{gotosleep}$ in normal mode. The NCA1021 in sleep mode supports 3 different methods to wake up. They are wake-up remotely via LIN bus, and wake-up locally via SLP_N or WAKE_N.

6.5. Standby mode

When NCA1021 is in sleep mode, it will enter standby mode by local or remote wake-up by LIN bus or WAKE_N. In standby mode, the INH changes from floating to high, which can be used as a control flag for other devices. At the same time, the 30kΩ pull-up resistor between LIN and VBAT is reconnected. Standby mode is signaled by a Low-level on RXD which can be used as an interrupt for the microcontroller.

It should be noted that two different wake-up methods will cause different states of the TXD. After being remotely awakened by the LIN bus, TXD will be in a weak pull-down state. After being woken up locally by the WAKE_N, TXD will be in a strong pull-down state. Therefore, the status of TXD can be used as a basis for judging the wake-up mode.

In standby mode, set the SLP_N high ($t_{(SLP\_N=1)} > t_{gotonorm}$) to enter the normal mode. Release the state of TXD and RXD at this time.

6.6. TXD dominant time-out function

A TXD dominant time-out timer circuit prevents the bus line from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD. If the duration of the Low-level on pin TXD exceeds the internal timer value ($t_{to(dom)TXD}$), the transmitter is disabled, driving the bus line into a recessive state. The timer is reset by a positive edge on pin TXD.

6.7. Fail-safe features

Pin TXD provides a pull-down to GND to force a predefined level on input pin TXD in case the pin TXD is unsupplied.

Pin SLP_N provides a pull-down to GND to force the transceiver into Sleep mode in case the pin SLP_N is unsupplied.

Pin RXD is set floating in case of lost power supply on pin V_{BAT}.

The current of the transmitter output stage is limited to protect the transmitter against short circuit to pins VBAT or GND.

A loss of power (pins V_{BAT} and GND) has no impact on the bus line and the microcontroller. There are no reverse currents from the bus. The LIN transceiver can be disconnected from the power supply without influencing the LIN bus.

The output driver at pin LIN is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature $T_{j(sd)}$, the thermal protection circuit disables the output driver. The driver is enabled again when the junction temperature has dropped below $T_{j(sd)}$ and a recessive level is present at pin TXD.

If V_{BAT} drops below $V_{th(VBATL)L}$, a protection circuit disables the output driver. The driver is enabled again when $V_{BAT} > V_{th(VBATL)H}$ and a recessive level is present at pin TXD.

7. Application Note

7.1. Typical Application

The NCA1021 requires a 0.1 µF bypass capacitors between VCC and GND. The bypass capacitance value can also be determined according to the actual situation of the system. The capacitor should be placed as close as possible to the package. Master node applications require and external 1kΩ pullup resistor and serial diode. The LIN external capacitance value is selected according to the actual situation (refer to ISO 17987-4:2016 5.3.6 Line characteristics), generally 220pF for the slave or 1nF for the master. If RXD on the MCU does not have an internal pull-up, an external pull-up resistor is required. The figure7.1 is the basic schematic of NCA1021.

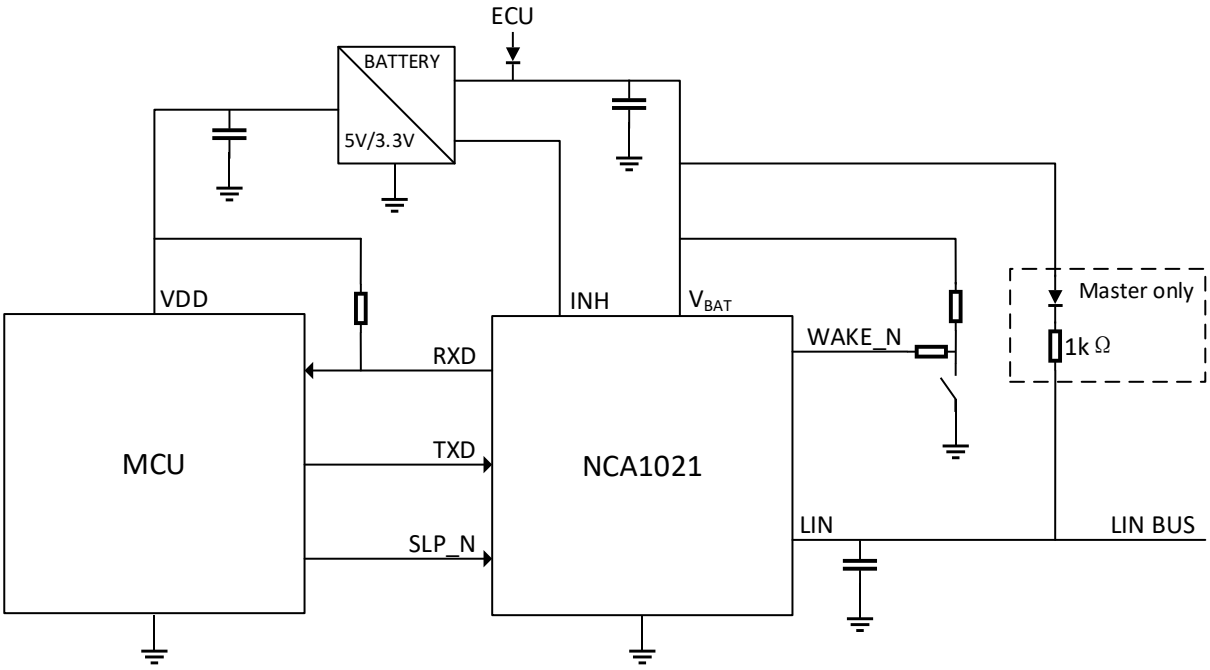
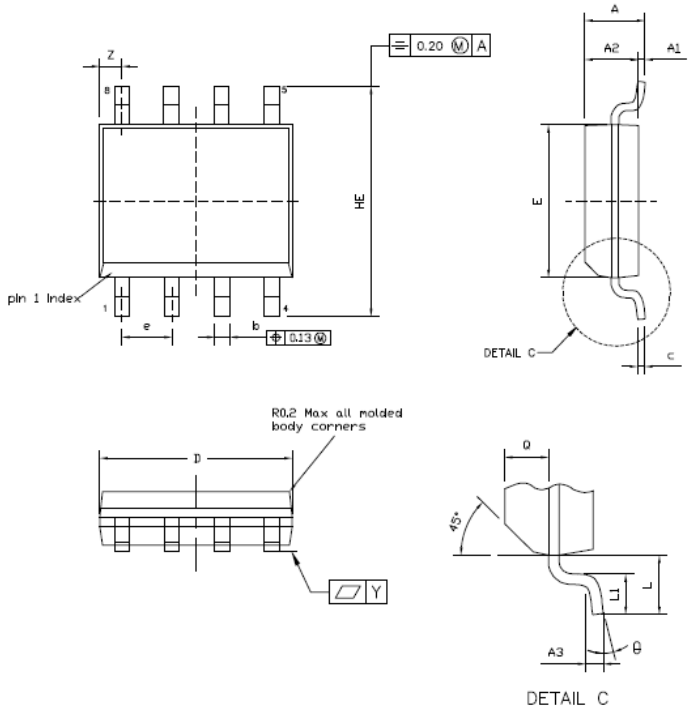


Figure 7.1 Basic schematic of NCA1021

8. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.75
A1	0.10	---	0.25
A2	1.25	1.35	1.45
b	0.33	0.38	0.49
c	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
Q	0.60	0.65	0.70
HE	5.80	6.00	6.20
e	1.27 BSC		
L	1.05 BSC		
L1	0.40	0.64	1.00
Y	---	0.10	---
Z	0.3	0.5	0.7
A3	0.25 BSC		
θ	0°	5°	8°

Figure 8.1 SOP8 Package Shape and Dimension in millimeters

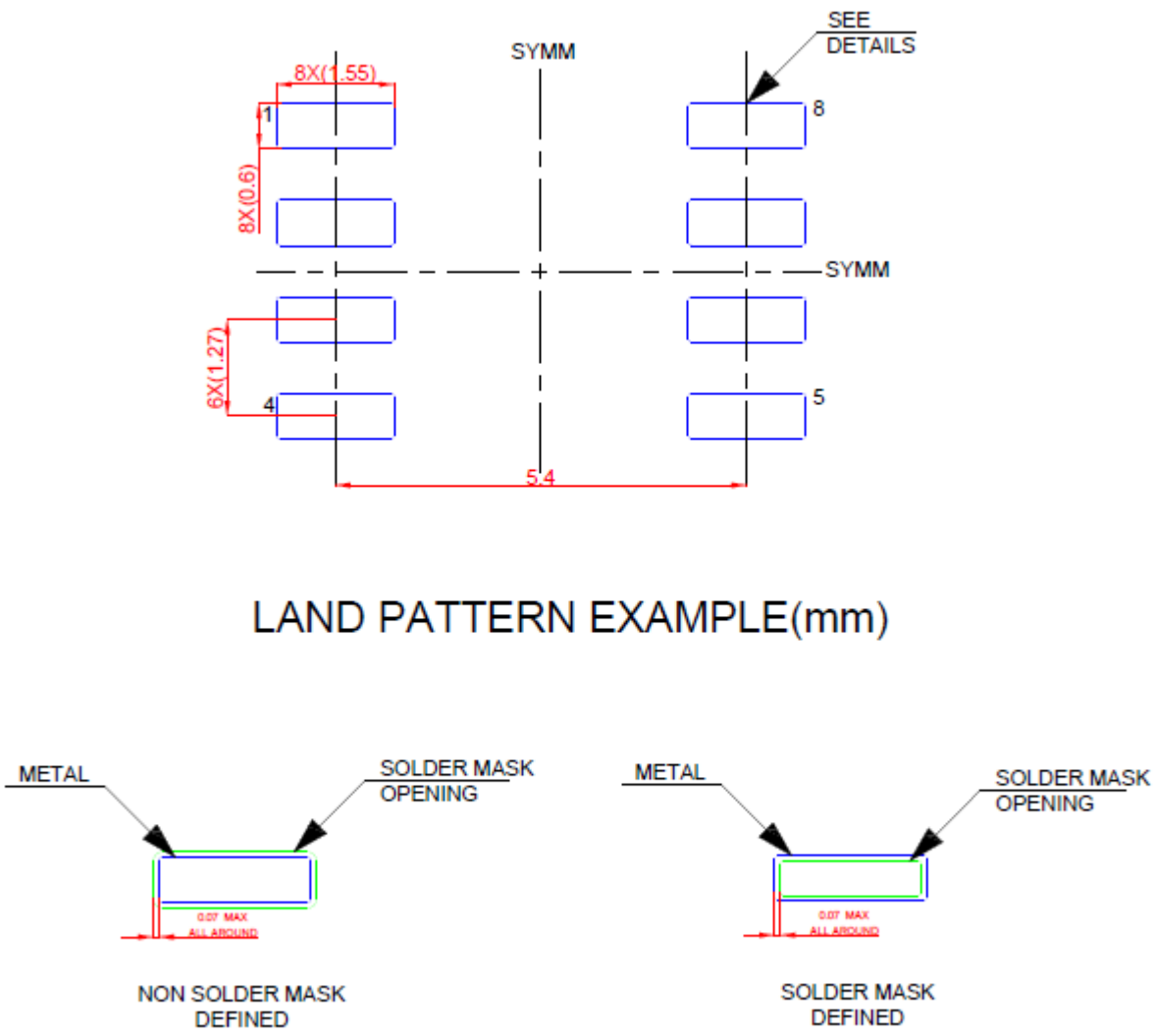
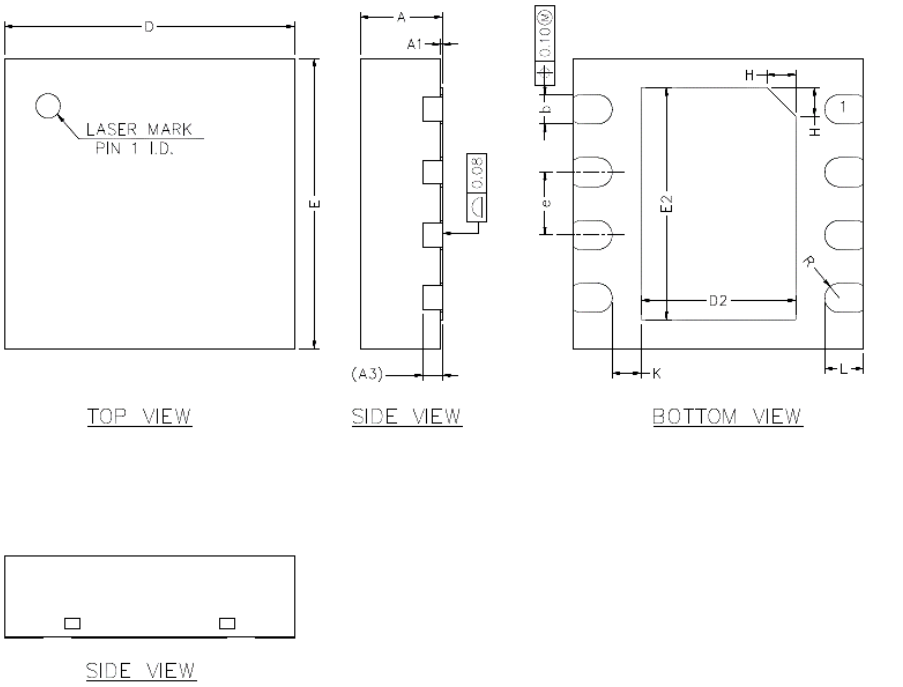


Figure 8.2 SOP8 Package Board Layout Example



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203REF	
b	0.25	0.30	0.35
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.50	1.60	1.70
E2	2.30	2.40	2.50
e	0.55	0.65	0.75
H		0.30REF	
K	0.20	0.30	0.40
L	0.35	0.40	0.45
R		0.15REF	

Figure 8.3 DFN8 Package Shape and Dimension in millimeters

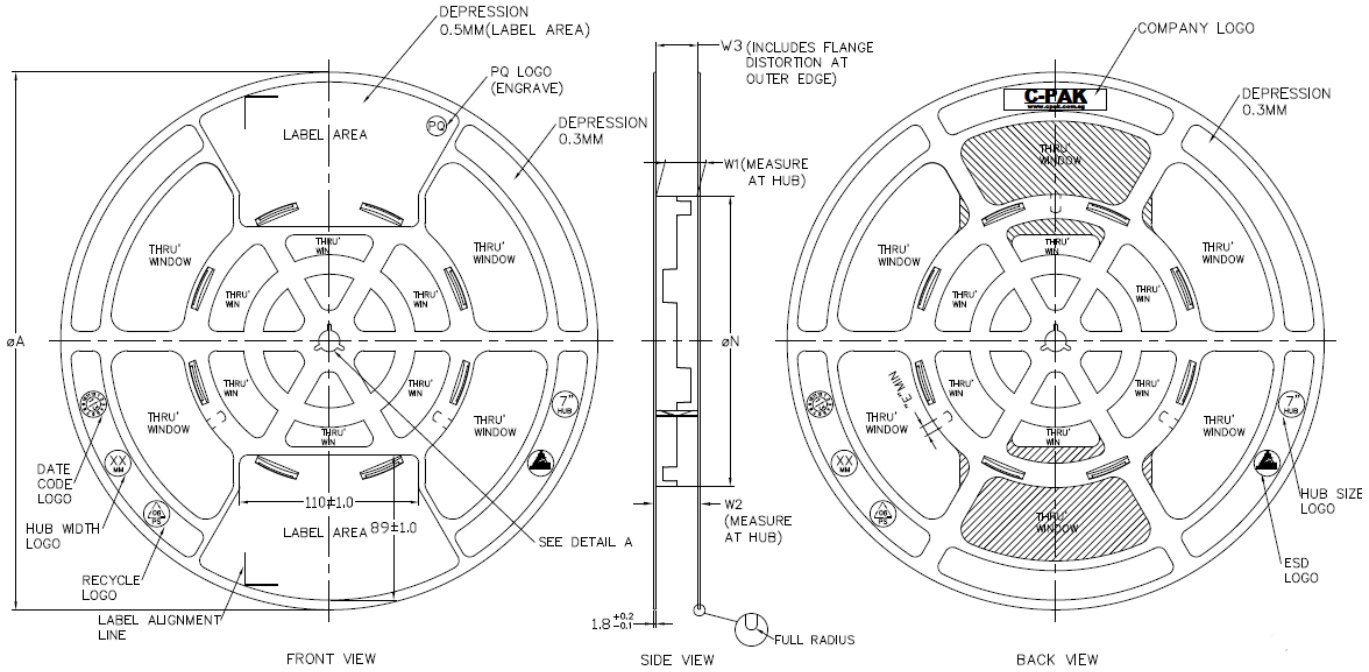
9. Order Information

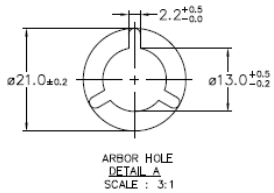
Part Number	*Max Data Rate (Kbps)*	*Junction Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NCA1021-Q1SPR	20	-40 to 150℃	1	SOP8(150mil)	SOP8	2500
NCA1021-Q1DNR	20	-40 to 150℃	1	DFN8	DFN8	3000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures. All devices are AEC-Q100 qualified.						

10. Documentation Support

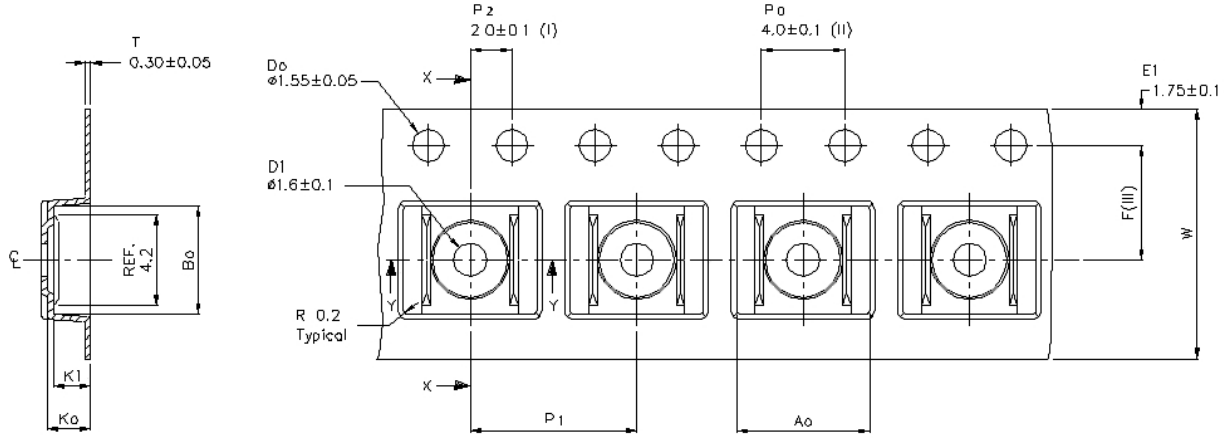
Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NCA1021	Click here	Click here	Click here	Click here

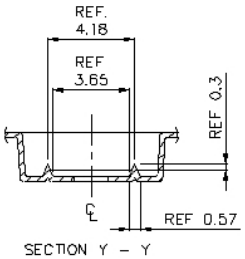
11. Tape and Reel Information





PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5





Ao	6.50	+/–	0.1
Bo	5.30	+/–	0.1
Ko	2.20	+/–	0.1
K1	1.90	+/–	0.1
F	5.50	+/–	0.1
P1	8.00	+/–	0.1
W	12.00	+/–	0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

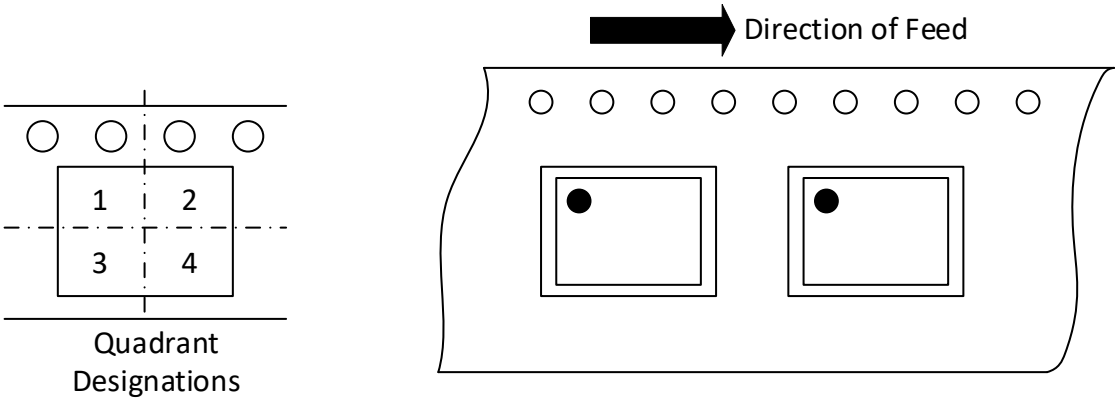
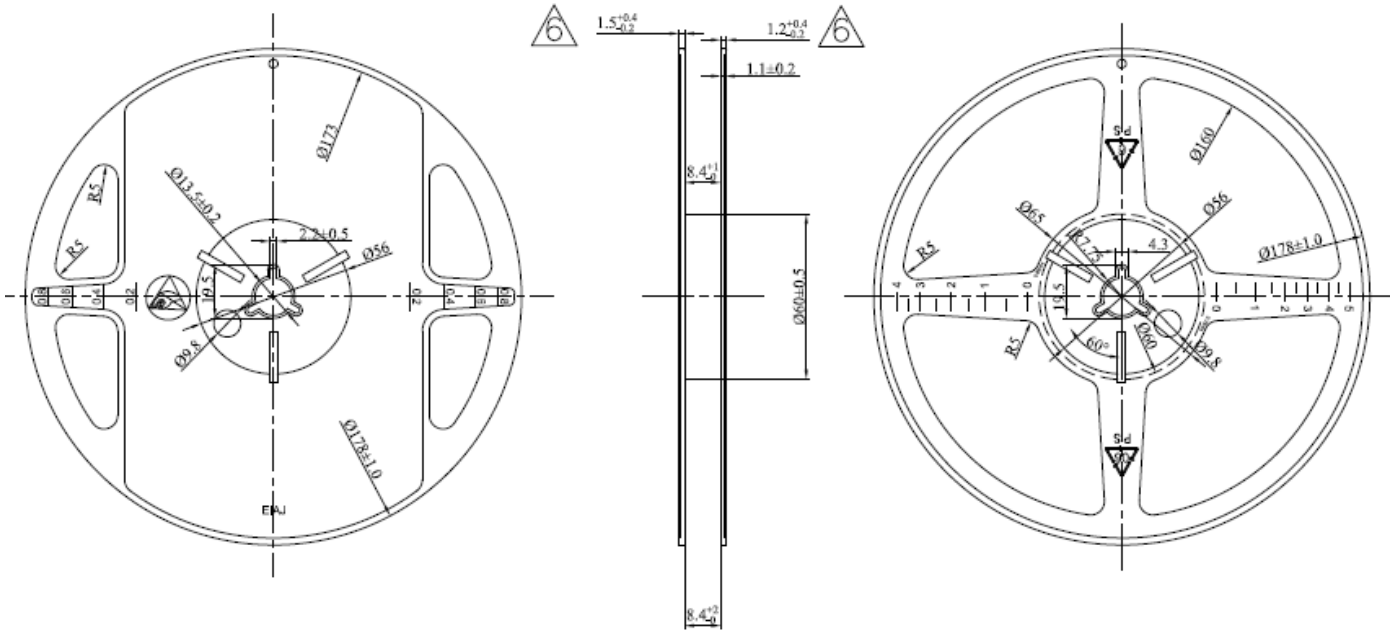


Figure 12.1 Tape and Reel Information of SOP8



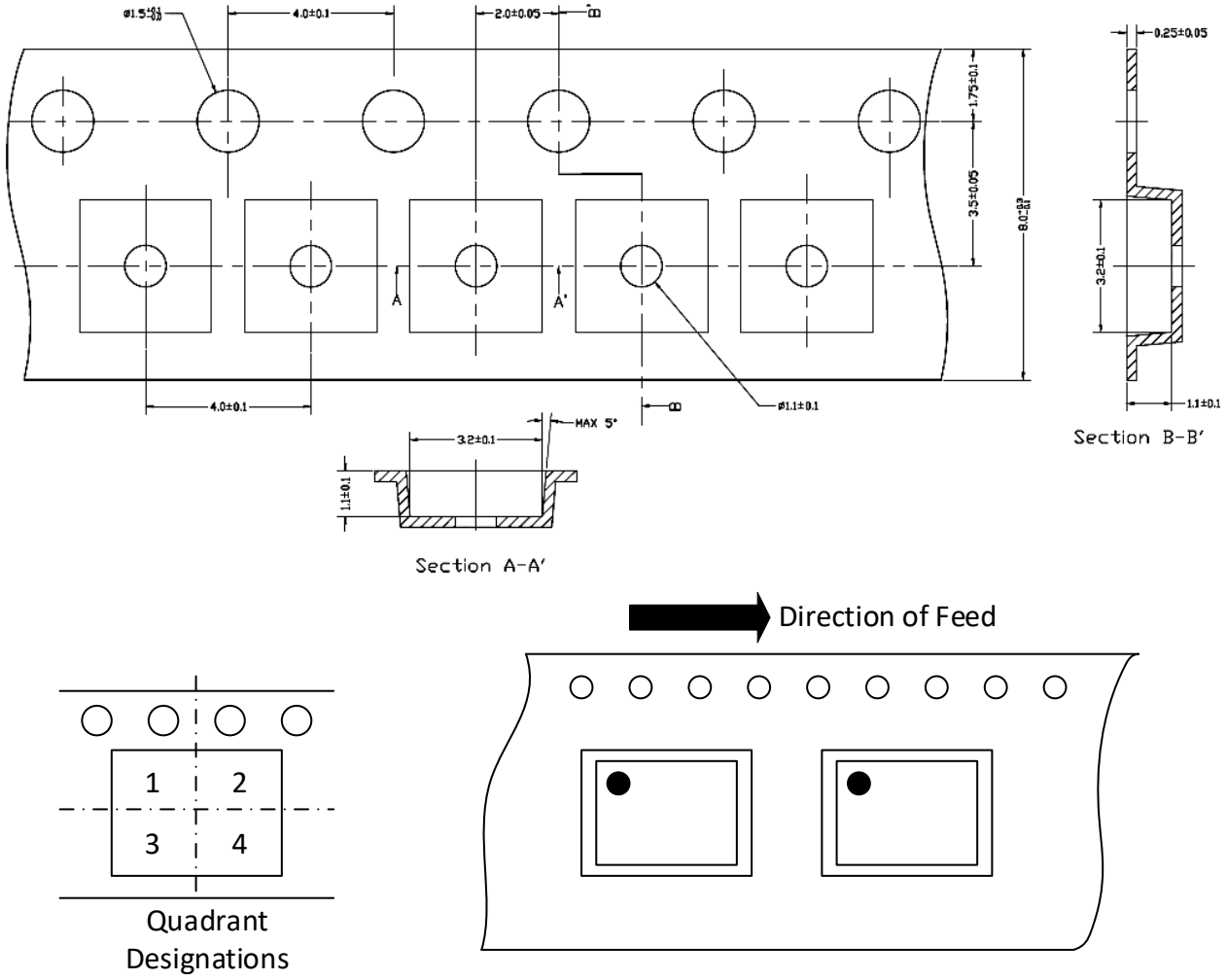


Figure 12.2 Tape and Reel Information of DFN8

12. Revision History

Revision	Description	Date
1.0	Initial version	2022/11/18

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party's intellectual property rights.

You are solely responsible for your use of Novosense' products and applications, and for the safety thereof. You shall comply with all laws, regulations and requirements related to Novosense's products and applications, although information or support related to any application may still be provided by Novosense.

The resources are intended only for skilled developers designing with Novosense' products. Novosense reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided. Novosense authorizes you to use these resources exclusively for the development of relevant applications designed to integrate Novosense's products. Using these resources for any other purpose, or any unauthorized reproduction or display of these resources is strictly prohibited. Novosense shall not be liable for any claims, damages, costs, losses or liabilities arising out of the use of these resources.

For further information on applications, products and technologies, please contact Novosense (www.novosns.com).

Suzhou Novosense Microelectronics Co., Ltd