

### Product Overview

NSE11409-Q1 is a 90mΩ low-side switch with 48V clamp voltage for automotive applications. It's designed for driving resistive or inductive loads with one side connected to the battery. Internal 48V clamp circuit protects device from surge energy when fast demagnetization at turn-off.

With internal output current limitation, the device is protected in overload condition. Built-in thermal shutdown protects the chip from over-temperature and short-circuit. A thermal swing mechanism is built to limit dissipated power to decelerate power accumulation. Thermal shutdown, with automatic restart, allows the devices to recover normal operation as soon as a fault condition disappears.

An internal diagnostic function is built to indicate any faults when thermal shutdown and open-drain conditions through an open-drain status output pin. This device operates in ambient temperatures from -40°C to 125°C.

### Key Features

- AEC-Q100 Qualified
- Drain current limitation: 8.5A
- 48V overvoltage clamp
- Thermal shutdown protection
- Thermal swing protection
- Fault diagnostic block:
  - Thermal shutdown diagnosis
  - Open-drain diagnosis
- Very low standby current
- Very low electromagnetic susceptibility
- ESD protection
- RoHS-compliant package

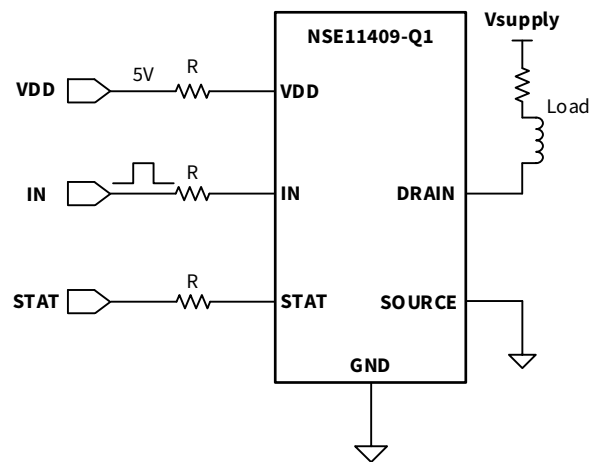
### Applications

- Automotive Relays
- Solenoids
- Valves
- Lighting

### Device Information

Part Number	Package	Body Size
NSE11409-QSPR	SOP8	4.9mm x 3.9mm
NSE11409-QSTBR	SOT223	6.48mm x 3.38mm

### Typical Application



**INDEX**

1. PIN CONFIGURATION AND FUNCTIONS ..... 3

2. BLOCK DIAGRAM ..... 3

3. ABSOLUTE MAXIMUM RATINGS ..... 4

4. ESD RATINGS ..... 4

5. THERMAL INFORMATION ..... 5

6. SPECIFICATIONS ..... 5

    6.1. ELECTRICAL CHARACTERISTICS ..... 5

    6.2. TYPICAL PERFORMANCE CHARACTERISTICS..... 7

        6.2.1. TRUE TABLE..... 7

        6.2.2. ELECTRICAL CHARACTERISTICS CURVES ..... 7

7. PROTECTIONS ..... 8

    7.1. CURRENT LIMITATION..... 8

    7.2. THERMAL SHUTDOWN AND THERMAL SWING..... 8

8. TYPICAL APPLICATION ..... 8

    8.1. APPLICATION CIRCUIT ..... 8

    8.2. MCU I/O PROTECTION..... 9

    8.3. THE VALUE OF STATUS PULL-UP RESISTOR ..... 9

    8.4. INDUCTIVE CLAMP ..... 10

9. LAYOUT ..... 11

    9.1. LAYOUT GUIDELINES ..... 11

    9.2. LAYOUT EXAMPLE ..... 11

10. PACKAGE INFORMATION..... 13

    10.1. SOP8..... 13

        10.1.1. TAPE AND REEL ..... 13

        10.1.2. MECHANICAL DATA..... 14

        10.1.3. RECOMMENDED LAND PATTERN..... 14

    10.2. SOT223..... 16

        10.2.1. TAPE AND REEL ..... 16

        10.2.2. MECHANICAL DATA..... 16

        10.2.3. RECOMMENDED LAND PATTERN..... 18

11. ORDER INFORMATION ..... 19

12. REVISION HISTORY ..... 19

### 1. Pin Configuration and Functions

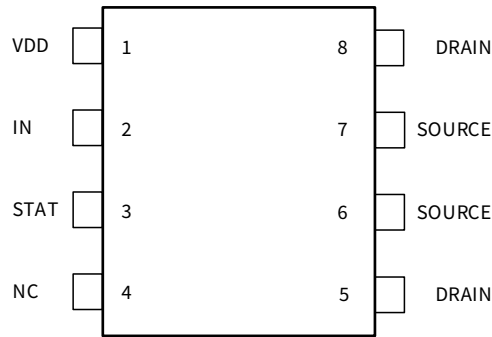


Figure 1 NSE11409-QSPR Pin-out

PIN NO.	SYMBOL	FUNCTION
1	VDD	Power supply pin.
2	IN	CMOS compatible, voltage controlled input pin.
3	STAT	Open drain digital diagnostic pin.
4	NC	Not connect.
5, 8	DRAIN	PowerMOS drain.
6, 7	SOURCE	PowerMOS source.

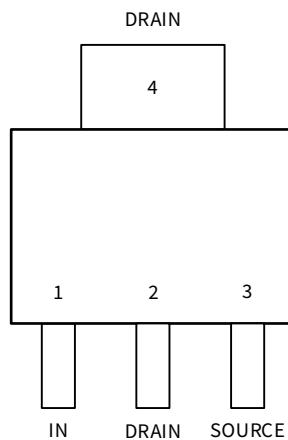


Figure 2 NSE11409-QSTBR Pin-out

PIN NO.	SYMBOL	FUNCTION
1	IN	CMOS compatible, voltage controlled input pin.
2, 4	DRAIN	PowerMOS drain.
3	SOURCE	PowerMOS source.

### 2. Block diagram

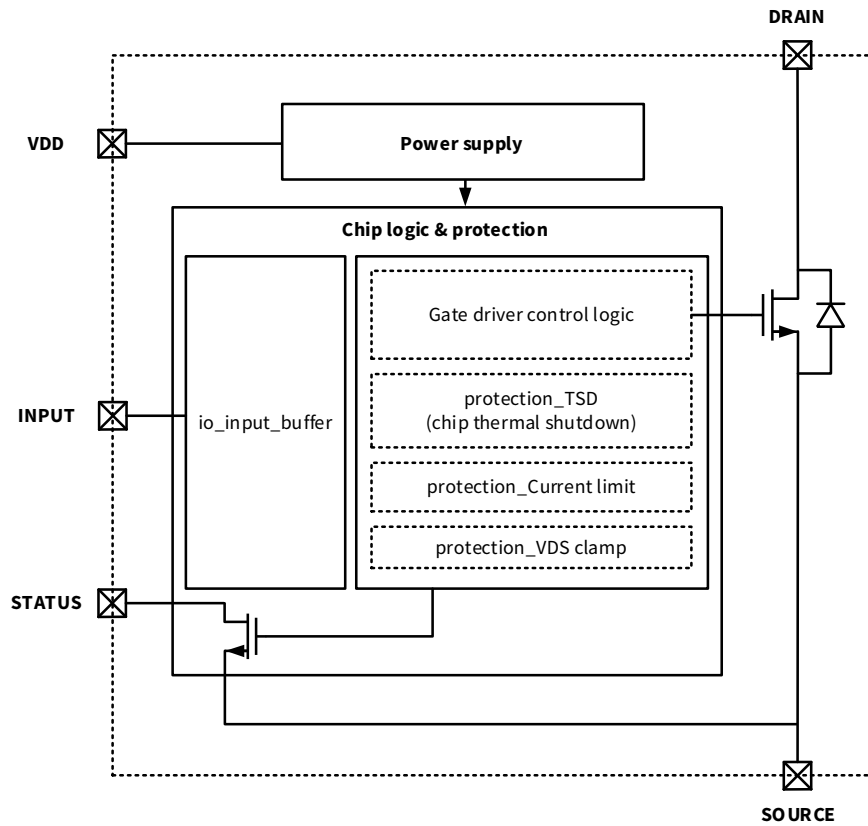


Figure 3 Block diagram

### 3. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Drain-to-Source Voltage	$V_{DS}$			Internally clamped	V
DC Drain Current	$I_D$			Thermal limited	A
Reverse DC drain current	$-I_D$			12.5	A
VDD Pin Current	$I_{VDD}$	-1		10	mA
INPUT Pin Current	$I_{IN}$	-1		10	mA
STATUS Pin Current	$I_{STAT}$	-1		10	mA
Junction Temperature	$T_J$	-40		150	°C
Storage Temperature	$T_{stg}$	-55		150	°C
Single pulse avalanche energy ( $L=90mH, I_{DS}=1.5A, V_{CC}=13.5V$ )	$E_{as}$		73 <sup>(1)</sup>		mJ

(1) Not subject to production test, bench evaluation.

### 4. ESD Ratings

Parameters	Symbol	Value	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), per AEC-Q100-002-RevD	± 3000	V
	Charged device model (CDM), per AEC-Q100-011-RevB	± 2000	V

## 5. Thermal Information

Parameters	Symbol	SOP8	SOT223	Unit
IC Junction-to-ambient Thermal Resistance <sup>(1)</sup>	$\theta_{JA}$	94.5	73	°C/W

(1) The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, four layer board.

## 6. Specifications

### 6.1. Electrical Characteristics

$V_{DD} = V_{IN} = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40\text{ °C to }125\text{ °C}$ . Unless otherwise noted, typical value is at  $T_A = 25\text{ °C}$ .

Parameters	Symbol	Min	Typ	Max	Unit	Comments
<b>Power MOSFET</b>						
ON-state resistance	$R_{ON}$		90	180	mΩ	$I_D = 1.6\text{ A}$ ; $V_{DD} = V_{IN} = 5\text{ V}$
Drain-source clamp voltage	$V_{CLAMP}$	46	48	56	V	$V_{IN} = 0\text{ V}$ ; $I_D = 1.6\text{ A}$
Drain-source clamp threshold voltage	$V_{CLTH}$	40			V	$V_{IN} = 0\text{ V}$ ; $I_D = 2\text{ mA}$
OFF-state output current	$I_{DSS}$	0		3	μA	$V_{IN} = 0\text{ V}$ ; $V_{DS} = 13\text{ V}$ ; $T_j = 25\text{ °C}$
		0		5	μA	$V_{IN} = 0\text{ V}$ ; $V_{DS} = 13\text{ V}$ ; $T_j = 125\text{ °C}$
Bode diode forward voltage	$V_{BD}$		0.8		V	$I_D = 1.6\text{ A}$ ; $V_{IN} = 0\text{ V}$
<b>VDD ( NSE11409-QSTBR supplied by pin IN )</b>						
Operating supply voltage	$V_S$	3.5	5	5.5	V	
Operating supply current	$I_S$		10	25	μA	OFF-state; $T_j = 25\text{ °C}$ ; $V_{IN} = V_{DS} = 0\text{ V}$ ;
			25	65		ON-state; $V_{IN} = 5\text{ V}$ ; $V_{DS} = 0\text{ V}$
Supply clamp voltage	$V_{SCL}$	5.5		8	V	$I_{SCL} = 1\text{ mA}$
			-0.7			$I_{SCL} = -1\text{ mA}$
<b>Logic Input ( NSE11409-QSPR only )</b>						
Low-level input voltage	$V_{IL}$			0.9	V	
Low-level input current	$I_{IL}$	1			μA	$V_{IN} = 0.9\text{ V}$
High-level input voltage	$V_{IH}$	2.1			V	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
High-level input current	$I_{IH}$			10	$\mu\text{A}$	$V_{IN} = 2.1\text{ V}$
Input hysteresis voltage	$V_{I(hyst)}$	0.13			V	
Input clamp voltage	$V_{ICL}$	5.5		8		$I_{IN} = 1\text{ mA}$
			-0.7			$I_{IN} = -1\text{ mA}$
<b>Status indicator (NSE11409-QSPR only)</b>						
Status low output voltage	$V_{STAT}$			0.5	V	$I_{STAT} = 1\text{ mA}$
Status leakage current	$I_{LSTAT}$			10	$\mu\text{A}$	$V_{STAT} = 5\text{ V}$
Status pin input capacitance	$C_{STAT}$			100	pF	$V_{STAT} = 5\text{ V}$
Status clamp voltage	$V_{STCT}$	5.5		8	V	$I_{STAT} = 1\text{ mA}$
			-0.7			$I_{STAT} = -1\text{ mA}$
<b>Open load detection (NSE11409-QSPR only)</b>						
Open load OFF-state voltage detection threshold	$V_{OI}$	1.1	1.2	1.3	V	$V_{IN} = 0\text{ V}$
Delay between INPUT falling edge and STATUS falling edge in open load condition	$t_{d(STAT)}$		225		$\mu\text{s}$	$I_{OUT} = 0\text{ A}$
<b>Switching characteristics (<math>V_{supply} = V_{IN} = 3.5\text{ V}</math> to <math>5.5\text{ V}</math>, See Figure 4 for Switching timing characteristics)</b>						
Turn-on delay time	$t_{d(ON)}$		8		$\mu\text{s}$	$R_L = 8.2\ \Omega; V_{CC} = 13\text{ V}$
Turn-off delay time	$t_{d(OFF)}$		18		$\mu\text{s}$	$R_L = 8.2\ \Omega; V_{CC} = 13\text{ V}$
Rise time	$t_r$		10		$\mu\text{s}$	$R_L = 8.2\ \Omega; V_{CC} = 13\text{ V}$
Fall time	$t_f$		10		$\mu\text{s}$	$R_L = 8.2\ \Omega; V_{CC} = 13\text{ V}$
Switching energy losses at turn-on	$W_{ON}$		57		$\mu\text{J}$	$R_L = 8.2\ \Omega; V_{CC} = 13\text{ V}$
Switching energy losses at turn-off	$W_{OFF}$		55		$\mu\text{J}$	$R_L = 8.2\ \Omega; V_{CC} = 13\text{ V}$
<b>Protection and diagnostics</b>						
DC short-circuit current	$I_{limH}$	5.5	8.5	11.5	A	$V_{DS} = 13\text{ V}; V_S = V_{IN} = 5\text{ V}$
Shutdown temperature	$T_{TSD}$	150	175	200	$^{\circ}\text{C}$	
Reset temperature	$T_R$	$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}\text{C}$	
Thermal reset of STATUS	$T_{RS}$	135			$^{\circ}\text{C}$	
Thermal hysteresis (TTSD - TR)	$T_{HYST}$		7		$^{\circ}\text{C}$	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Dynamic temperature	$\Delta T_j$		40		K	$T_j = -40^\circ\text{C}; V_{CC} = 13\text{V}$
Dynamic temperature hysteresis	$\Delta T_{j(\text{HYS})}$		15		K	

## 6.2. Typical Performance Characteristics

### 6.2.1. True table

Conditions	Input	Drain	Status
Normal operation	L	H	H
	H	L	H
Current limitation	L	H	H
	H	X	H
Over-temperature limitation	L	H	H
	H	H	L
$V_{DD}$ under-voltage	L	H	X
	H	H	X
Open-drain detection	L	L	L
	H	L	H

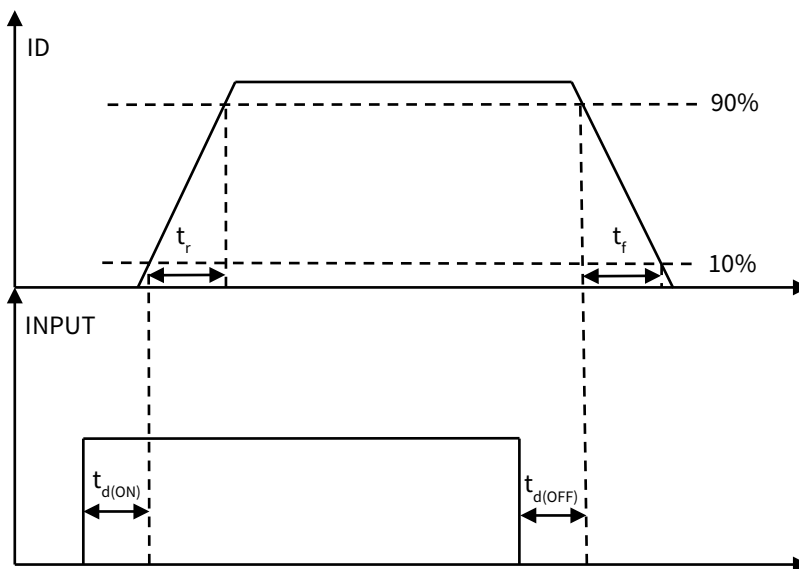


Figure 4 Switching characteristics

### 6.2.2. Electrical characteristics curves

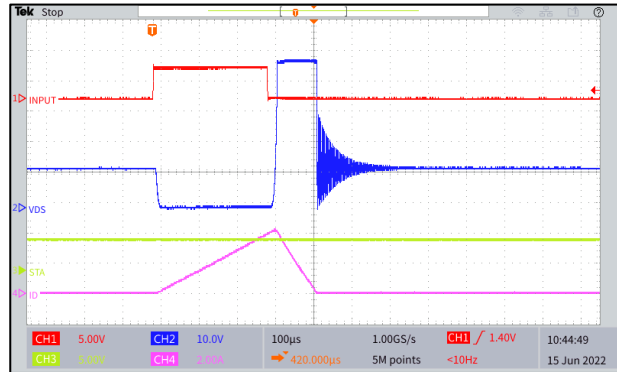


Figure 5 Inductive clamp voltage

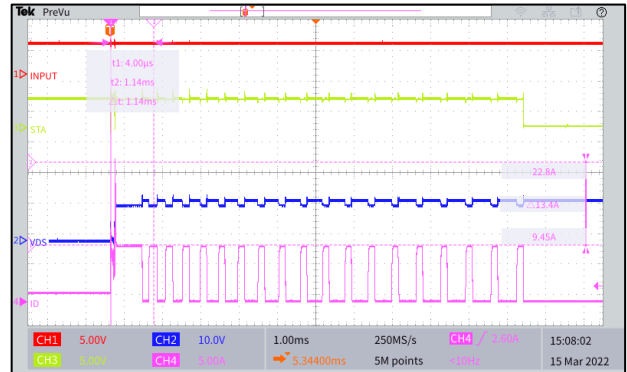


Figure 6 Thermal swing & current limitation

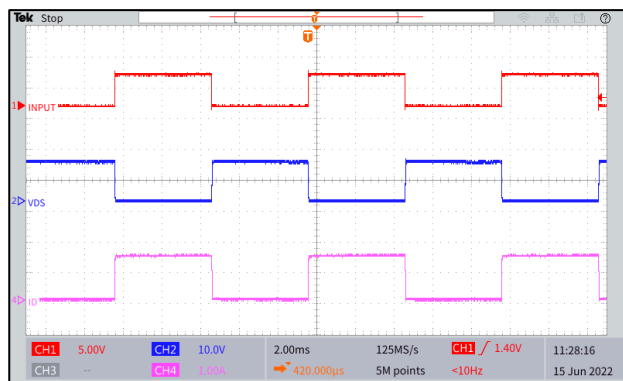


Figure 7 Normal load (1.5A,  $R_{load}$ , 25°C)

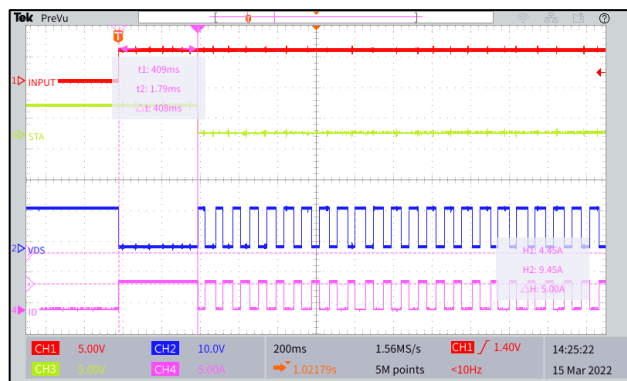


Figure 8 Thermal shutdown (5A,  $R_{load}$ , 85°C)

## 7. Protections

### 7.1. Current limitation

NSE11409-Q1 has current limitation to protect the silicon and bonding wire in case of overload or short circuit to ground.

### 7.2. Thermal shutdown and thermal swing

This device has both absolute and dynamic temperature protection. There are two thermal sensors on the controller and the MOSFET, the one on the MOSFET is the hottest and the one on the controller is the coldest. The absolute temperature protection is to shutdown the MOSFET when the hottest junction temperature exceeds the  $T_{SD}$ , and the dynamic temperature protection is also to shutdown the MOSFET when the temperature difference between the hottest and the coldest exceeds  $\Delta T_j$ .

## 8. Typical Application

### 8.1. Application Circuit



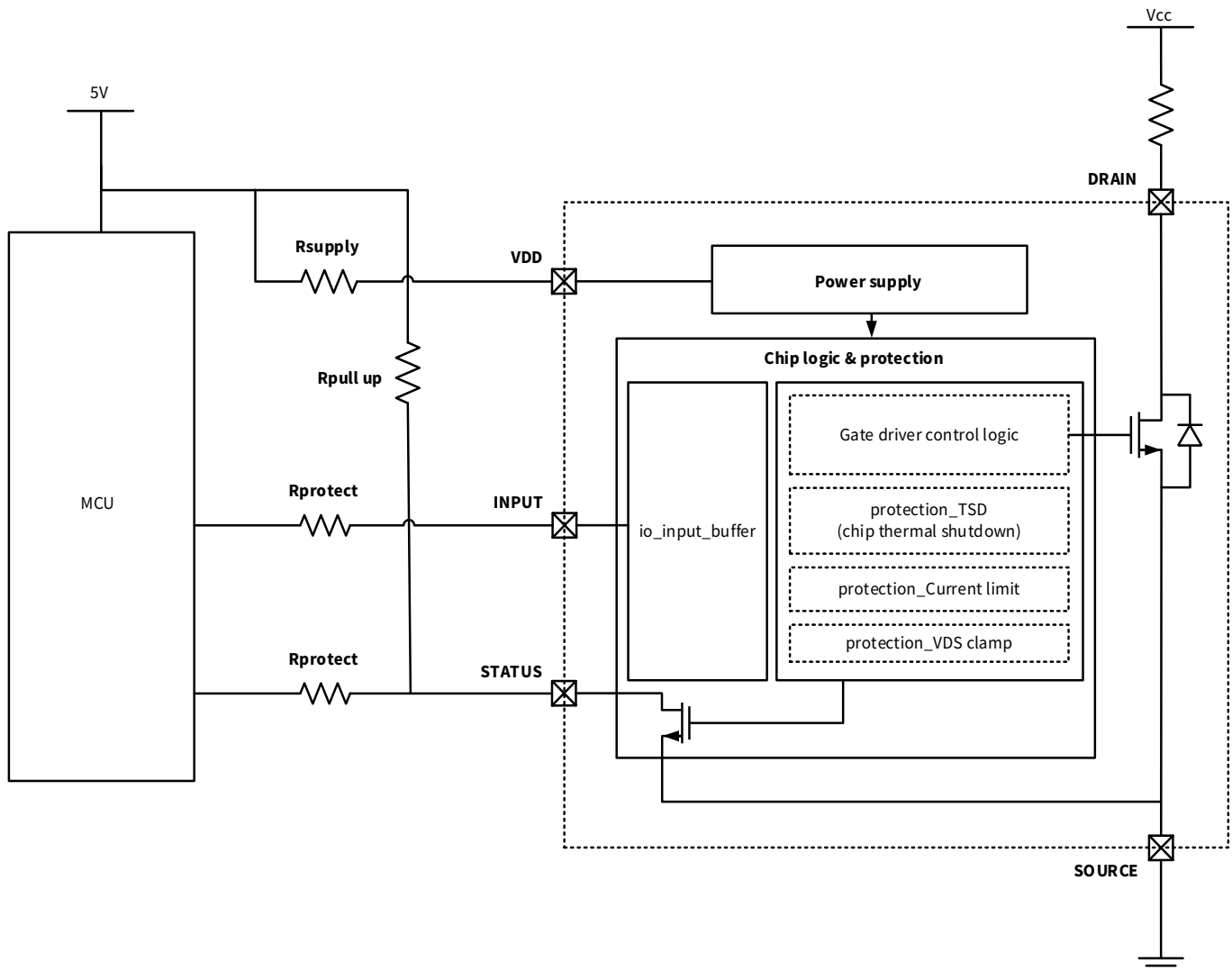


Figure 9 Typical application circuit of NSE11409-Q1

## 8.2. MCU I/O protection

NSE11409-Q1 has Zener diodes inside for ESD protection and the intrinsic NPN parasitic bipolar, so that resistors for protection are necessary in series with the digital inputs to limit the current to protect MCU I/Os during transient and reverse battery conditions.

The value of resistors for protection can be calculated by the formula as shown below:

$$\frac{V_{ICL}}{I_{latchup}} \leq R_{prot} \leq \frac{V_{MCU\_OUT} - V_{IH}}{I_{IH\ max}}$$

Where  $V_{ICL}$  is reverse clamp voltage of NSE11409-Q1,  $I_{latchup}$  is the MCU I/O latch up current,  $V_{MCU\_OUT}$  is the output voltage of MCU I/O,  $V_{IH}$  is the High-level input voltage of NSE11409-Q1,  $I_{IH}$  is the high level input current.

Let:

$I_{latchup} \geq 20\text{mA}$ ;  $V_{MCU\_OUT} \geq 4.5\text{V}$ , so  $35\Omega \leq R_{prot} \leq 100\text{k}\Omega$ . The recommended value is 1kΩ. The supply resistor is the same.

## 8.3. The value of STATUS pull-up resistor

Because the STATUS pin is open drain output, a pull up resistor is needed to fix the high voltage during normal operation. When the fault occurs, the voltage level of STATUS is pulled down by the internal MOSFET on. The value of pull-up resistor can be calculated by the formula as shown below:

$$\left(\frac{V_{pull-up}}{V_{OL}} - 1\right) R_{on} < R_{pull-up} < \frac{V_{pull-up} - V_{OH}}{I_{leak}}$$

Where  $V_{pull-up}$  is the minimum of pull-up supply,  $V_{OL}$  is the maximum of MCU logic low,  $R_{on}$  is the on resistance of the MOSFET of STATUS pin,  $V_{OH}$  is the minimum of MCU logic high,  $I_{leak}$  is the maximum leakage current of STATUS pin.

Let:

$$V_{pullup} = 4.5V; R_{on} = V_{STAT}/I_{STAT} = 500\Omega; V_{OL} = 0.9V; V_{OH} = 2.1V; I_{leak} = 10\mu A, \text{ so } 2k\Omega \leq R_{pull-up} \leq 240k\Omega.$$

### 8.4. Inductive clamp

When the LSS is turned off while driving the inductive load, due to the energy stored on the inductor during the ON time, this energy needs to be dissipated through LSS without an external freewheeling diode. At this point, the inductor will pull the output voltage to a negative voltage. In order to prevent the drain and source terminals of the MOS from exceeding the breakdown voltage of MOS due to excessive voltage,  $V_{DS}$  clamps are needed to protect the MOS.

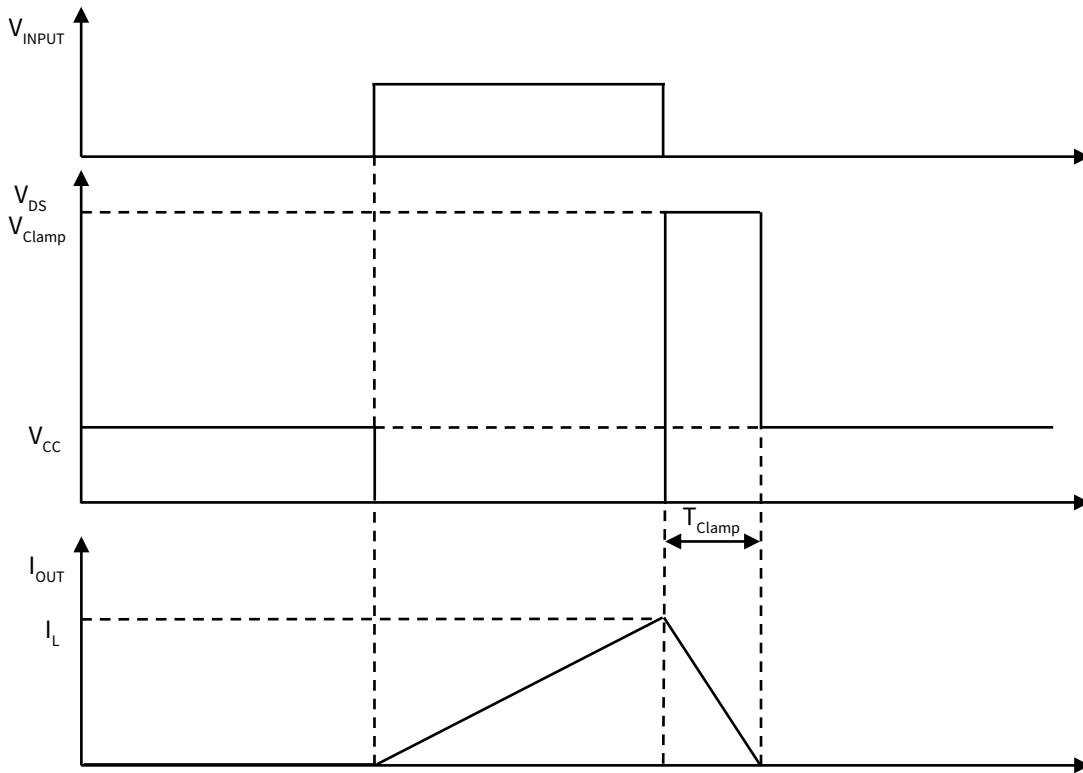


Figure 10 Switching characteristics of inductive load

The formula for calculating clamping energy is derived as follows, assuming that the inductance value is  $L$ , low side switch opens for a period of time, the current on  $L$  rises to  $I_L$  (less than inductance Saturation current), the energy stored on the inductor is:

$$E_L = \frac{1}{2} \cdot L \cdot I_L^2$$

$$V_{clamp} - V_{CC} = -L \frac{di}{dt}$$

$$di = -\frac{V_{clamp} - V_{CC}}{L} dt$$

$$i = I_L - \left(\frac{V_{clamp} - V_{CC}}{L}\right)t$$

$$E = \int_0^{t_{clamp}} i \times V_{clamp} dt = \int_0^{t_{clamp}} \left(I_L - \left(\frac{V_{clamp} - V_{CC}}{L}\right)t\right) \times V_{clamp} dt = [I_L \times V_{clamp} \times t - \frac{1}{2} \left(\frac{V_{clamp} - V_{CC}}{L}\right) \times V_{clamp} \times t^2]_0^{t_{clamp}}$$

Where,

$$t_{clamp} = \frac{L \times I_L}{V_{clamp} - V_{CC}}$$

So that:

$$E = \frac{1}{2} \cdot I_L^2 \cdot L \cdot \frac{V_{clamp}}{V_{clamp} - V_{CC}}$$

For better working reliability, a diode (e.g. 40V, 1A or 2A) could be placed in reverse parallel with the inductor according to the actual load current. Figure 11 shows the recommended application circuit for inductive loads of NSE11409.

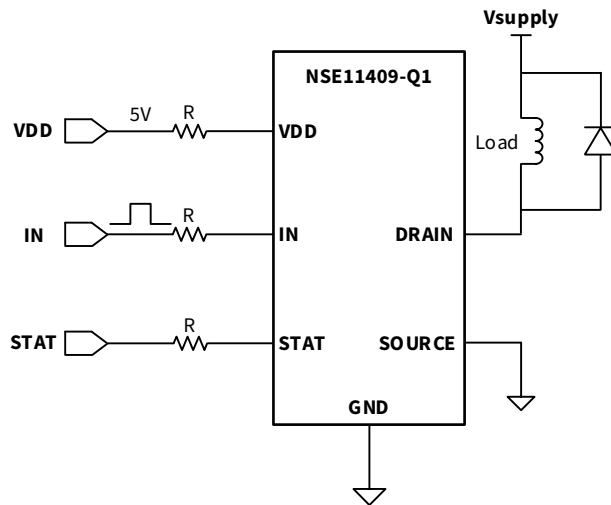


Figure 11 Recommended application circuit for inductive loads of NSE11409

## 9. Layout

### 9.1. Layout Guidelines

Both drain and source traces should be wide enough for better heat dissipation, via arrays are recommended to connect multiple layers to improve thermal performance.

### 9.2. Layout Example

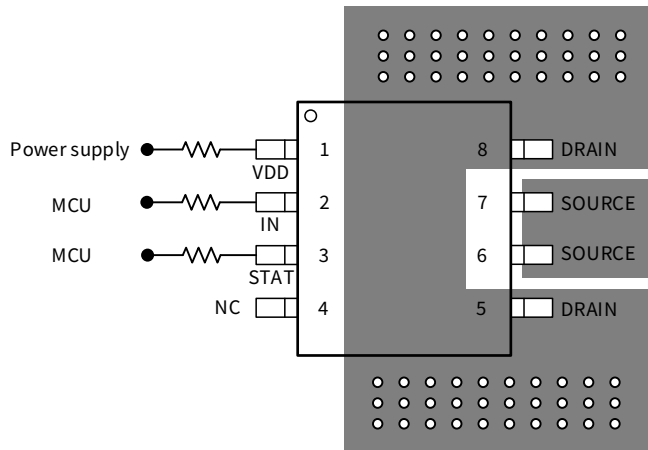


Figure 12 SOP8 Layout Example

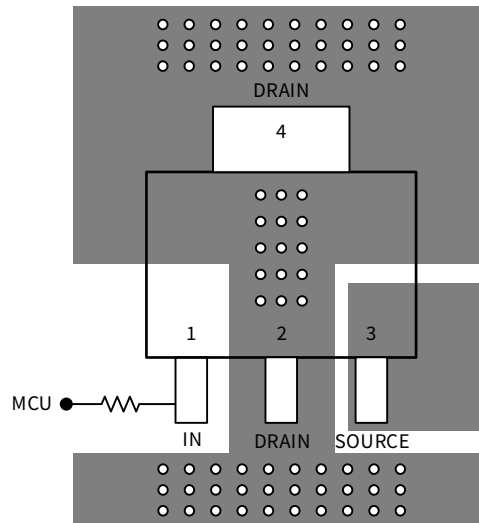
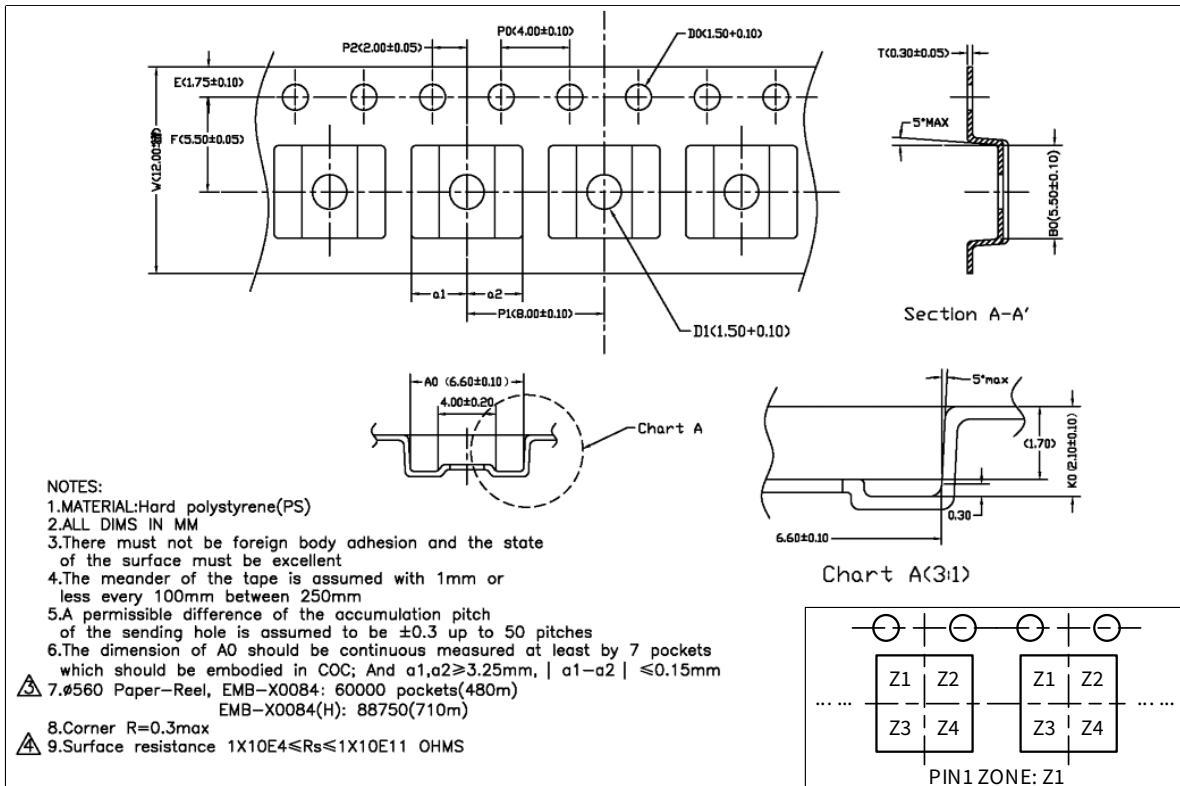
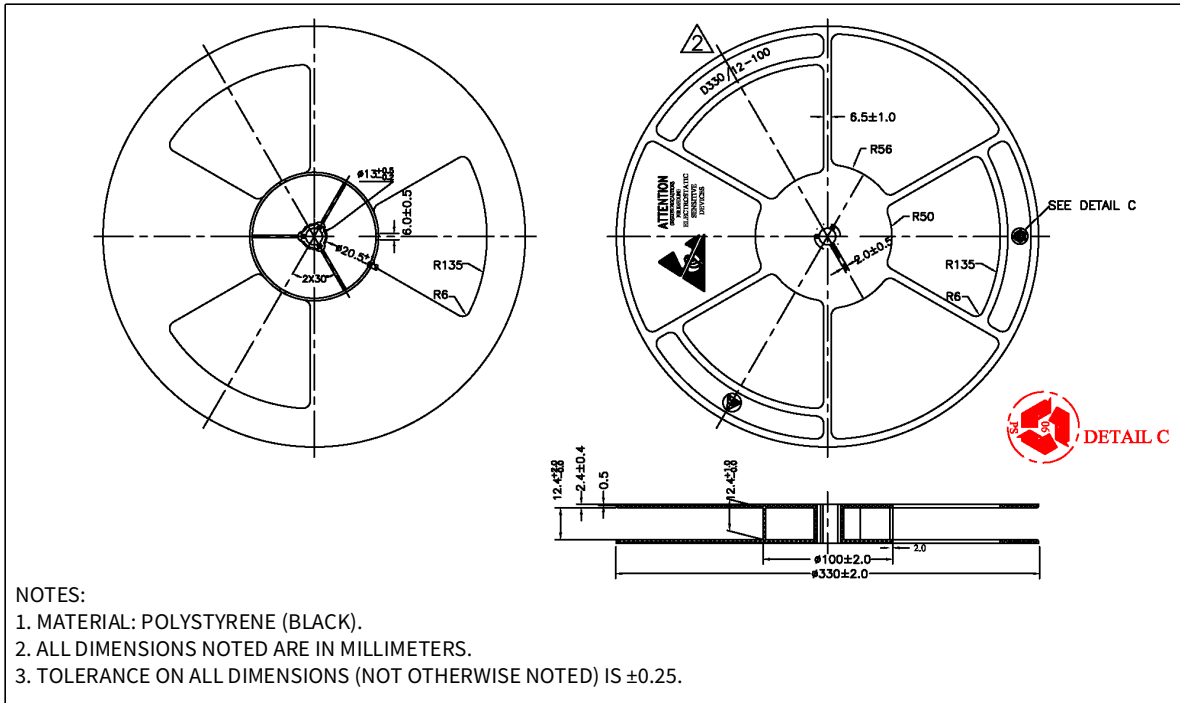


Figure 13 SOT223 Layout Example

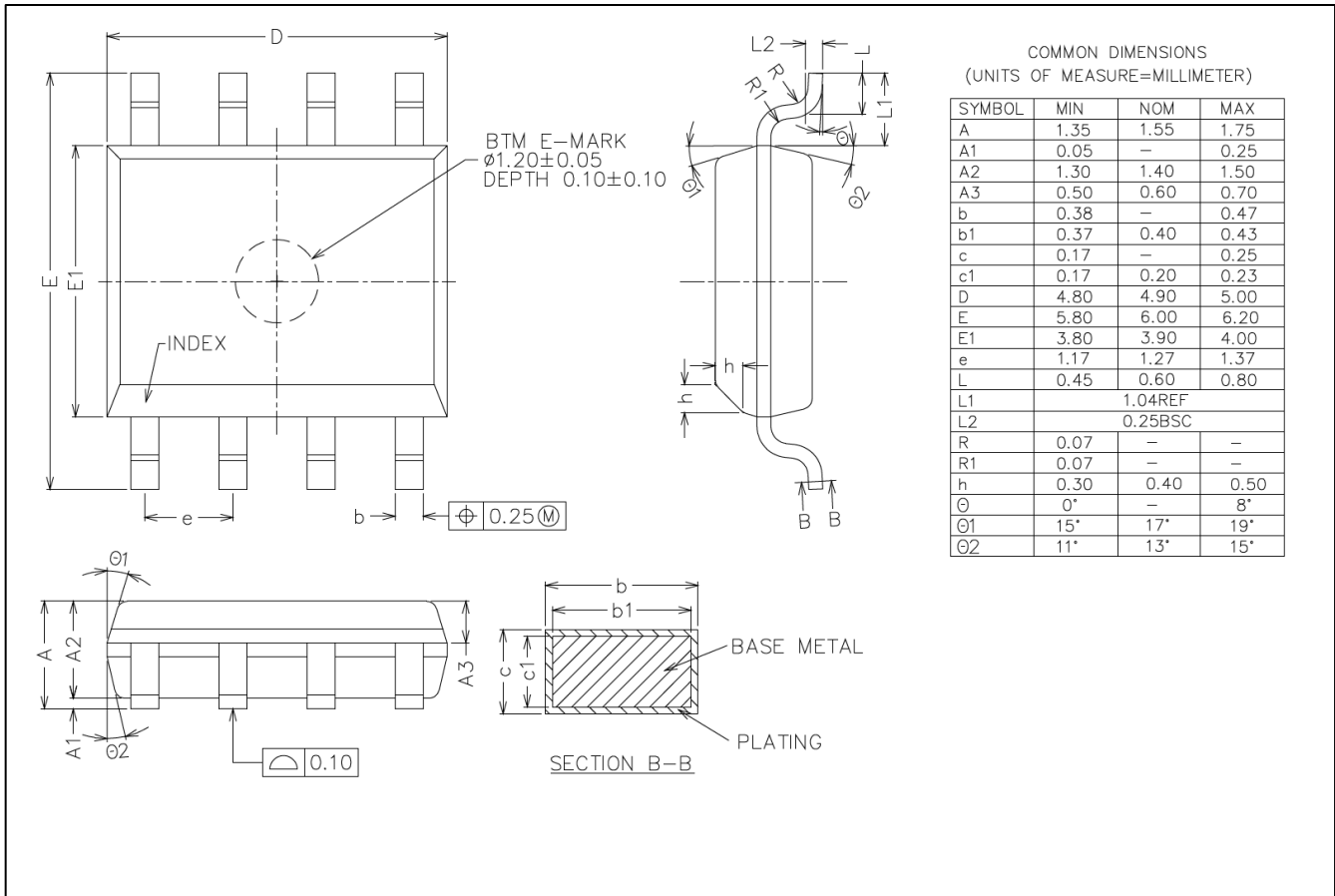
### 10. Package Information

#### 10.1. SOP8

##### 10.1.1. Tape and Reel

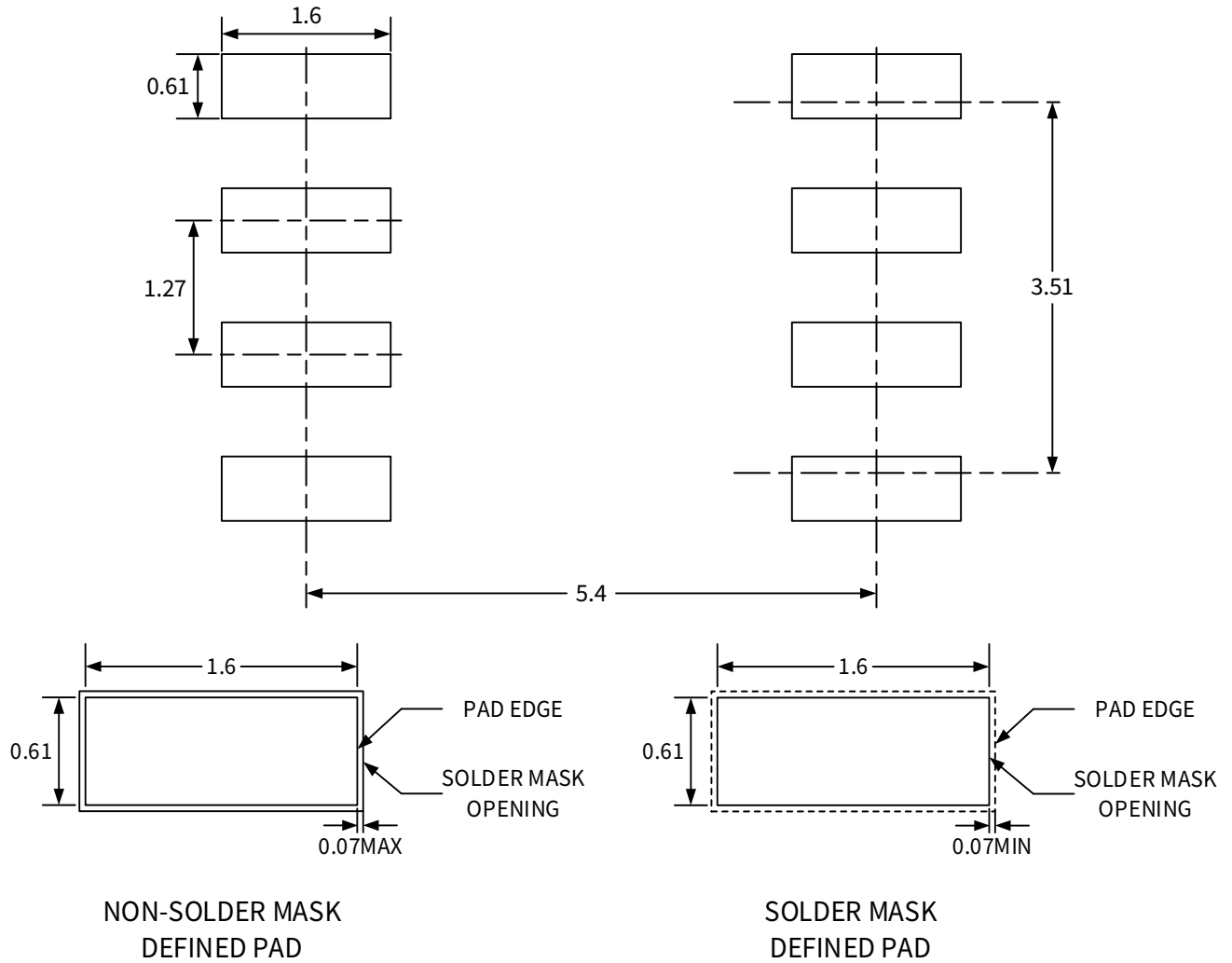


10.1.2. Mechanical Data



10.1.3. Recommended Land Pattern

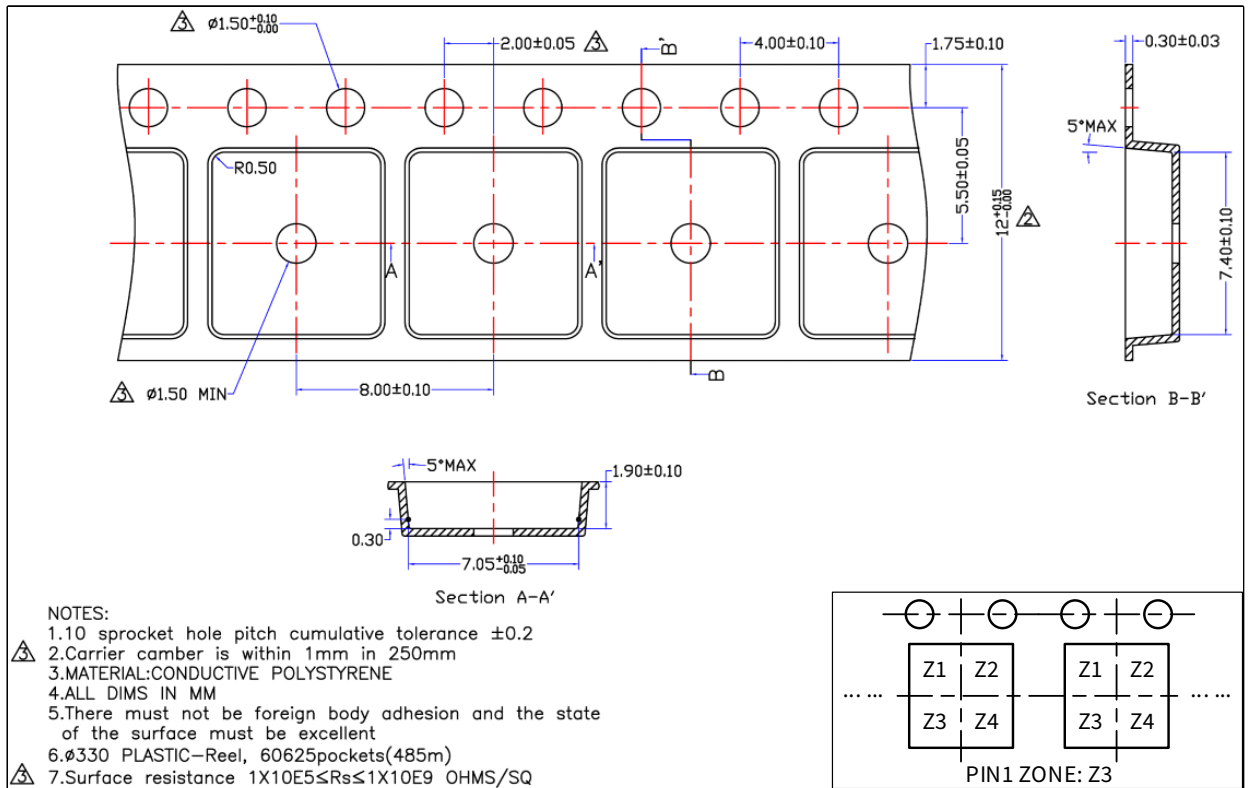
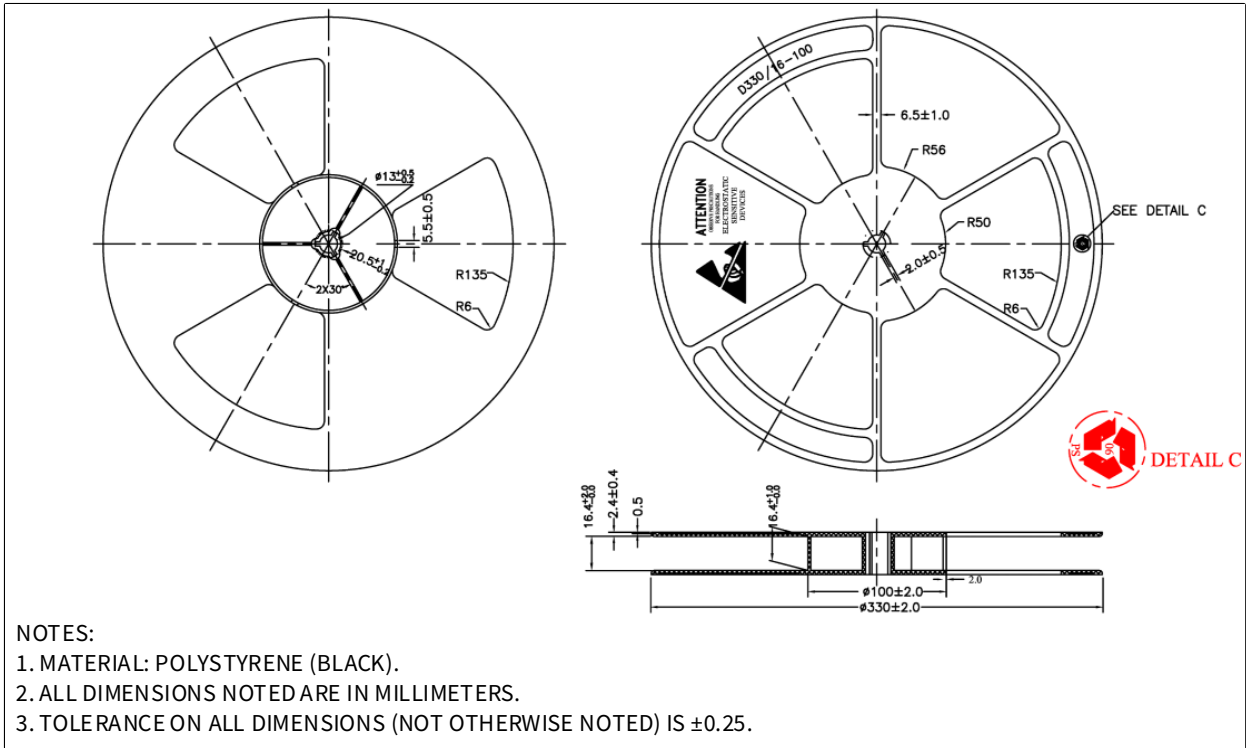
LAND PATTERN EXAMPLE



NOTES: ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.

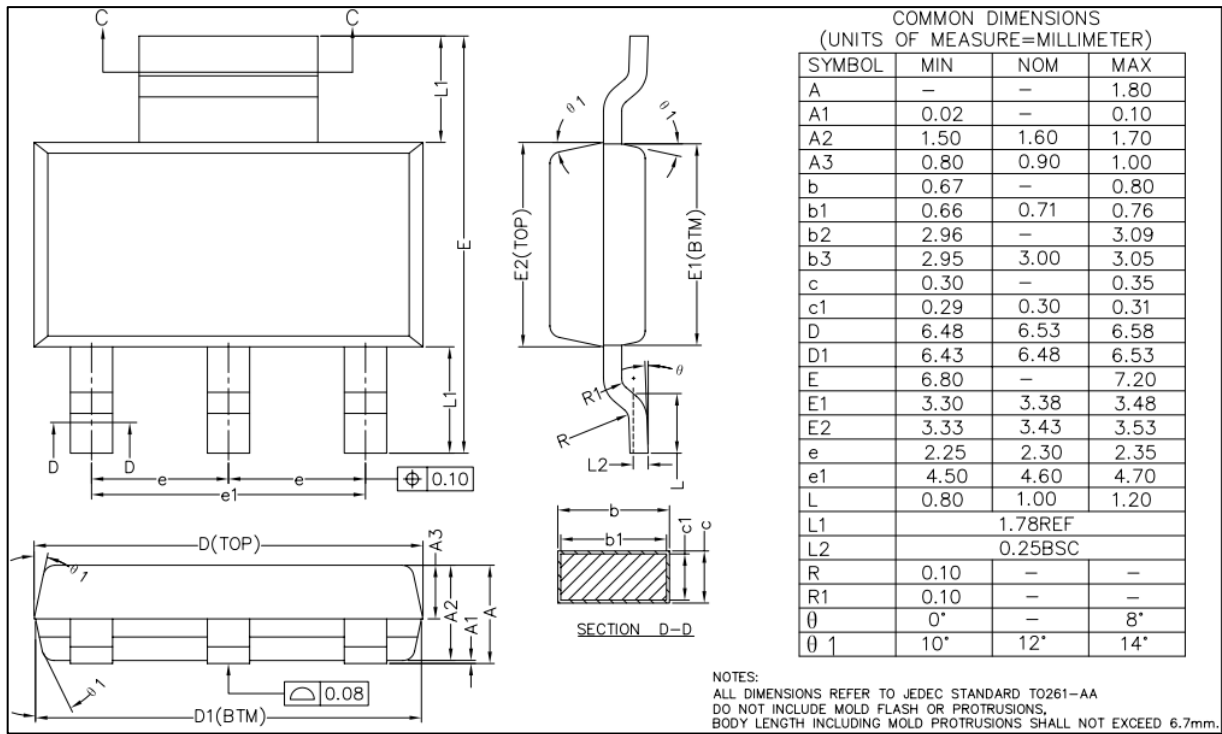
10.2. SOT223

10.2.1. Tape and Reel

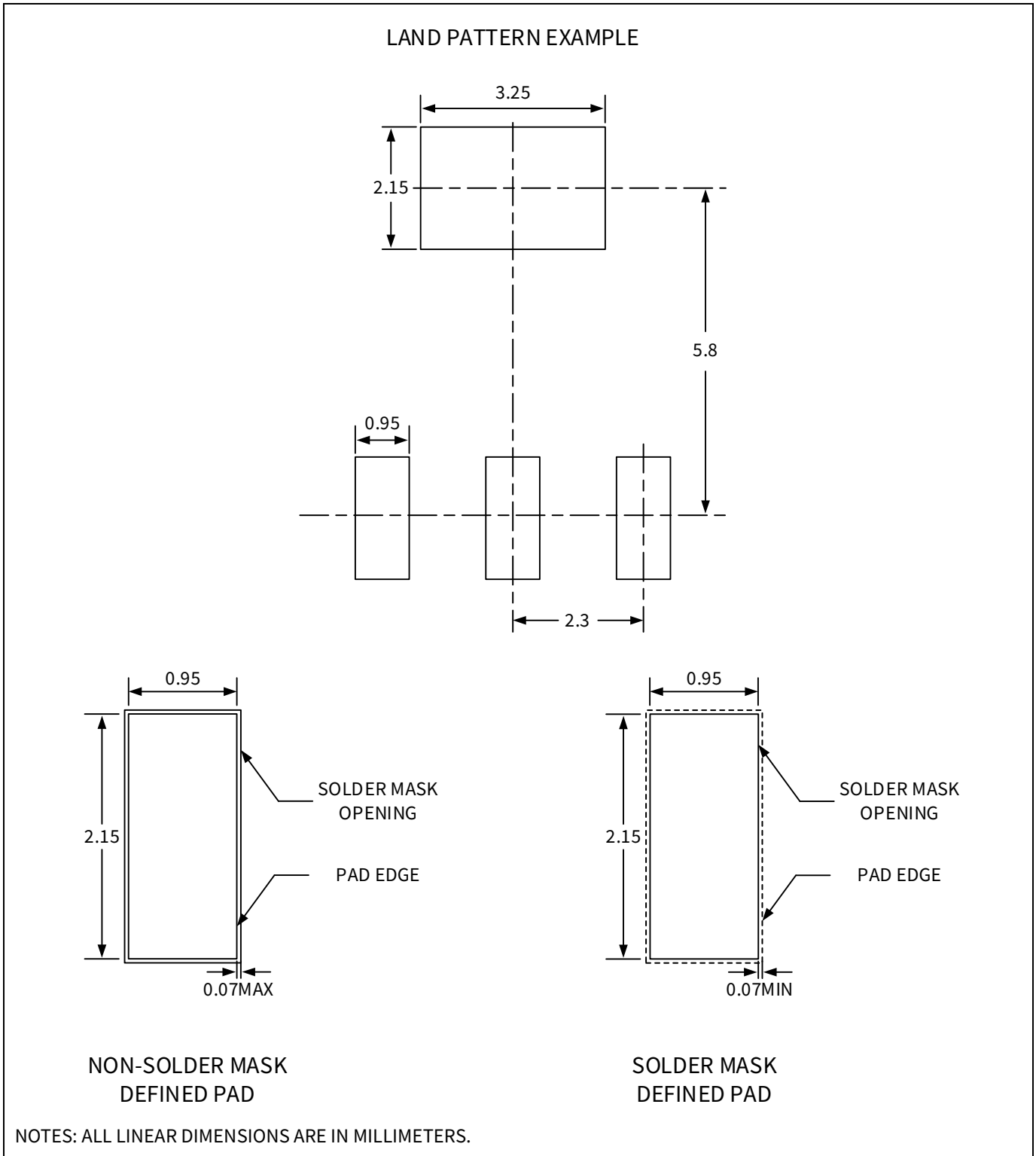


10.2.2. Mechanical Data





10.2.3. Recommended Land Pattern



**11. Order Information**

<b>Orderable Part Number</b>	<b>MSL</b>	<b>Package</b>	<b>SPQ</b>	<b>Marking</b>
NSE11409-QSPR	3	SOP8	2500	NSE 11409Q1
NSE11409-QSTBR	3	SOT223	2500	NSE 11409Q1
NOTE: All packages are RoHS-compliant				

**12. Revision history**

<b>Revision</b>	<b>Description</b>	<b>Date</b>
1.0	Initial released version	2023/12

## **IMPORTANT NOTICE**

The information given in this document shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party's intellectual property rights.

You are solely responsible for your use of Novosense' products and applications, and for the safety thereof. You shall comply with all laws, regulations and requirements related to Novosense's products and applications, although information or support related to any application may still be provided by Novosense.

The resources are intended only for skilled developers designing with Novosense' products. Novosense reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided. Novosense authorizes you to use these resources exclusively for the development of relevant applications designed to integrate Novosense's products. Using these resources for any other purpose, or any unauthorized reproduction or display of these resources is strictly prohibited. Novosense shall not be liable for any claims, damages, costs, losses or liabilities arising out of the use of these resources.

For further information on applications, products and technologies, please contact Novosense ([www.novosns.com](http://www.novosns.com)).

**Suzhou Novosense Microelectronics Co., Ltd**