MK Micro SD Specification

High Endurance

Product List

MKUS032G-CGT1B/ MKUS064G-CGT1A
MKUS128G-CGT2A / MKUS256G-CGT4A

Revision History

Version	Date	Description
Rev 1.0	*2021/02/02*	*Released*

Notice :

The datasheet is prepared and approved by MK Founder semiconductor co., LTD.

MK Founder reserves the right to change products or specifications without notice.

CONTENTS

1. Description ..... - 5 -

2. Product List ..... - 5 -

3. Features ..... - 5 -

4. Functional Block Diagram ..... - 6 -

5. Product Specification ..... - 6 -

5.1Current Consumption ..... - 6 -

5.2 Reliability and Durability ..... - 6 -

6. Pin Assignment ..... - 7 -

7. SD Card Registers ..... - 7 -

7.1 Card Identification Register (CID) ..... - 7 -

7.2 Card Specific Data Register (CSD) ..... - 8 -

8. Bus Operation Conditions ..... - 10 -

8.1 For 3.3V Signaling ..... - 10 -

8.1.1 Threshold Level for High Voltage Range ..... - 10 -

8.1.2 Peak Voltage and Leakage Current ..... - 10 -

8.1.3 Bus Signal Line Load ..... - 10 -

8.1.4 Bus Signal Levels ..... - 11 -

8.1.5 Bus Timing(Default) ..... - 11 -

8.1.6 Bus Timing (High-Speed Mode) ..... - 13 -

8.2 For 1.8V Signaling ..... - 14 -

8.2.1 Threshold Level for High Voltage Range ..... - 14 -

8.2.2 Peak Voltage and Leakage Current ..... - 15 -

8.2.3 Bus Timing Specification in SDR12, SDR25, SDR50 and SDR104 Modes ..... - 15 -

8.2.3.1 Clock Timing ..... - 15 -
8.2.3.2 Card Input Timing ..... - 16 -
8.2.3.3 Card Output Timing ..... - 16 -
9.Physical Dimension ..... - 17 -

1. Description

MK Micro SD is a removable flash memory card solution.

MK Micro SD is a hybrid device combining a flash controller include LDPC based ECC and a flash memory, complying with SDA Standard interface.

The flash controller includes LDPC based ECC technology, wear-leveling, IOPS optimization and performance optimization algorithm to stabilize the performance after long time operation.

SD is an ideal storage solution for many electronics devices. SD is designed to cover a wide area of application such as smart phones, Tablet PCs, notebook, sports camera, car video recorder, etc. Not only used in consumer products, SD is being adopted widely in embedded applications, such as surveillance application, because of its compact size, low power consumption and many enhanced feature.

2. Product List

Part Number	Capacity	Flash Type	Actual Size	Speed Class	Write/Read Speed	UHS-I	Type
MKUS032G-CGT1B	32GB	TLC	29.12GB	C10, U3, V30, A2	Up to 80/100MB/s	SDR104	SDHC
MKUS064G-CGT1A	64GB	TLC	58.24GB	C10, U3, V30, A2	Up to 80/100MB/s	SDR104	SDHC
MKUS128G-CGT2A	128GB	TLC	116.48GB	C10, U3, V30, A2	Up to 80/100MB/s	SDR104	SDHC
MKUS256G-CGT4A	256GB	TLC	232.96GB	C10, U3, V30, A2	Up to 80/100MB/s	SDR104	SDHC

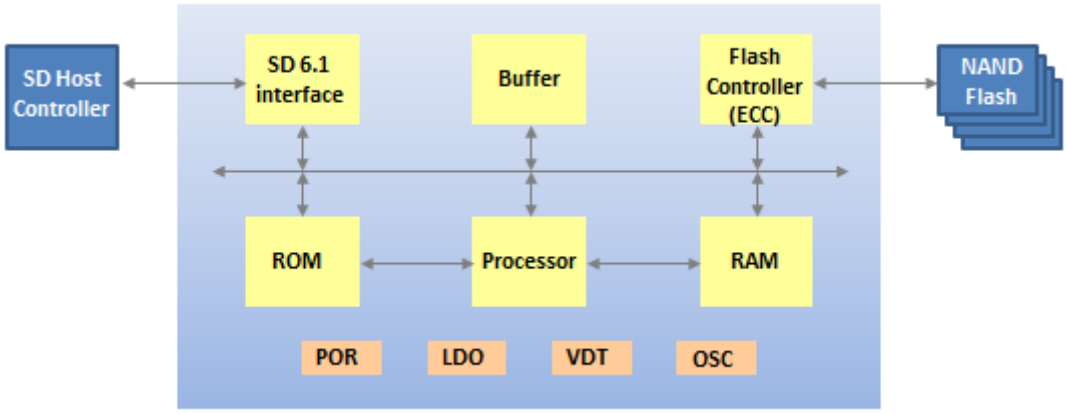
Table 1：Product List

3. Features

- Complies to SD specifications version 6.1
- Voltage operating: 2.7~3.6V.
- Targeted for portable and stationary applications
- Bus Speed Mode:
  - DS-Default Speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5MB/sec
  - HS-High Speed mode: 3.3V signaling, frequency up to 50MHz, up to 25MB/sec
  - SDR12-1.8V signaling, frequency up to 25MHz, up to 12.5MB/sec
  - SDR25-1.8V signaling, frequency up to 50MHz, up to 25MB/sec
  - SDR50-1.8V signaling, frequency up to 100MHz, up to 50MB/sec
  - SDR104-1.8V signaling, frequency up to 208MHz, up to 104MB/sec
  - DDR50-1.8V signaling, Frequency up to 50 MHz, sampled on both clock edges, up to 50MB/sec
- Switch function command supports Bus Speed Mode, Command System, Drive Strength, and future functions.

- password protection (CMD42-LOCK_UNLOCK)
- LDPC ECC & Global Wear Leveling
- Power management for low power operation
- Up to 3K P/E cycles

4. Functional Block Diagram



5. Product Specification

5.1Current Consumption

- Standby current: 150uA（Maximum value）
- Standby current: 100uA（average value）
- Operating current: 100mA（Maximum value）
- Operating current: 80mA（average value）

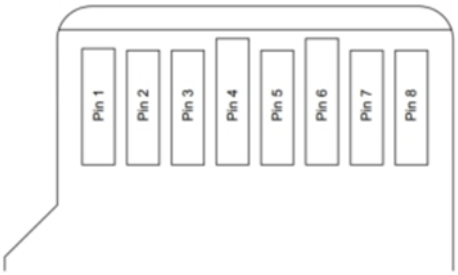
*Test condition: Realtek5329 card reader @SDR104, VCC=3.3v

5.2 Reliability and Durability

Temperature	Operation: -25°C/85°C Storage: -40°C/85°C
Durability	10,000 insertion/removal cycles;
Bending	10[N] Center 200[mm/minute] 60[sec]
Torque	0.10Nm,+/-2.5 deg.max.
Drop test	1.5m free fall
Electrostatic Discharge (ESD)	IEC 61000-4-2 contact discharge: +/- 2[kV] and +/- 4[kV] 150[pF],330[Ohm] air discharge: up to +/- 15[kV] 150[pF], 330[Ohm]

Table 2: Reliability and Durability

6. Pin Assignment



Pin No.	SD Mode			SPI Mode		
	Name	Type	Description	Name	Type	Description
1	Dat2	I/O/PP	Data Line [Bit 2]	RSV		Reserved
2	CD/DAT3	I/O/PP	Card Detect / Data Line [Bit 3]	CS	I	Chip Select
3	CMD	PP	Command/Response	DI	I	Data In
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS	S	Supply voltage ground	VSS	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [Bit 1]	RSV		Reserved

S: power supply; I: input; O: output; PP: I/O using push-pull drivers

Table 3 : Pin Assignment

7. SD Card Registers

7.1 Card Identification Register (CID)

The Card Identification (CID) register is 128 bit wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number.

The structure of the CID register is defined in the following table.

CID Bit	Width	Name	Field
[127:120]	8	Manufacture ID	MID
[119:104]	16	OEM/Application ID	OID
[103:64]	40	Product Name	PNM
[63:56]	8	Product Revision	PRV
[55:24]	32	Product Serial Number	PSN
[23:20]	4	Reserved	---
[19:8]	12	Manufacturing Date	MDT
[7:1]	7	CRC7 check sum	CRC
[0]	1	Not used,always”1	---

Table 4 ：SD Card CID Table

- All contents in the CID table are programmable; Manufacturers can update the CID data through utility.
- Manufacturers should license MID and OID field form the SD Card Association(SDA)

7.2 Card Specific Data Register (CSD)

The Card-Specific Data register provides information regarding access to the card contents. The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used, etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The CSD Table Version 2.0(as shown below) is applied to SDHC and SDXC Cards. Note that bits [15:0] are programmable by the host side. Refer to the SD specification for detailed information

CSD Bit	Width	Name	Field	Value	Note
[127:126]	2	CSD structure	CSD_STRUCTURE	01b	V2.0(>2GB Card)
[125:120]	6	Reserved	---	---	---
[119:112]	8	Data read access-time 1	(TAAC)	0E h	
[111:104]	8	Data read access-time2 in CLK cycles(NSA*100)	(NSAC)	00 h	
[103:96]	8	Max data transfer rate	(TRAN_SPEED)	32 h 5A h 0B h 2B h	
[95:84]	12	Card command classes	CCC	5B5 h	
[83:80]	4	Max. read data block length	(READ_BL_LEN)	9 h	512 Byte
[79]	1	Partial block read allowed	(READ_BL_PARTIAL)	0	
[78]	1	Write block misalignment	(WRITE_BLK_MISALIGN)	0	

[77]	1	Read block misalignment	(READ_BLK_MISALIGN)	0	
[76]	1	DSR implemented	DSR_IMP	X	
[75:70]	6	Reserve	---	---	
[69:48]	22	Device size	C_SIZE	xxxxxxh	
[47]	1	Reserved	---	0	
[46]	1	Erase single block enable	(ERASE_BLK_EN)	1	
[45:39]	7	Erase sector size	(SECTOR_SIZE)	7F h	
[38:32]	7	Write protect group size	C_SIZE	0 b	
[31]	1	Write protect group enable	---	0	
[30:29]	2	Reserved	(ERASE_BLK_EN)	0 b	
[28:26]	3	Write speed factor	(SECTOR_SIZE)	010 b	
[25:22]	4	Max. write data block length	(WP_GRP_SIZE)	9 h	
[21]	1	Partial block write allowed	(WP_GRP_ENABLE)	0	
[20:16]	5	Reserved	---	---	
[15]	1	File format group	(FILE_FORMAT_GRP)	0	
[14]	1	Copy flag	COPY	x	
[13]	1	Permanent write protection	PERM_WRITE_PROTECT	x	
[12]	1	Temporary write protection	TMP_WRITE_PROTECT	x	
[11:10]	2	File format	(FILE_FORMAT)	00 b	
[9:8]	2	Reserved	---	00 b	
[7:1]	7	CRC	CRC	---	
[0]	1	Not used,always’1’	---	1	

Table 5: CSD (Version 2.0) Table

8. Bus Operation Conditions

8.1 For 3.3V Signaling

8.1.1 Threshold Level for High Voltage Range

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	VDD	2.7	3.6	V	
Output High Voltage	VOH	0.75* VDD		V	IOH=2mA VDD min
Output Low Voltage	VOL		0.125* VDD	V	IOL=2mA VDD min
Input High Voltage	VIH	0.625* VDD	VDD+0.3	V	
Input Low Voltage	VIL	Vss-0.3	0.25* VDD	V	
Power Up Time			250	ms	From 0V to VDD min

Table 6: Threshold Level for High Voltage

8.1.2 Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remark
Peak voltage on all lines		-0.3	VDD+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 7: Peak Voltage and Leakage Current

8.1.3 Bus Signal Line Load

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	RCMD RDAT	10	100	KΩ	To prevent bus floating
Total bus capacitance for each signal line	CL		40	pF	1 card CHOST+CBUS shall not exceed 30pF
Card capacitance for each signal pin	CCARD		10	pF	
Maximum signal inductance			16	nH	
Pull-up resistance inside card(pin1)	RDAT3	10	90	KΩ	May be used for card detection
Capacity Connected to Power Line	CC		5	uF	To prevent inrush current

Table 8: Bus Operating Conditions - Signal Line's Load

8.1.4 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

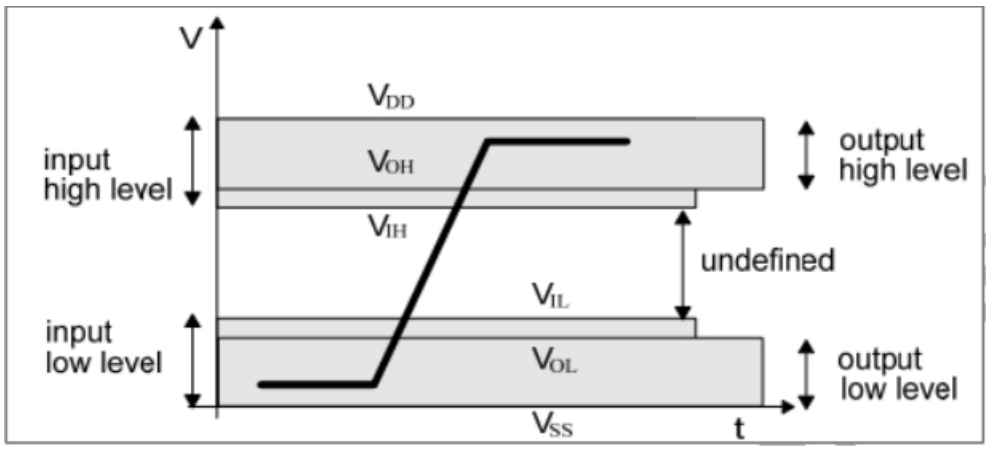


Figure 1: Bus Signal Levels

To meet the requirements of the JEDEC specification JESD8-1A and JESD8-7, the card input and output voltages shall be within the specified ranges shown in Table 6-2 for any VDD of the allowed voltage range:

8.1.5 Bus Timing(Default)

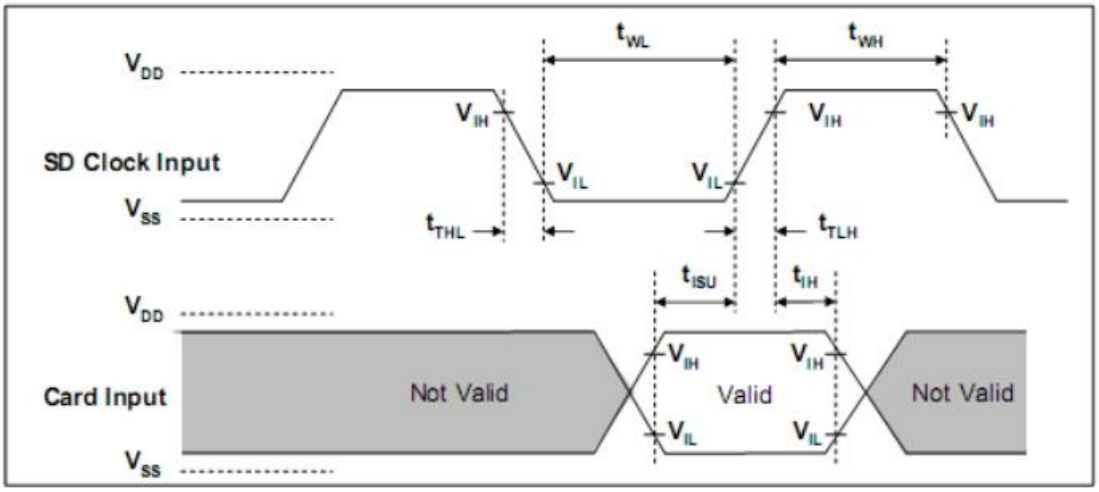


Figure 2: Card input Timing (Default Speed Card)

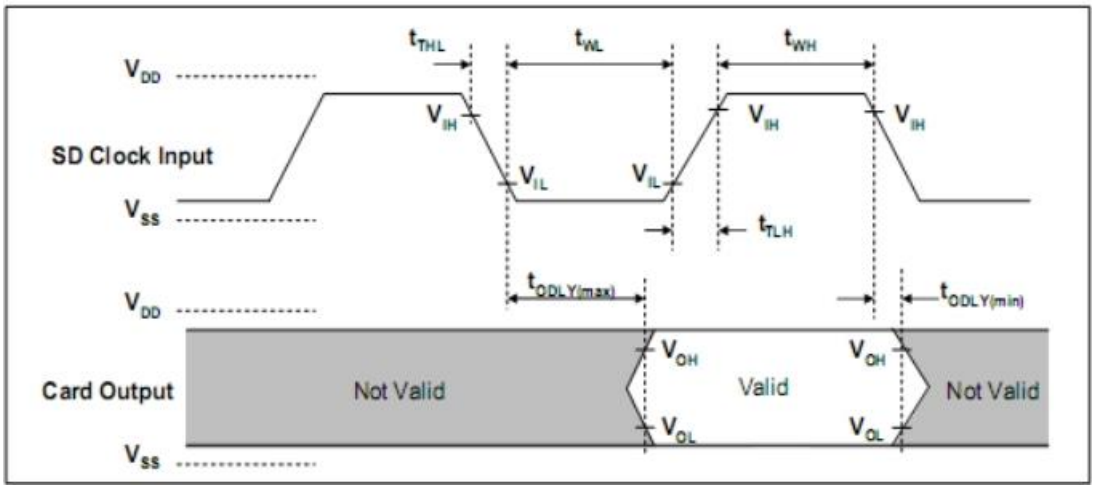


Figure 3: Card Output Timing (Default Speed Mode)

Parameter	Symbol	Min.	Max	Unit	Remark
Clock CLK （All values are referred to min（VIH）and max（VIL））					
Clock frequency data transfer Mode	fpp	0	25	MHz	CCARD ≤ 10pF (1 card)
Clock frequency Identification Mode	fOD	0(1)/100	400	KHz	CCARD ≤ 10pF (1 card)
Clock low time	tWL	10		ns	CCARD ≤ 10pF (1 card)
Clock high time	tWH	10		ns	CCARD ≤ 10pF (1 card)
Clock rise time	tTLH		10	ns	CCARD ≤ 10pF (1 card)
Clock fall time	tTHL		10	ns	CCARD ≤ 10pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	5		ns	CCARD ≤ 10pF (1 card)
Input hold time	tIH	5		ns	CCARD ≤ 10pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	tODLY	0	14	ns	CL ≤ 40pF (1 card)
Output Hold time	tOH	0	50	ns	CL ≤ 40pF (1 card)

(1) 0 Hz means to stop the clock.The given minimum frequency range is for cases were continues clock is required (refer to Chapter 4.4-Clock Control)

Table 9: Bus Timing-Parameters Values (Default Speed)

8.1.6 Bus Timing (High-Speed Mode)

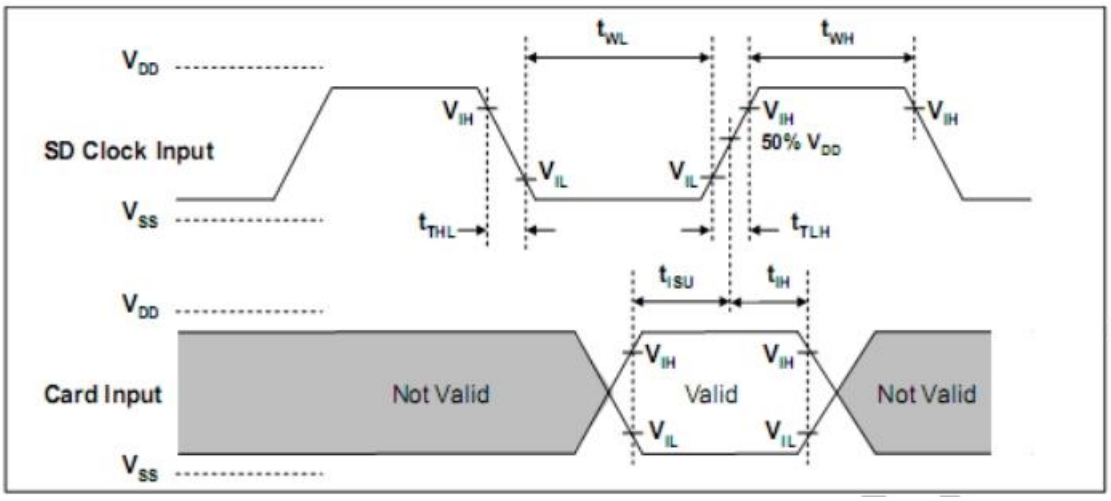


Figure 4: Card Input Timing(High Speed Card)

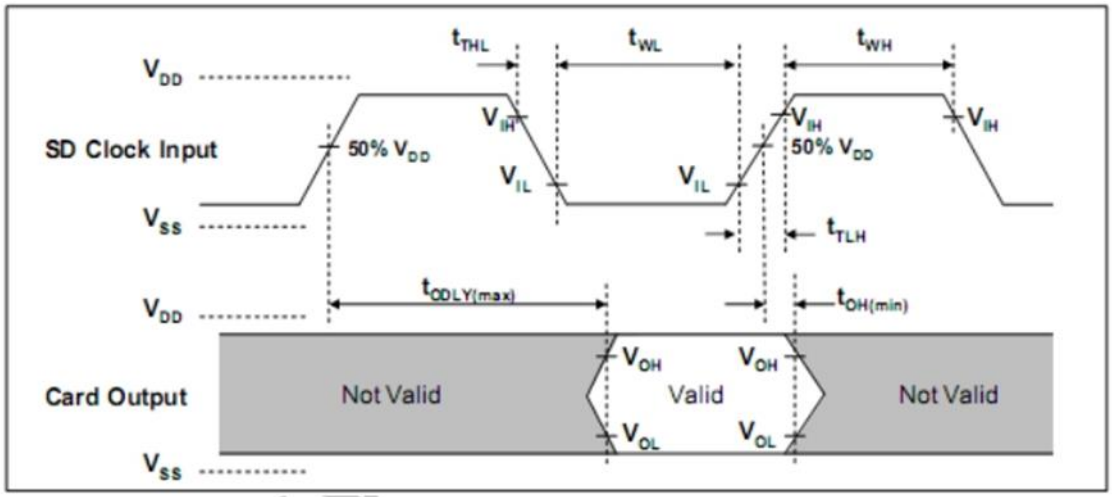


Figure 5: Card Output Timing(High Speed Mode)

Parameter	Symbol	Min.	Max	Unit	Remark
Clock CLK （All values are referred to min（VIH）and max（VIL））					
Clock frequency data transfer Mode	fpp	0	50	MHz	CCARD ≤ 10pF (1 card)
Clock low time	tWL	7		ns	CCARD ≤ 10pF (1 card)
Clock high time	tWH	7		ns	CCARD ≤ 10pF (1 card)
Clock rise time	tTLH		3	ns	CCARD ≤ 10pF (1 card)
Clock fall time	tTHL		3	ns	CCARD ≤ 10pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	6		ns	CCARD ≤ 10pF (1 card)
Input hold time	tIH	2		ns	CCARD ≤ 10pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	tODLY		14	ns	CL ≤ 40pF (1 card)
Output Hold time	tOH	2.5		ns	CL ≥ 15pF (1 card)
Total System capacitance for each line[1]	CL		40	pF	1 card

(1) In order to satisty sever timing , host shall drive only one card.

Table 10: Bus Timing – Parameters Values (High Speed)

8.2 For 1.8V Signaling

8.2.1 Threshold Level for High Voltage Range

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	VDD	2.70	3.60	V	
Regulator Voltage	VDDIO	1.70	1.95	V	Generated by VDD
Output High Voltage	VOH	1.40		V	IOH=2mA
Output Low Voltage	VOL		0.45	V	IOL=2mA
Input High Voltage	VIH	1.27	2.00	V	
Input Low Voltage	VIL	Vss-0.30	0.58	V	

Table 11: Threshold Level for High Voltage

8.2.2 Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remark
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected

Table 12: Peak Voltage and Leakage Current

8.2.3 Bus Timing Specification in SDR12, SDR25, SDR50 and SDR104 Modes

8.2.3.1 Clock Timing

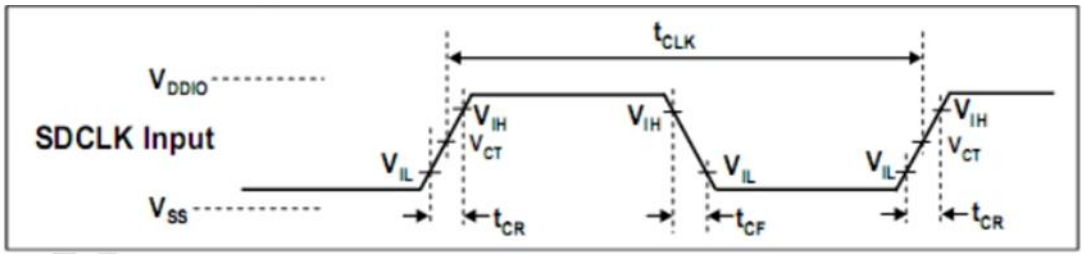


Figure 6: Clock Signal Timing

Symbol	Min	Max	Unit	Remark
tCLK	4.8	-	ns	208MHz (Max.), Between rising edge, VCT=0.975V
tCR, tCF	-	0.2* tCLK	ns	tCR, tCF < 2.00ns (max.) at 208MHz, CCARD=10pF tCR, tCF < 2.00ns (max.) at 100MHz, CCARD=10pF The absolute maximum value of tCR, tCF is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

Table 13: Clock Signal Timing

8.2.3.2 Card Input Timing

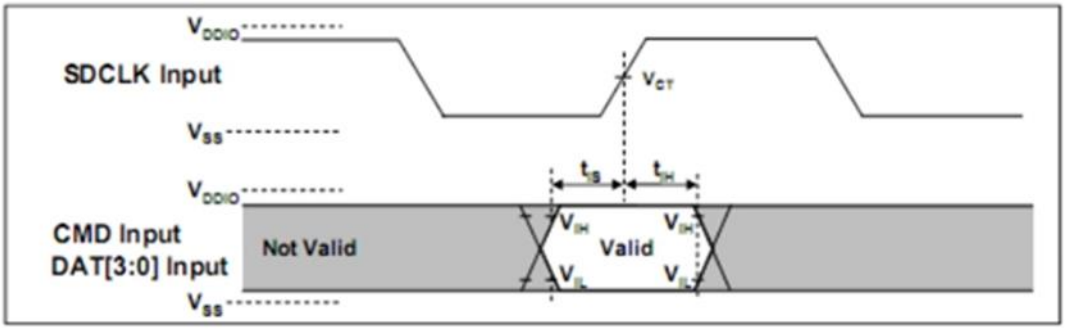


Figure 7: Card Input Timing

Symbol	Min	Max	Unit	SDR104 modes
tIS	1.40	-	ns	CCARD = 10pF, VCT = 0.975V
tIH	0.80	-	ns	CCARD = 5pF, VCT = 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 modes**
tIS	3.00	-	ns	CCARD = 10pF, VCT = 0.975V
tIH	0.80	-	ns	CCARD = 5pF, VCT = 0.975V

Table 14: SDR50/SDR104 Input Timing

8.2.3.3 Card Output Timing

8.2.3.3.1 Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)

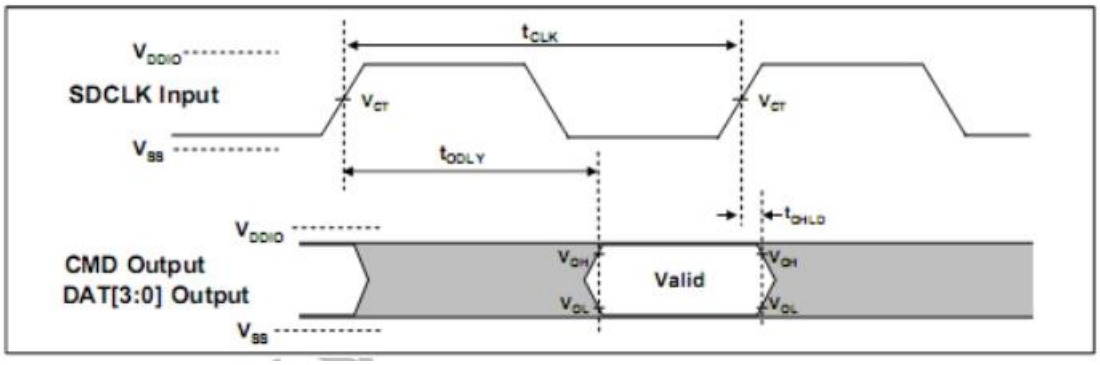


Figure 8: Output Timing of Fixed Data Window

Symbol	Min	Max	Unit	Remark
tODLY	-	7.5	ns	tCLK ≥10.0ns, CL=30pF, using driver Type B, for SDR50.
tODLY		14	ns	tCLK ≥20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12.
tOH	1.5	-	ns	Hold time at the tODLY (min.). CL=15pF

Table 15: Output Timing of Fixed Data Window

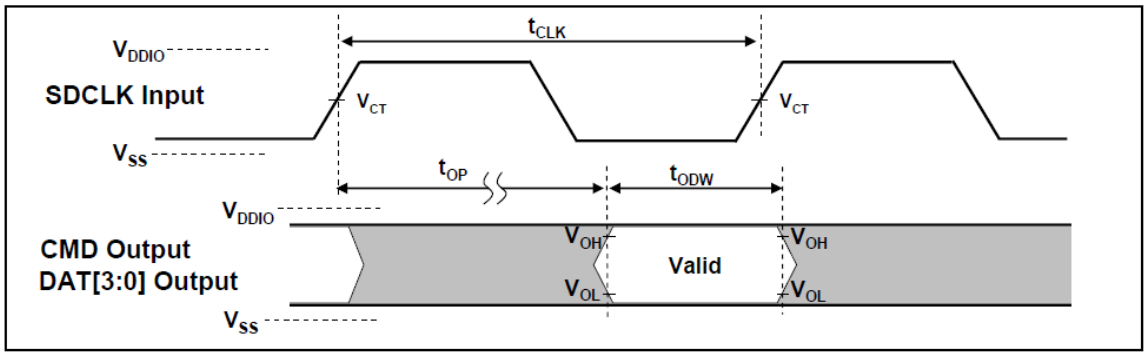


Figure 9: Output Timing of Variable Data Window

Symbol	Min	Max	Unit	Remark
tOP	0	2	UI	Card Output Phase
ΔtOP	-350	+1550	ps	Delay variation due to temperature change after tuning
tOH	1.5	-	UI	tODW = 2.88ns at 208MHz

Table 16: Output Timing of Variable Data Window

9.Physical Dimension

Type	Measurement
Length	15mm +/- 0.1mm(B)
Width	11mm +/- 0.1mm(A)
Thickness	1.0mm+/-0.1mm(C)
	0.7mm+/-0.1mm(C1)
Weight	0.33 gram Max

Table 17: Physical Dimension Specifications (Unit in mm)

Mechanical form factor as follows: (Unit in mm)

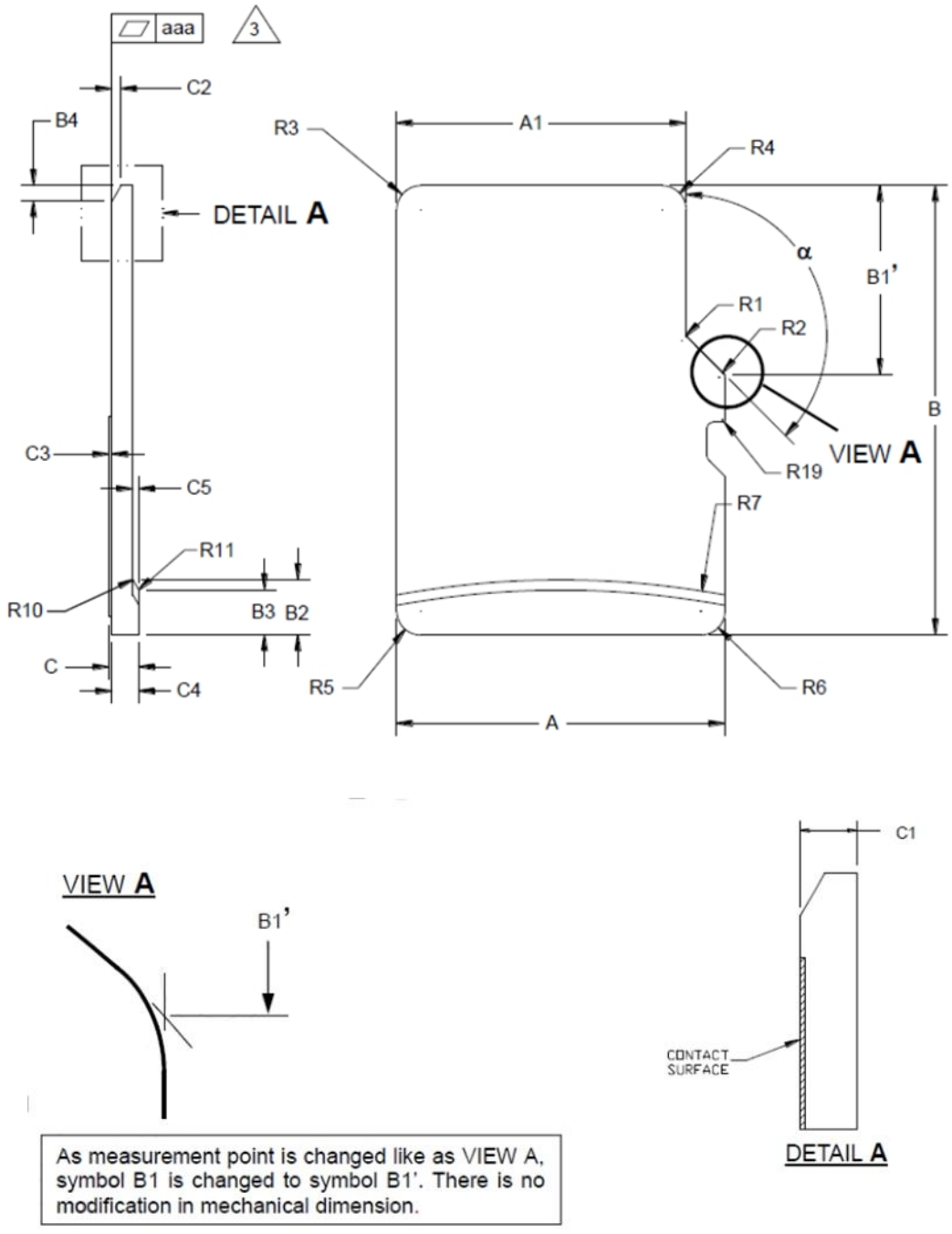


Figure 10: Top View

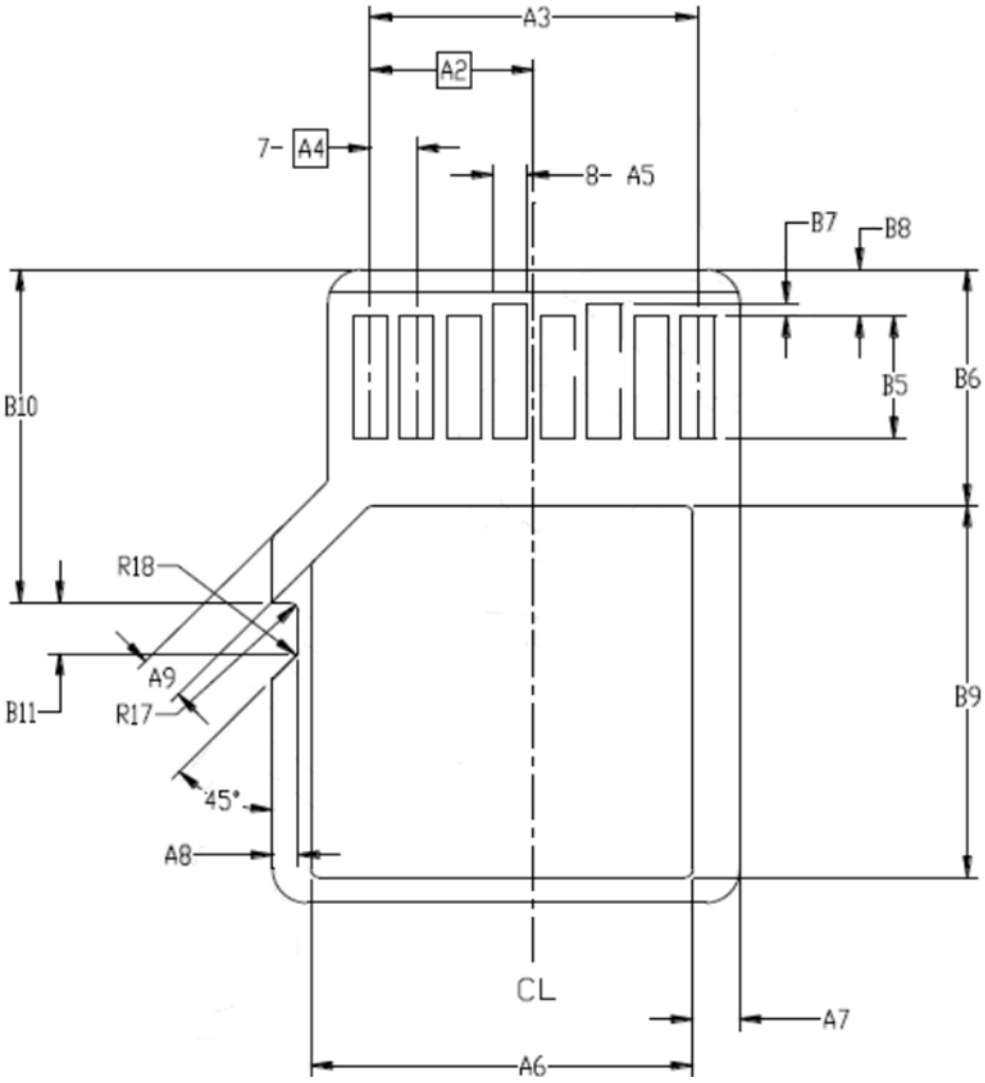


Figure 11: Bottom View

SYMBOL	MIN (mm)	NOM (mm)	MAX (mm)	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
B	14.90	15.00	15.10	
B1’	6.13	6.23	6.33	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
C4	0.80	-	1.10	
C5	0.15	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.60	0.80	0.90	
R6	0.60	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	

Table 18: Dimensions