18V, 2A, ACOT™ Step-Down Converter in 8 Pin TSOT-23

General Description

The RT6218A/B is a simple, easy-to-use, 2A synchronous step-down DC-DC converter with an input supply voltage range of 4.5V to 18V. The device integrates low $R_{DS(ON)}$ power MOSFETs to achieve high efficiency in a SOT23 package and build-in accurate reference voltage (0.765V by product options).

The RT6218A/B adopts Advanced Constant On-Time (ACOT™) control architecture to provide an ultrafast transient response with few external components and to operate in nearly constant switching frequency over the line, load, and output voltage range. The RT6218A operates in automatic PSM that maintains high efficiency during light load operation. RT6218B operates in Forced PWM that helps meet tight voltage regulation accuracy requirements.

The RT6218A/B senses both FETs current for a robust over-current protection. The device features cycle-by-cycle current limit protection and prevent the device from the catastrophic damage in output short circuit, over current or inductor saturation. The RT6218A/B series offers programmable start-up by connecting a capacitor at external SS pin. The device also includes input under-voltage lockout, output under-voltage protection, and over-temperature protection (thermal shutdown) to provide safe and smooth operation in all operating conditions. The RT6218A/B are offered in TSOT-23-8(FC) package.

Applications

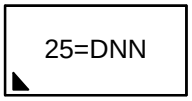
- Set-Top Boxes
- LCD TVs
- Home Networking Devices
- Surveillance
- General Purpose

Features

- **Input Supply Voltage Range : 4.5V to 18V**
- **2A Converter With Built-in 120mΩ/65mΩ Low $R_{DS(ON)}$ Power FETs**
- **Advanced Constant On-Time (ACOT™) Control for Ultrafast Transient Response**
- **Fixed Switching Frequency : 650kHz (SOT23-8)**
- **Optional for Operation Modes :**
  - **Automatically Power Saving Mode (PSM) (RT6218A)**
  - **Forced PWM Mode (RT6218B)**
- **Optimized for Low-ESR Ceramic Output Capacitors**
- **±1.5% High-Accuracy Feedback Reference Voltage**
- **Output Voltage Range : up to 6.5V**
- **Externally Adjustable Soft-Start**
- **Monotonic Start-Up for Pre-biased Outputs**
- **Both HS/LS FETs Protection for Robust Over Current Protection**
- **Input Under-Voltage Lockout (UVLO)**
- **Output Under-Voltage Protection (UVP) with Hiccup Mode**
- **Over-Temperature Protection (OTP) (Thermal Shutdown)**
- **Enable Control**
- **Power Good Indication**
- **RoHS Compliant and Halogen Free**
- **Available in TSOT-23-8 Package**

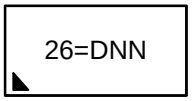
Marking Information

RT6218AHRGJ8F



25= : Product Code
DNN : Date Code

RT6218BHRGJ8F



26= : Product Code
DNN : Date Code

Ordering Information

RT6218A/B □ R □□

- Package Type
  J8F : TSOT-23-8 (FC)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Reference Voltage
  V_{REF} = 0.765V
- UVP Option
  H : Hiccup
- PWM Operation Mode
  A : Automatic PSM
  B : Forced PWM

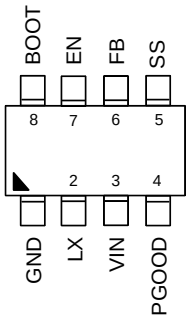
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)

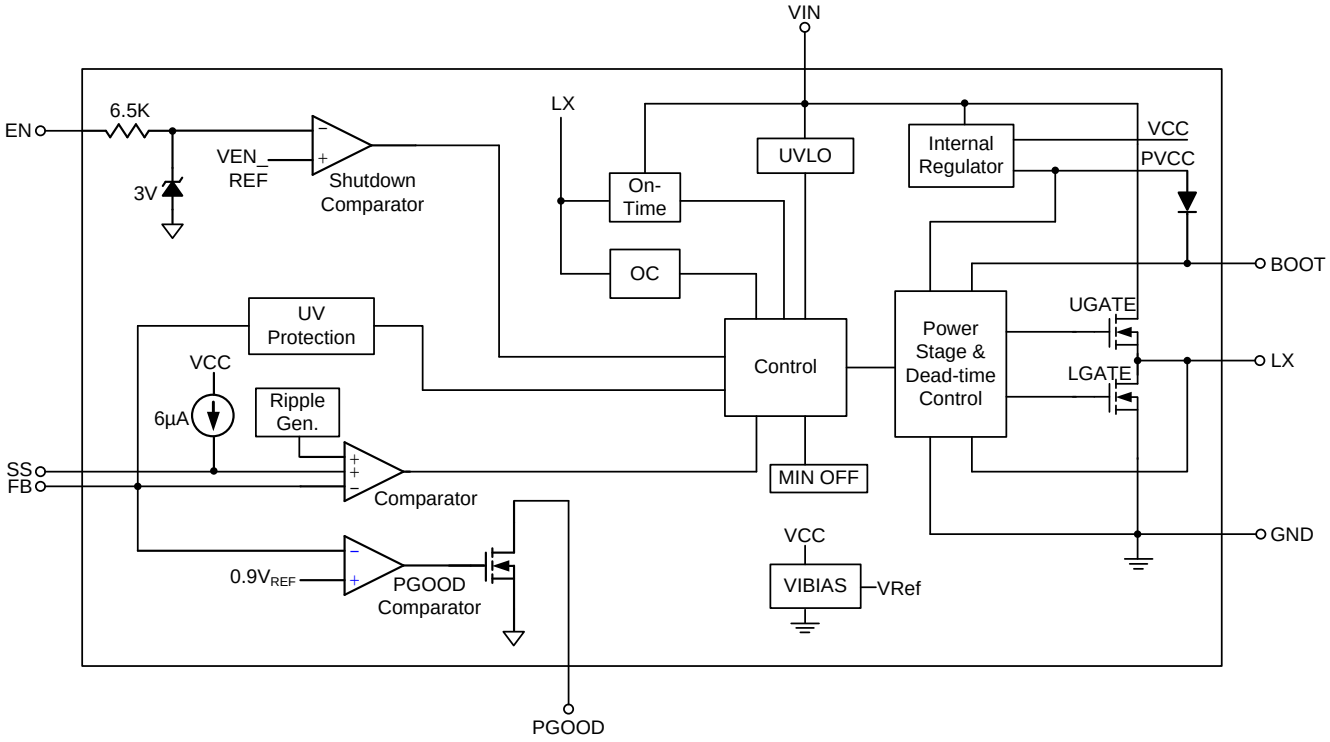


TSOT-23-8 (FC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Power ground. This pin, connected to analog ground, must be soldered to a large PCB copper area for maximum power dissipation.
2	LX	Switch node between the internal switch and the synchronous rectifier. Connect this pin to the inductor and bootstrap capacitor.
3	VIN	Power input. The input voltage range is from 4.5V to 18V. Connect a suitable input capacitor between this pin and GND, with a typical capacitance of 22μF.
4	PGOOD	Open-drain power-good indication output. Once being started-up, PGOOD will be pulled low to GND if any internal protection is triggered.
5	SS	Soft-start capacitor connection node. Connect an external capacitor between this pin and ground to set the soft-start time. Do not leave this pin unconnected. A capacitor of 8.2nF is suggested.
6	FB	Feedback voltage input. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at Feedback Threshold Voltage, typically 0.765V.
7	EN	Enable control input. Floating this pin or connecting this pin to GND can disable the device and connecting this pin to logic high can enable the device.
8	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF ceramic capacitor between this pin and LX pin.

Functional Block Diagram



Operation

The RT6218A/B is a high-efficiency, synchronous step-down DC-DC converter that can deliver up to 2A output current from a 4.5V to 18V input supply. The RT6218A/B adopts ACOT™ control mode, which can reduce the output capacitance and provide ultrafast transient responses, and allow minimal component sizes without any additional external compensation network.

Enable Control

The RT6218A/B provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below a logic-low threshold voltage (V_{ENH}–ΔV_{EN}) of the enable input (EN), the converter will enter into shutdown mode, that is, the converter is disabled and switching is inhibited even if the VIN voltage is above VIN under-voltage lockout threshold (V_{UVLO}). During shutdown mode, the supply current can be reduced to I_{SHDN} (5μA or below). If the EN voltage rises above the logic-high threshold voltage (V_{ENH}) while the VIN voltage is higher than UVLO threshold (V_{UVLO}), the device will be turned on, that is, switching being enabled and soft-start sequence being initiated.

Low-Side Current Limit Protection

The RT6218A/B features a cycle-by-cycle valley-type current limit protection, measuring the inductor current through the synchronous rectifier (low-side switch). The inductor current level is determined by measuring the low-side switch voltage between the LX pin and GND, which is proportional to the switch current, during the low-side on-time. For greater accuracy, temperature compensation is added to the voltage sensing. Once the current rises above the low-side switch valley current limit (I_{LIM}), the on-time one-shot will be inhibited until the inductor current ramps down to the current limit level (I_{LIM}), that is, another on-time can only be triggered when the inductor current goes below the low-side current limit. This function can prevent the average output current from greatly exceeding the guaranteed low-side current limit value.

If the output load current exceeds the available inductor current (clamped by the above-mentioned low-side current limit), the output capacitor needs to supply the extra current such that the output voltage will begin to drop. If it drops below the output under-voltage protection trip threshold, the IC will stop switching to avoid excessive heat.

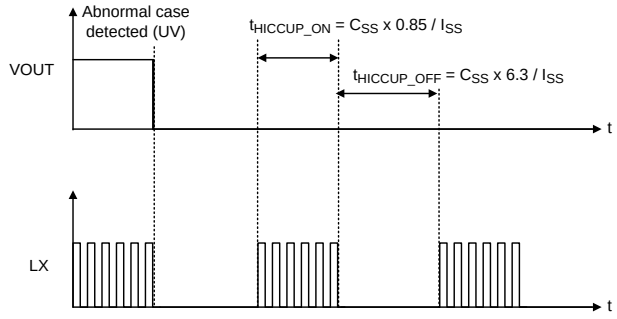
High-Side Current Limit Protection

The RT6218A/B also includes a cycle-by-cycle peak-type current limit protection against the condition that the inductor current increasing abnormally, even over the inductor saturation current rating. To ensure the low-side current limit protection can still function properly, the inductor current through the high-side switch will only be measured after a certain amount of delay when the high-side switch being turned on. If an over-current condition occurs, the converter will immediately turn off the high-side switch and turn on the low-side switch to prevent the inductor current exceeding the high-side switch peak-current limit.

Output Under-Voltage Protection and Hiccup Mode

The RT6218A/B includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold (typically 62.5% of the internal feedback reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches.

If the output under-voltage condition continues for a period of time, the RT6218A/B will enter output under-voltage protection with hiccup mode. During hiccup mode, the IC will shut down for t_{HICCUP_OFF} (C_{SS} x 6.3 / I_{SS}), and then attempt to recover automatically for t_{HICCUP_ON} (C_{SS} x 0.85 / I_{SS}). Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed.



External Bootstrap Capacitor

Connect a 0.1μF low-ESR ceramic capacitor between the BOOT and LX pins. This bootstrap capacitor supplies for the gate driver of the high-side N-channel MOSFET switch.

Over-Temperature Protection (Thermal Shutdown)

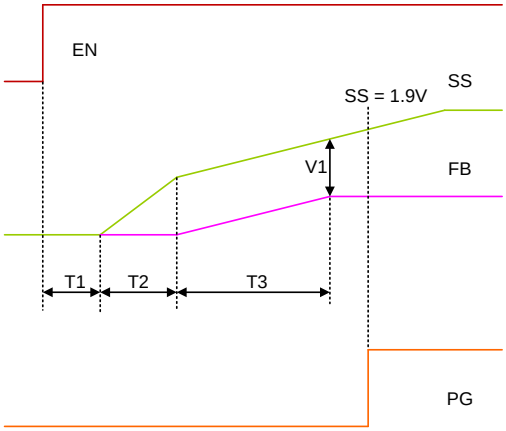
The RT6218A/B includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold T_{SD}. Once the junction temperature cools down by a thermal shutdown hysteresis (ΔT_{SD}), the IC will resume normal operation with a complete soft-start.

Soft-Start

The RT6218A/B provides adjustable soft-start function. When the EN pin becomes high, the SS charge current (I_{SS}) begins charging the capacitor which is connected from the SS pin to GND (C_{SS}).The soft-start function is used to prevent large inrush current while converter is being powered-up. The soft-start timing can be programmed by the external capacitor CSS between SS and GND. An internal current source I_{SS} (6μA) charges an external capacitor to build a soft-start ramp voltage. The VFB voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is calculated as follows :

Soft-Start time t_{SS} = 55μs + C_{SS} x 0.55 / 11μA + C_{SS} x 0.86 / I_{SS}

t_{SS} = SS rising to FB settled (T2 + T3)



T1 : EN delay, from EN go high to SS start rising, T1 = 55μs;
T2 : speed up SS, from SS rising to FB start rising, T2 = C_{SS} x 0.55 / 11μA;
T3 : normal SS, from FB rising to settled, T3 = C_{SS} x 0.86 / I_{SS};
V1 : offset voltage between SS and FB, V1 = 700mV;
PG go high after SSOK (SS = 1.9V)

Power Good Indication

The PGOOD pin is an open-drain output and is connected to an external pull-up resistor. It is controlled by a comparator, which the feedback signal V_{FB} is fed to. If V_{FB} is above 90% of the internal reference voltage after soft-start finished, the PGOOD pin will be in high impedance and V_{PGOOD} will be held high. Otherwise, the PGOOD output will be pulled low.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 20V
- Switch Node Voltage, LX ---------- –0.3V to (V_{IN} + 0.3V)
  < 50ns ---------- –5V to 25V
- BOOT Pin Voltage ---------- (V_{LX} – 0.3V) to (V_{IN} + 6.3V)
- BOOT to LX, V_{BOOT} – V_{LX} ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  TSOT-23-8 (FC) ---------- 1.667W
- Package Thermal Resistance (Note 2)
  TSOT-23-8 (FC), θ_{JA} ---------- 60°C/W
  TSOT-23-8 (FC), θ_{JC} ---------- 8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 4.5V to 18V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Supply Input Operating Voltage	V_{IN}		4.5	--	18	V
Under-Voltage Lockout Threshold	V_{UVLO}		--	3.7	--	V
Under-Voltage Lockout Threshold Hysteresis	ΔV_{UVLO}		--	300	--	mV
Supply Current						
Supply Current (Shutdown)	I_{SHDN}	V_{EN} = 0V	--	--	5	μA
Supply Current (Quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.85V	--	0.5	--	mA
Soft-Start						
Soft-Start Internal Charging Current	t_{SS}		--	6	--	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Enable Voltage						
Enable Voltage Threshold	V_{EN_R}	VEN rising	1.32	1.43	1.55	V
Enable Voltage Hysteresis			--	0.18	--	V
Feedback Voltage						
Feedback Reference Voltage	V_{REF}	4.5V ≤ VIN ≤ 18V,	0.753	0.765	0.777	V
Internal MOSFET						
High-Side On-Resistance	$R_{DS(ON)\_H}$	$V_{BOOT} - V_{LX}$ = 4.8V	--	120	--	mΩ
Low-Side On-Resistance	$R_{DS(ON)\_L}$		--	65	--	
Current Limit						
Current Limit	I_{LIM}	Valley current	2.5	3.2	--	A
Switching Frequency						
Switching Frequency	f_{SW}		--	650	--	kHz
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}		--	60	--	ns
Minimum Off-Time	t_{OFF_MIN}		--	240	--	
Output Under-Voltage Protections						
UVP Trip Threshold		UVP detect	57.5	62.5	67.5	%
		Hysteresis	--	10	--	
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C
Power Good						
Power Good Threshold	VPGOOD	FB rising	--	90	--	%
		FB falling	--	85	--	

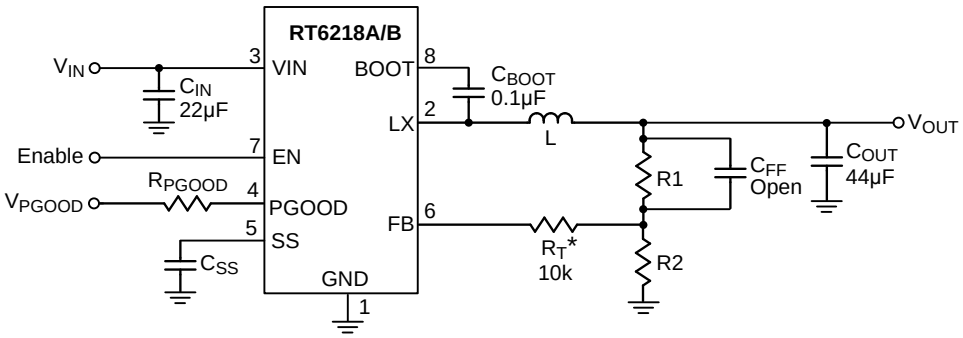
Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. The first layer is filled with copper. θ_{JA} is measured at the lead of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit



* Note : When C_{FF} is added, it is necessary to add R_T = 10k between feedback network and chip FB pin.

Table 1. Suggested Component Values (V_{IN} = 12V)

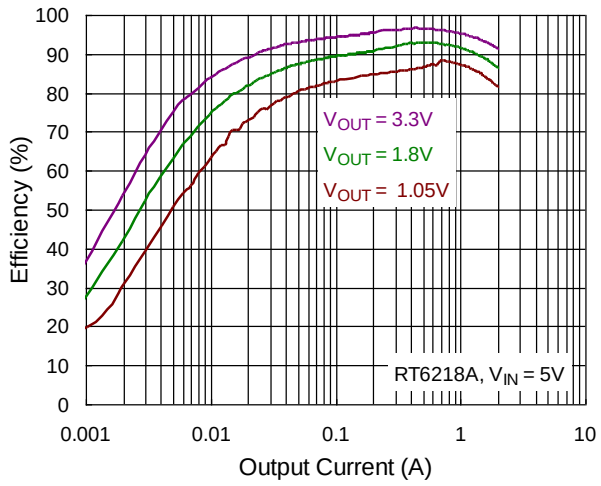
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (µH)	C_{OUT} (µF)	C_{FF} (pF)
1.05	10	27	2.2	44	--
1.2	20.5	36	2.2	44	--
1.8	40.2	30	3.6	44	--
2.5	40.2	18	3.6	44	22 to 68
3.3	40.2	12.1	4.7	44	22 to 68
5	40.2	7.32	4.7	44	22 to 68

Note 1 : All the input and output capacitances are the suggested values, which refer to the effective capacitances, and are subject to any de-rating effect, like a DC bias.

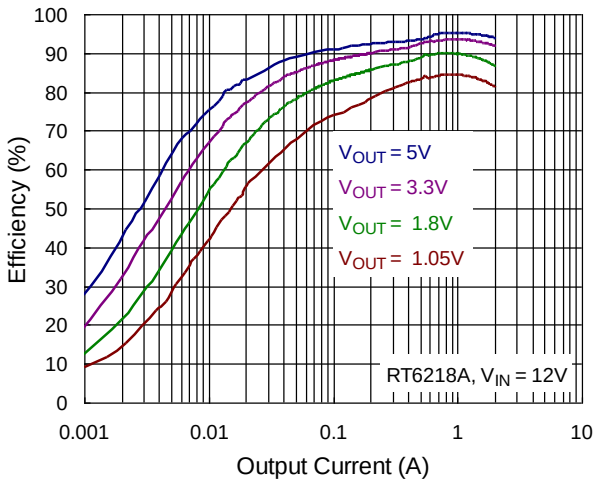
Note 2 : For lower output voltage applications, load transient responses can also be improved by adding a feedforward capacitor (C_{FF}, 22pF to 68pF).

Typical Operating Characteristics

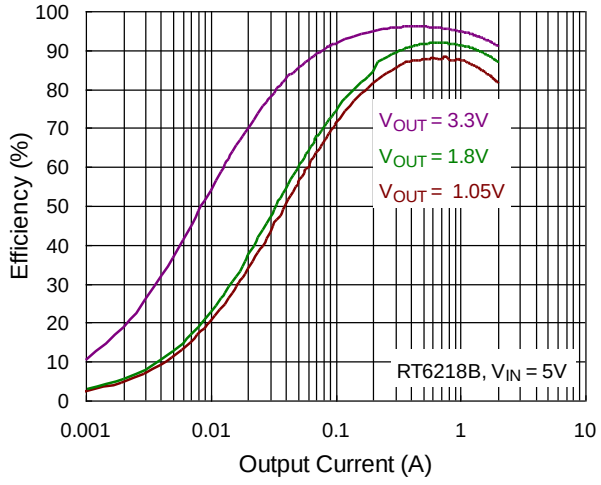
Efficiency vs. Output Current



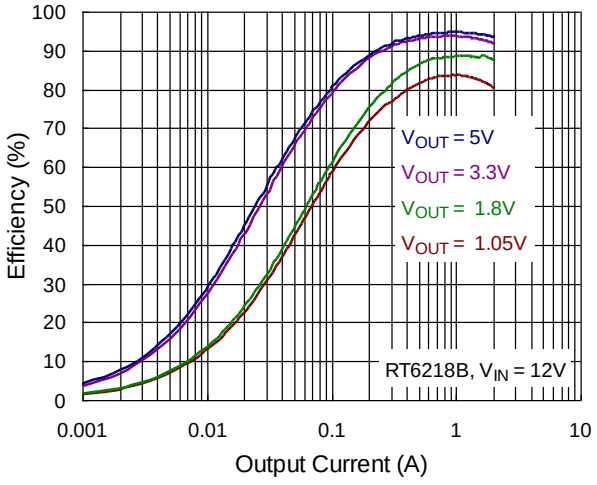
Efficiency vs. Output Current



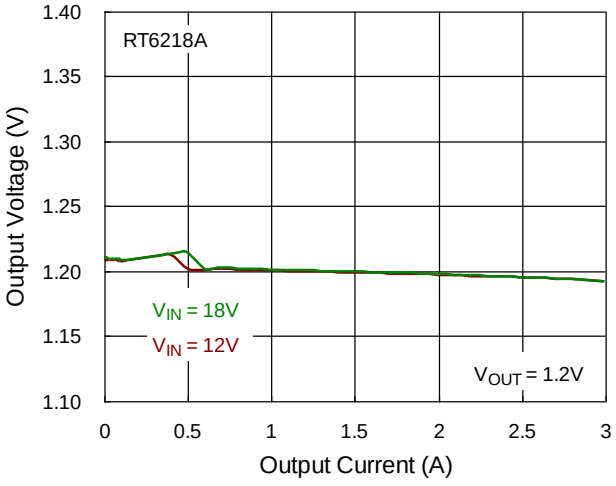
Efficiency vs. Output Current



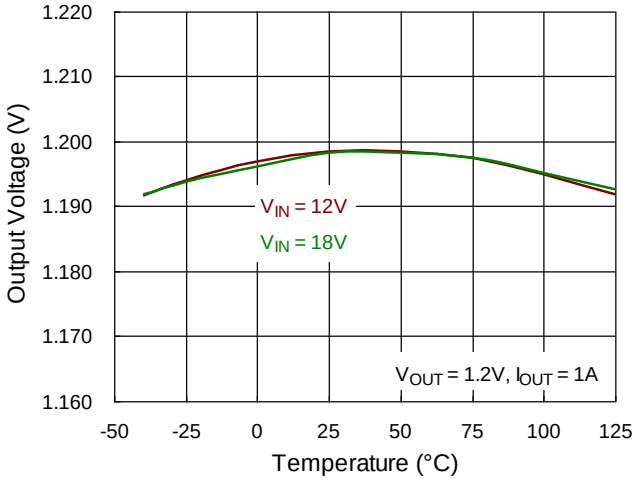
Efficiency vs. Output Current



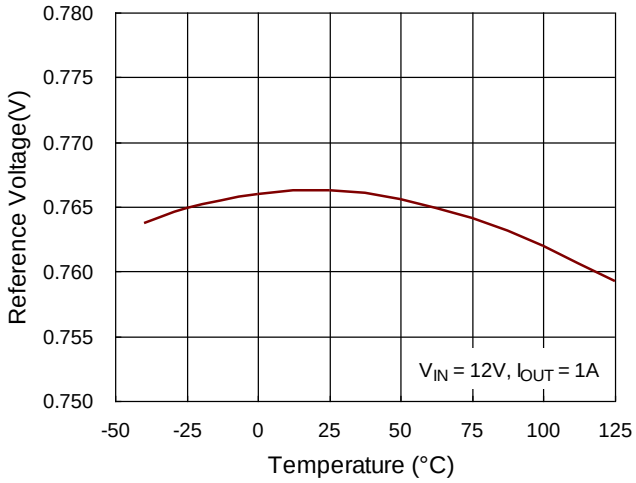
Output Voltage vs. Output Current



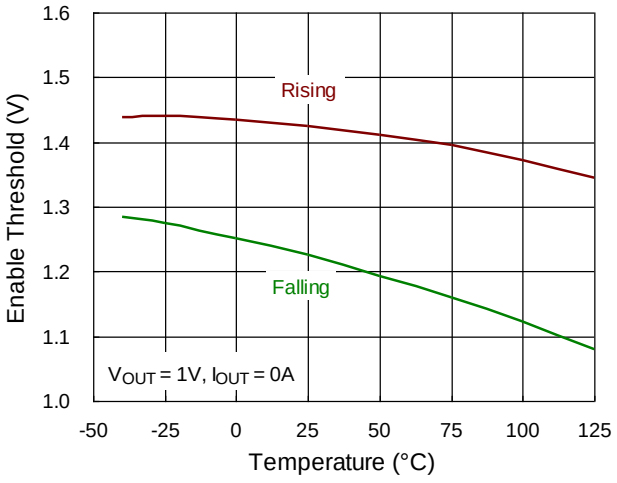
Output Voltage vs. Temperature



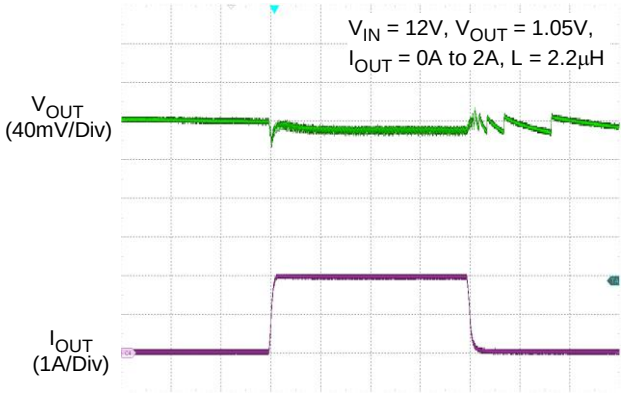
Reference Voltage vs. Temperature



Enable Threshold vs. Temperature

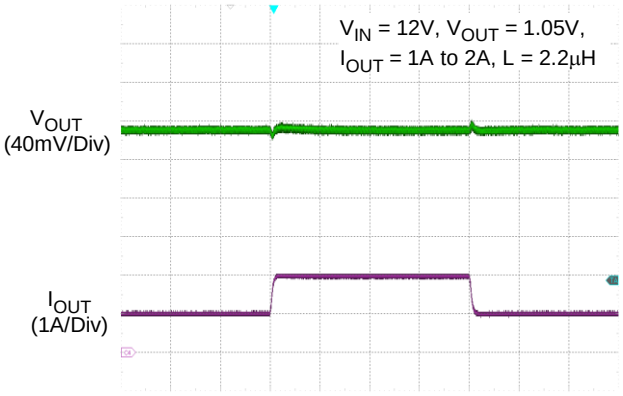


Load Transient Response



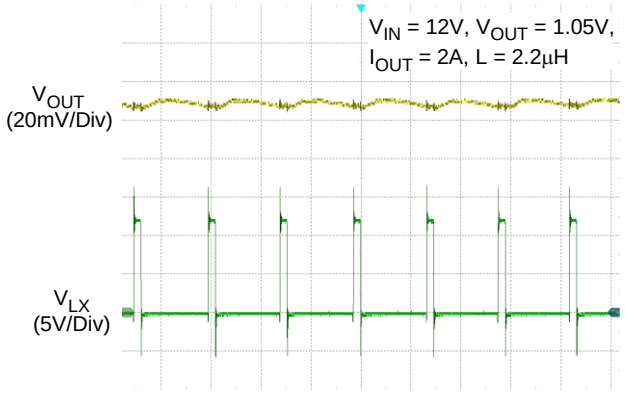
Time (100µs/Div)

Load Transient Response



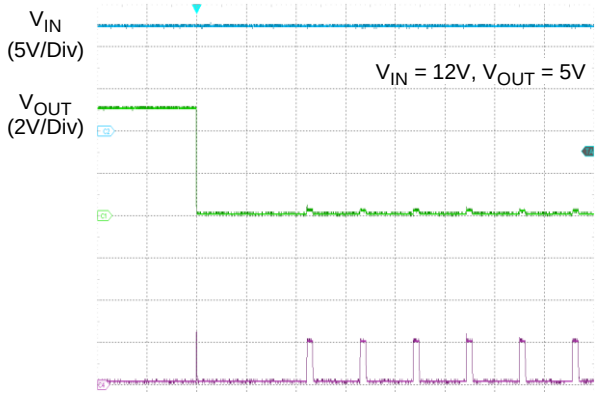
Time (100µs/Div)

Output Ripple Voltage



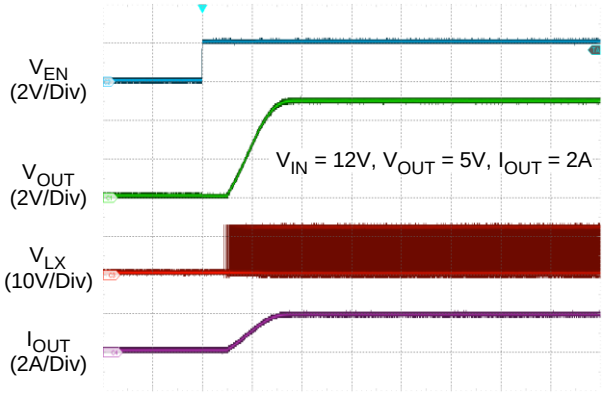
Time (1µs/Div)

Power On Then Short



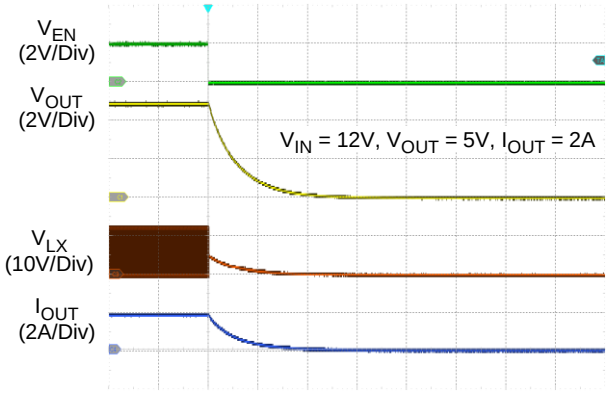
Time (10ms/Div)

Power On from EN



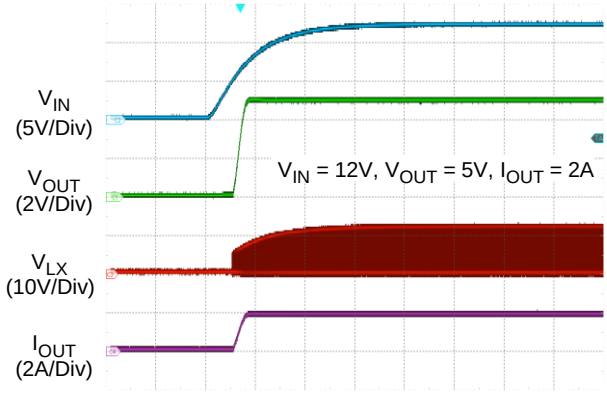
Time (1ms/Div)

Power Off from EN



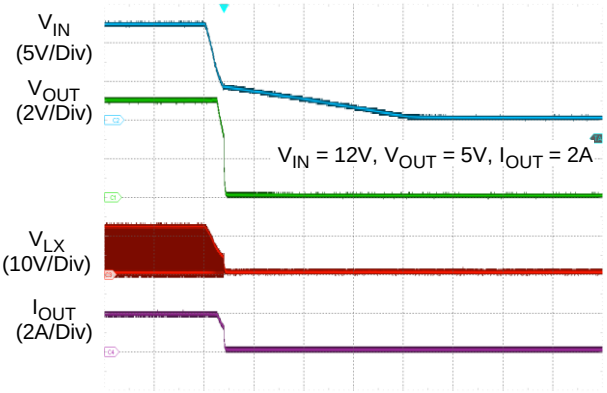
Time (200μs/Div)

Power On from VIN



Time (4ms/Div)

Power Off from VIN



Time (10ms/Div)

Application Information

Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response, but they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required and transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) about 20% to 50% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and } I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output under-voltage shutdown feature make this unnecessary for most applications.

$I_{L(PEAK)}$ should not exceed the minimum value of IC's upper current limit level or the IC may not be able to meet the desired output current. If needed, reduce the inductor ripple current (ΔI_L) to increase the average inductor current (and the output current) while ensuring that $I_{L(PEAK)}$ does not exceed the upper current limit level.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For low inductor core losses some type of ferrite core is usually best and a shielded core type, although possibly larger or more expensive, will probably give fewer EMI and other noise problems.

Considering the Typical Operating Circuit for 1.2V output at 2A and an input voltage of 12V, using an inductor ripple of 0.6A (30%), the calculated inductance value is :

$$L = \frac{1.2 \times (12 - 1.2)}{12 \times 650kHz \times 0.6A} = 2.77\mu H$$

The ripple current was selected at 0.6A and, as long as we use the calculated 2.77μH inductance, that should be the actual ripple current amount. The ripple current and required peak current as below :

$$\Delta I_L = \frac{1.2 \times (12 - 1.2)}{12 \times 650kHz \times 2.77\mu H} = 0.6A$$

$$\text{and } I_{L(PEAK)} = 2A + \frac{0.6A}{2} = 2.3A$$

For the 2.77μH value, the inductor's saturation and thermal rating should exceed 2.3A. Since the actual value used was 2.77μH and the ripple current exactly 0.6A, the required peak current is 2.3A.

Input Capacitor Selection

Input capacitors are needed to smooth out the RMS ripple current (I_{RMS}) imposed by the switching currents and drawn from the input power source, by reducing the ripple voltage amplitude seen at the input of the converters. The voltage rating of the input filter capacitors must be greater than the maximum input voltage. It's also important to consider the ripple current capabilities of capacitors.

The RMS ripple current (I_{RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) as the following equation :

$$I_{RMS} = I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

From the above, the maximum RMS input ripple current occurs at maximum output load, which will be used as the requirements to consider the current capabilities of the input capacitors. Furthermore, for a single phase buck converter, the duty cycle is approximately the ratio of output voltage to input voltage. The maximum ripple voltage usually occurs at 50% duty cycle, that is, V_{IN} = 2 x V_{OUT}. The maximum I_{RMS}, as I_{RMS} (Max), can be approximated as 0.5 x I_{OUT_MAX}, where I_{OUT_MAX} is the maximum rated output current. Besides, the variation of the capacitance value with temperature, DC bias voltage, switching frequency, and allowable peal-to-peak ripple voltage that reflects back to the input, also need to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases; also, higher switching frequency allows the use of input capacitors of smaller capacitance values.

Ceramic capacitors are most commonly used to be placed right at the input of the converter to reduce ripple voltage amplitude because only ceramic capacitors have extremely low ESR which is required to reduce the ripple voltage. Note that the capacitors need to be placed as close as to the input pins as possible for highest effectiveness. Ceramic capacitors are preferred also due to their low cost, small size, high RMS current ratings, robust inrush surge current capabilities, and low parasitic inductance, which helps reduce the high-frequency ringing on the input supply.

However, care must be taken when ceramic capacitors are used at the input, and the input power is supplied by a wall adapter, connected through a long and thin wire. When a load step occurs at the output, a sudden inrush current will surge through the long inductive wire, which can induce ringing at the device's power input and potentially cause a very large voltage spike at the VIN pin to damage the device. For applications where the input power is located far from the device input, it may be required that the low-ESR ceramic input capacitors be placed in parallel with a bulk capacitor of other types, such as tantalum, electrolytic, or polymer, to dampen the voltage ringing and overshoot at the input, caused by the long input power path and input ceramic capacitor.

It is suggested to choose capacitors with higher temperature ratings than required. Several ceramic capacitors may be parallel to meet application requirements, such as the RMS current, size, and height. The Typical Application Circuit can use one 22μF, or two 10μF and one high-frequency-noise-filtering 0.1uF low-ESR ceramic capacitors at the input.

Output Capacitor Selection

Output capacitance affects the output voltage of the converter, the response time of the output feedback loop, and the requirements for output voltage sag and soar. The sag occurs after a sudden load step current applied, and the soar occurs after a sudden load removal. Increasing the output capacitance reduces the output voltage ripple and output sag and soar, while it increases the response time that the output voltage feedback loop takes to respond to step loads, Therefore, there is a tradeoff between output capacitance and output response. It is recommended to choose a minimum output capacitance to meet the output voltage requirements of the converter, and have a quick transient response to step loads.

The ESR of the output capacitor affects the damping of the output filter and the transient response. In general, low-ESR capacitors are good choices due to their excellent capability in energy storage and transient performance. The RT6218A/B, therefore, is specially optimized for ceramic capacitors. Consider also DC bias and aging effects while selecting the output capacitor.

Output Ripple

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

For the Typical Operating Circuit for 1.2V output and an inductor ripple of 0.6A, with 2 x 22μF output capacitance each with about 5mΩ ESR including PCB trace resistance, the output voltage ripple components are :

$$V_{RIPPLE(ESR)} = 0.6A \times 5m\Omega = 3mV$$

$$V_{RIPPLE(C)} = \frac{0.6A}{8 \times 44\mu F \times 650kHz} = 2.62mV$$

$$V_{RIPPLE} = 3mV + 2.62mV = 5.62mV$$

Feed-Forward Capacitor (C_{FF})

The RT6218A/B is optimized for ceramic output capacitors and for low duty-cycle applications. This optimization makes circuit stability easy to achieve with reasonable output capacitors, but it also narrows the optimization of transient responses of the converter. For high output voltage (that is, high duty-cycle) applications, the FB voltage is highly attenuated from the output, the circuit's response becomes under-damped and transient response is slowed. A small feedforward capacitor (C_{FF}) can be introduced into the feedback network to speed up the transient response of high output voltage circuits. The feedforward capacitor is added across the upper FB divider resistor (as seen in Figure 1) to speed up the transient response without affecting the steady-state stability of the circuit.

To optimize transient response, a C_{FF} value is chosen so that the gain and phase boost of the feedback network increases the bandwidth of the converter, while still maintaining an acceptable phase margin. Generally, larger C_{FF} values provide higher bandwidth, but may result in an unacceptable phase margin or instability. Suitable feedforward capacitor values can be chosen from the table of Suggested Component Values.

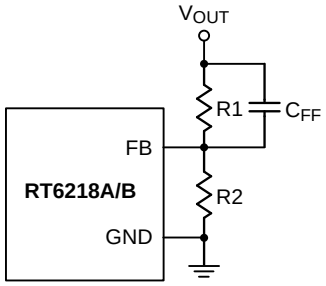


Figure 1. C_{FF} Capacitor Setting

Enable Operation (EN)

For automatic start-up the EN pin can be connected to VIN, through a 100kΩ resistor. Its large hysteresis band makes EN useful for simple delay and timing circuits. EN can be externally pulled to VIN by adding a resistor-capacitor delay (R_{EN} and C_{EN} in Figure 2). Calculate the delay time using EN's internal threshold where switching operation begins.

An external MOSFET can be added to implement digital control of EN when no system voltage above 2V is available (Figure 3). In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between VIN and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin. To prevent enabling circuit when VIN is smaller than the VOUT target value or some other desired voltage level, a resistive voltage divider can be placed between the input voltage and ground and connected to EN to create an additional input under voltage lockout threshold (Figure 4).

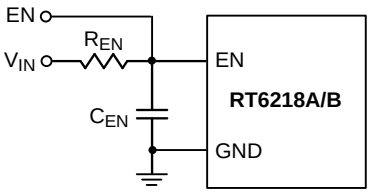


Figure 2. External Timing Control

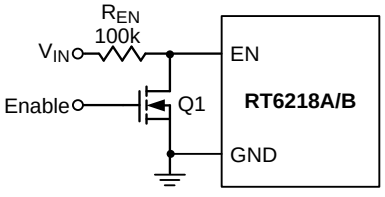


Figure 3. Digital Enable Control Circuit

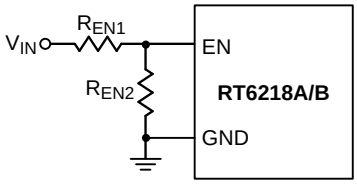


Figure 4. Resistor Divider for Lockout Threshold Setting

Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB. The output voltage is set according to the following equation :

V_{OUT} = 0.765V x (1 + R1 / R2)

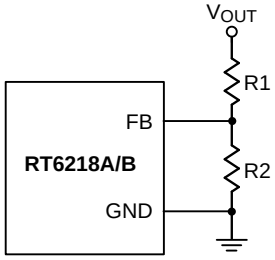


Figure 5. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. Choose R2 between 10kΩ and 100kΩ to minimize power consumption without excessive noise pick-up and calculate R1 as follows :

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For output voltage accuracy, use divider resistors with 1% or better tolerance.

External BOOT Bootstrap Diode

A bootstrap capacitor of 0.1μF low-ESR ceramic capacitor is connected between the BOOT and LX pins to supply the high-side gate driver. It is recommended to add an external bootstrap diode between an external 5V voltage supply and the BOOT pin to improve enhancement of the internal MOSFET switch and improve efficiency when the input voltage is below 5.5V. The bootstrap diode can be a low-cost one, such as 1N4148 or BAT54. The external 5V can be a fixed 5V voltage supply from the system, or a 5V output voltage generated by the RT6218A/B. Note that the BOOT voltage V_{BOOT} must be lower than 5.5V.

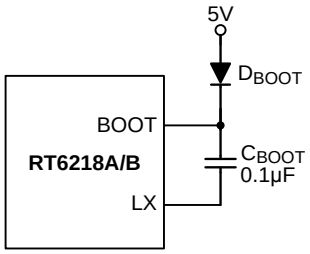


Figure 6. External Bootstrap Diode

Resistor at BOOT Pin

The gate driver of an internal power MOSFET, utilized as a high-side switch, is optimized for turning on the switch not only fast enough for reducing switching power loss, but also slow enough for minimizing EMI. The EMI issue is worse when the switch is turned on rapidly due to high di/dt noises induced. When the high-side switch is being turned off, the LX node will be discharged relatively slowly by the inductor current due to the presence of the dead time when both the high-side and low-side switches are turned off.

In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small (< 47Ω) resistor between the BOOT pin and the external bootstrap capacitor. This will slow down the rates of the high-side switch turn-on and the rise of V_{LX}. The recommended application circuit is shown in Figure 7, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} being placed between the BOOT pin and the capacitor/diode connection.

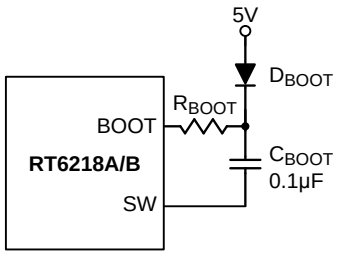


Figure 7. External Bootstrap Diode and Resistor at the BOOT Pin

Power-Good Output

The PGOOD pin is an open-drain power-good indication output and is to be connected to an external

voltage source through a pull-up resistor. The power-good function is activated after soft-start is finished and is controlled by the feedback signal V_{FB}. During soft-start, PGOOD is actively held low and only allowed to transition high after soft-start is over. If V_{FB} rises above a power-good threshold (V_{TH_PGLH}) (typically 90% of the target value), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. Once being started-up, if any internal protection is triggered, PGOOD will be pulled low to GND.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a TSOT-23-8 (FC) package, the thermal resistance, θ_{JA}, is 60°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (60°C/W) = 1.667W for a TSOT-23-8 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

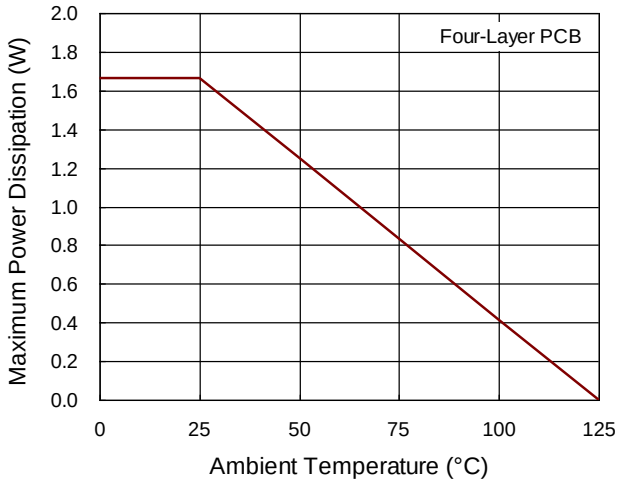


Figure 8. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the device.

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path comprising of input capacitor, high-side FET, inductor, and the output capacitor should be as short as possible. This practice is essential for high efficiency.
- Place the input MLCC capacitors as close to the VIN and GND pins as possible. The major MLCC capacitors should be placed on the same layer as the RT6218A/B.
- LX node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the LX node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Place the feedback components next to the FB pin.
- For better thermal performance, to design a wide and thick plane for GND pin or to add a lot of vias to GND plane.
- An example of PCB layout guide is shown from Figure 9.

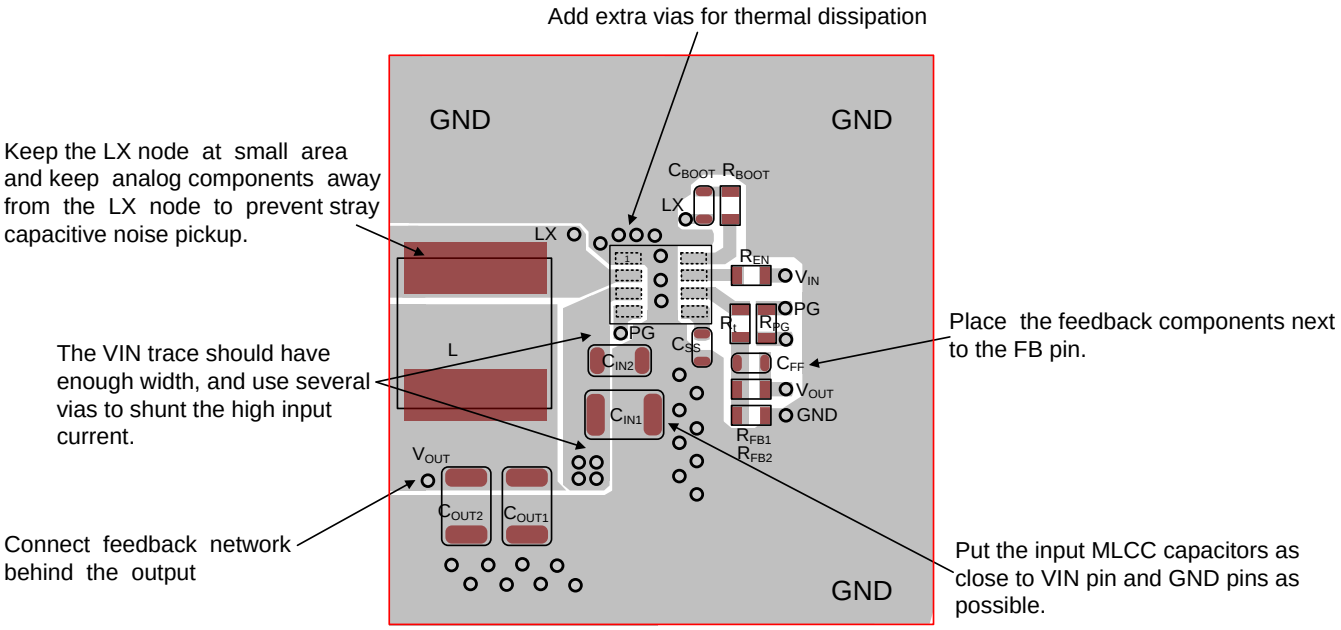
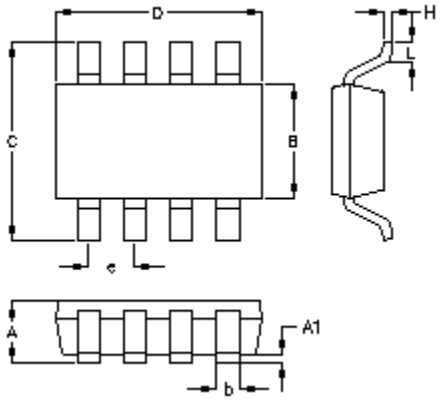


Figure 9. PCB Layout Guide for TSOT-23-8 package

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.220	0.380	0.009	0.015
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.585	0.715	0.023	0.028
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-8 (FC) Surface Mount Package

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