

LT8668SX-D --- Product Brief

High Definition Display Controller

1. Features

● USB Type-C

- Compliant with VESA DisplayPort alt mode on USB Type-C standard 1.0
- Compliant with USB power delivery specification 3.0
- Compliant with USB Type-C cable and connector specification 1.3
- Built-in dual CC controllers for charger and normal communication
- Data roles supported: DFP, UFP and DRP
- Power roles supported: source and sink

● DP1.4 Receiver

- Compliant with DisplayPort specification 1.4 for 1.62Gbps, 2.7Gbps, 5.4Gbps, 8.1Gbps
- Compliant Embedded DisplayPort specification version 1.4
- Support DisplayPort 1/2/4 lanes
- Support HDCP 1.3/2.2/2.3
- Support HDCP repeater
- Support 4K@60Hz
- Support HDR10 and HDR12
- Support FEC
- Support Adaptive-sync
- Support ASSR for eDP

● HDMI2.1 Receiver

- Compliant with HDMI2.1, HDMI2.0b, HDMI1.4 and DVI1.0
- Data rate up to 8Gbps
- Support HDCP 1.4/2.2/2.3
- Support HDCP repeater
- Support 4K@60Hz
- Support HDR10 and HDR12
- Support FEC

- Support CEC
- Integrated EDID shadow (max 512-byte)

● DP1.4 Transmitter

- Compliant with DisplayPort specification 1.4 for 1.62Gbps, 2.7Gbps, 5.4Gbps, 8.1Gbps
- Compliant Embedded DisplayPort specification version 1.4
- Support DisplayPort 1/2/4 lanes
- Support HDCP 1.3/2.2/2.3
- Support HDCP repeater
- Support 4K@60Hz
- Support HDR10 and HDR12
- Support FEC
- Support MCCA over AUX for eDP
- Support ASSR for eDP
- Support channel swap and polarity inversion

● HDMI2.1 Transmitter

- Compliant with HDMI2.1, HDMI2.0b, HDMI1.4 and DVI1.0
- Data rate up to 8Gbps
- Support HDCP 1.4/2.2/2.3
- Support HDCP repeater
- Support 4K@60Hz
- Support HDR10 and HDR12
- Support FEC
- Support CEC
- Support channel swap and polarity inversion

● Four-Port LVDS Transmitter

- Compatible with VESA and JEIDA standard
- Support 1/2/4 configurable ports
- 1 Clock lane and 3/4/5 configurable data lanes per port
- Data rate up to 1.2Gbps per data lane
- Support 4K@60Hz
- Programmable transmitter swing

- Support SSC
- Support channel swap and polarity inversion
- Support port swap
- **Four-Port MIPI® DSI/CSI Transmitter**
 - Compliant with D-PHY1.2 & DSI 1.3 & CSI-2 1.3, 1 clock lane, and 1/2/3/4 configurable data lanes, 2.5Gbps per data lane
 - Compliant with C-PHY1.0 & DSI-2 1.0 & CSI-2 2.0, 1/2/3 configurable data lanes, 5.7Gbps per data lane
 - Support 1/2/4 configurable ports
 - Support 4K@60Hz
 - Support overlap mode
 - DSI Support 16/20/24-bit YCbCr4:2:2, 24/30/36-bit RGB, 12-bit YCbCr4:2:0, compressed pixel stream
 - CSI Support RGB888/666, YUV422 8/10bit, YUV420 8bit(legacy)
 - Video stream copy mode for each port
 - Support channel swap and polarity inversion
 - Support port swap
- **eDP / eDPx Transmitter**
 - Support resolution up to 4K@60Hz
 - Support RGB/YUV 8/10-bit
 - Support eDP transmitter up to 8 lane with 5.4Gbps link rate
 - Support 8 pairs eDPx @3Gbps interface
 - Support MCCC over AUX for eDP
 - Support ASSR for eDP
 - Support SSC
 - Support channel swap and polarity inversion
- **Video Process**
 - Vertical blanking interval expansion
 - Video format conversion for I to P
 - Rotate 90, 270 degree
 - Frame rate control function
 - 3D format conversion: frame packing 3D to side by side 3D
 - Gamma and LUM adjustment
 - Zoom scaling up and down
 - Support font-based and bit-map OSD
- **Digital Audio Output**
 - I2S interface supporting 8-channel audio, with sample rates of 32~192 KHz and sample sizes of 16~24 bits
 - SPDIF interface supporting PCM, dolby digital, DTS digital audio at up to 192KHz frame rate
 - IEC60958 or IEC61937 compatible
- **Miscellaneous**
 - VESA DSC v1.2a (v1.1 compatible) decode and encode
 - CSC: RGB <-> YUV444 <-> YUV422<-> YUV420
 - Integrated 100/400KHz I2C slave
 - External oscillator 25MHz, +/-100ppm
 - Integrated microprocessor
 - Embedded SDRAM
 - Embedded SPI flash for firmware and HDCP keys
 - Support backlight control
 - Firmware update through SPI or I2C interface
 - Power supply: 3.3V for I/O and 1.1V for core

2. Description

LT8668SX-D can be configured to work under HDMI2.1 standard with maximum 8Gbps data rate.

LT8668SX-D also can be configured to work under DP1.4 with up to 8.1Gbps data rate.

For LVDS output, LT8668SX-D can be configured as single, dual or quad-port LVDS with 1 high-speed clock lane, and 3~5 high-speed data lanes, operating at maximum 1.2Gbps per lane, which can support a total bandwidth of up to 24Gbps. LT8668SX-D supports flexible video data mapping path for 2D and side by side 3D applications.

For MIPI output, LT8668SX-D features configurable single-port or dual-port or quad-port MIPI®DSI/CSI with 1 high-speed clock lane and 1~4 high-speed data lanes operating at maximum 2.5Gbps per lane with D-PHY, which can support a total bandwidth of up to 40Gbps for four port. Also support 5.7Gbps per lane with C-PHY, which can support a total bandwidth of up to 68.4Gbps for four port.

For eDP output, it consists of 8 data lanes, supporting RBR (1.62Gbps), HBR (2.7Gbps) and HBR2 (5.4Gbps) link speeds. The build-in optional SSC function reduces EMI effect on EMI-concerned system application.

For eDPx output, it consists of 8 data lanes, with operating at maximum 3Gbps per lane, can support 4K@60Hz.

For video process, LPDDR controller is built-in and bandwidth up to 3733Mbps, support 2Gb x16 SDRAM organization.

Two digital audio output interfaces are available I2S and SPDIF. The I2S interface supports 8-ch LPCM and the SPDIF interface supports 2-ch LPCM or compressed

audio, both at maximum 192 KHz sample rate.

The device is capable of automatic operation which is enabled by an integrated microprocessor that uses an embedded SPI flash for firmware storage. System control is also available through the configuration I2C slave interface.

LT8668SX-D is fabricated in advanced CMOS process and implemented in 12mmx12mm BGA288 package.

3. Applications

- Display System on Motherboard, Monitor
- Display System for PCs and embedded applications Display



Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Product Name	Part Number	Product Status	Package	Bonding Wire	Grade	Operating Temperature Range	Stack Die Option	Packing Method
LT8668SX-D	LT8668SX-D_U2B03AEI	Preview	BGA288 (12*12)	Au	Consumer	TBD	I	Tray

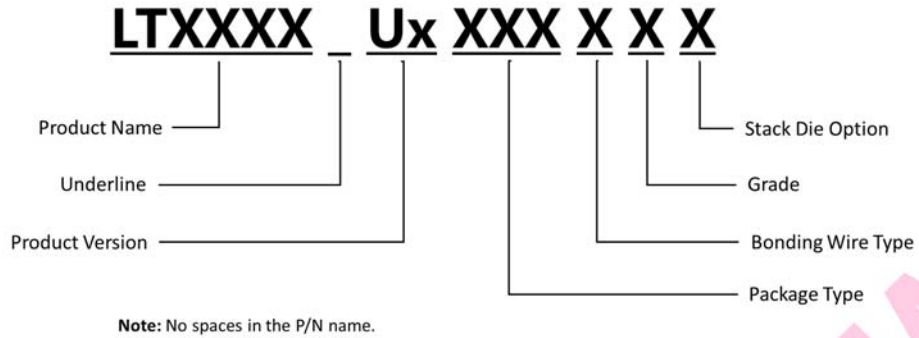


Figure 4.1 Part Number Naming Rules

LONTIUM CONFIDENTIAL

Copyright © 2021 Lontium Semiconductor Corporation, All rights reserved.

Lontium Semiconductor Proprietary & Confidential

This document and the information it contains belong to Lontium Semiconductor. Any review, use, dissemination, distribution or copying of this document or its information outside the scope of a signed agreement with Lontium is strictly prohibited.

LONTIUM DISCLAIMS ALL WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING THOSE OF NONINFRINGEMENT, MERCHANTABILITY, TITLE AND FITNESS FOR A PARTICULAR PURPOSE. CUSTOMERS EXPRESSLY ASSUME THEIR OWN RISK IN RELYING ON THIS DOCUMENT.

LONTIUM PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE IN LIFE SUPPORT APPLIANCES, DEVICES OR SYSTEMS WHERE A MALFUNCTION OF A LONTIUM DEVICE COULD RESULT IN A PERSONAL INJURY OR LOSS OF LIFE.

Lontium assumes no responsibility for any errors in this document, and makes no commitment to update the information contained herein. Lontium reserves the right to change or discontinue this document and the products it describes at any time, without notice. Other than as set forth in a separate, signed, written agreement, Lontium grants the user of this document no right, title or interest in the document, the information it contains or the intellectual property it embodies.

Trademarks

Lontium™ 龙迅™ and ClearEdge™ is a registered trademark of Lontium Semiconductor. All other brand names, product names, trademarks, and registered trademarks contained herein are the property of their respective owners.

Visit our corporate web page at: www.lontiumsemi.com

Technical support: support@lontium.com

Sales: sales@lontium.com