

#### High Speed USB 2.0 (480Mbps)DPDT Analog Switch

#### **General Description**

The SL7227 is a DPDT (double-pole/double-throw)analog switch. It operates from a 1.8V to 4.3V single power supply. Each switch of the SL7227 is bidirectional, which can ensure that the high speed signals have little or no attenuation at the outputs. The SL7227 features high speed, low power and wide bandwidth. The high performances make it very suitable for multiple applications, such as cellular phones and computer peripherals, etc.

The SL 7227 has a power-off protection. It can prevent accidental signal leakage and ensure system reliability under power-down and over-voltage conditions. In addition, the device is capable of withstanding a  $V_{BUS}$  short to D+ or D- when the device is either powered on or powered off because of the special circuitry on the D+/D- pins.

The SL 7227 is available in Green UTQFN-1.8  $\times$  1.4-10L and MSOP-10 packages. It operates over an ambient temperature range of -40°C to +85°C.

#### Features

- Supply Voltage Range: 1.8V to 4.3V
- On-Resistance: 5Ω (TYP) at 3.0V
- Off-Isolation: -51dB (R<sub>L</sub> =  $50\Omega$ , f = 250MHz)
- Crosstalk: -26dB ( $R_L = 50 \Omega$ , f = 250MHz)
- Fast Switching Times at  $V_{CC} = 3.3V$ :
  - $\succ$  t<sub>ON</sub> = 20ns (TYP)
  - >  $t_{OFF} = 18ns (TYP)$
- Break-Before-Make Switching
- Rail-to-Rail Input and Output Operation
- Power-Off and Power-On Protections
- -40 °C to +85 °C Operating Temperature Range
- Available in Green UTQFN-1.8×1.4-10L and MSOP-10 Packages

### Applications

- Cellular Phones
- Digital Cameras
- Portable Equipment
- Computer Peripherals
- Battery-Powered Systems
- Routes Signals for USB 2.0 Full-Speed



# **Pin Configurations**





# **Pin Description**

UTQFN1.8X1.4-10L	MSOP-10	Symbol	Description	
Pin Nun	ıber			
1,2	3,4	D+,D-		
4,5	6,7	HSD1+,HSD1-	Data ports	
6,7	8,9	HSD2+,HSD2-		
3	5	GND	Ground	
8	10	OE	Output Enable Control Pin	
9	1	V <sub>CC</sub>	Positive Power Supply Pin	
10	2	S	Select Input Pin.	

### **Ordering Information**

Type Number	Package	Quantity
SL7227XF10	QFN1.8*1.4-10L	3000PCS
SL7227XV10	MSOP-10	3000PCS



Symbol	parameter	Rating	UNIT
	V <sub>CC</sub> to GND	0 to4.6	V
	Analog, Digital Voltage Range	-0.3 to (V <sub>CC</sub> +0.3)	V
	Continuous Current HSDn or Dn	±50	mA
	Peak Current HSDn or Dn	±100	mA
$T_A$	Operating Temperature Range	-40 to 85	°C
$T_J$	Junction Temperature	+150	°C
T <sub>STG</sub>	Storage Temperature Range .	-65 to 150	°C
$T_{\rm L}$	Lead Temperature (Soldering, 10s)	+260	°C
	НВМ	4000	V
ESD Susceptibility	ММ	400	V

# Absolute Maximum Ratings ( $T_A = 25^{\circ}C$ )

#### 备注:

1.Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. This integrated circuit can be damaged if ESD protections are not considered carefully. SLKOR recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications. 3.SLKOR reserves the right to make any change in circuit design, or specifications without prior notice.



## **Electrical Characteristics**

### $(V_{CC} = +3.3V, Full = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ typical values are at } T_A = +25^{\circ}C, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Тетр	Min.	Тур.	Max.	Units
Analog Sw	vitch						
V <sub>IS</sub>	Analog I/O Voltage (HSD1+, HSD1-, HSD2+, HSD2-)		Full	0		V <sub>CC</sub>	v
R <sub>ON</sub> On-Resistance	$V_{CC} = 3.0V, V_{IS} = 0V \text{ to } 0.4V,$	+25℃		5	8	Ω	
	OII-RESIStance	$I_D = 8mA$ , Test Circuit 1	Full			9	Ω
	On-Resistance	$V_{CC} = 3.0V, V_{IS} = 0V \text{ to } 0.4V,$ $I_D = 8\text{mA}, \text{ Test Circuit } 1$	+25°C		0.3	0.7	Ω
$\Delta R_{0N}$	Match Between Channels		Full			0.8	Ω
R <sub>FLAT(ON)</sub> On-Resistance Flatness	$V_{CC} = 3.0V$ , $V_{IS} = 0V$ to 1.0V, $I_D = 8$ mA, Test Circuit 1	+25℃		1	1.8	Ω	
		Full			2	Ω	
I <sub>OFF</sub>	Power Off Leakage Current (D+, D-)	$V_{CC} = 0V, V_D = 0V \text{ to } 3.6V,$ $V_S, V_{OE} = 0V \text{ or } 3.6 \text{ V}$	Full			1	μΑ
Ісст	Increase in I <sub>CC</sub> per Control Voltage	$V_{CC} = 3.6V,$ $V_{S}$ or $V_{OE} = 2.6V$	Full			5	μA
I <sub>HSD2(OFF</sub> ) I <sub>HSD1(OFF</sub> )	Source Off Leakage Current	$V_{CC} = 3.6V, V_{IS} = 3.3V/0.3V, V_D = 0.3V/3.3V$	Full			1	μA
$I_{\rm HSD2(ON)} \\ I_{\rm HSD1(ON)}$	Channel On Leakage Current	$\label{eq:V_CC} \begin{split} V_{CC} &= 3.6V,  V_{IS} = 3.3V/0.3V, \\ V_{D} &= 3.3V/0.3V \text{ or floating} \end{split}$	Full			1	μA
Digital Inp	outs				1	1	
$\mathbf{V}_{\mathrm{IH}}$	Input High Voltage		Full	1.6			V
VIL	Input Low Voltage		Full			0.3	V
I <sub>IN</sub>	Input Leakage Current	$V_{CC} = 3.0V, V_S, V_{OE} = 0V \text{ or}$ $V_{CC}$	Full			1	μΑ



## **Electrical Characteristics**

 $(V_{CC} = +3.3V, Full = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ typical values are at } T_A = +25^{\circ}C, \text{ unless otherwise noted})$ 

Symbol	Parameter	Conditions	Temp	Min.	Тур.	Max.	Units
Dynamic	Dynamic Characteristics						
ton	Turn-On Time	$V_{IS} = 0.8V,$ $R_{L} = 50\Omega,$	+25°C		20		ns
t <sub>OFF</sub>	Turn-Off Time	$C_L = 10 pF$ , Test Circuit 2	+25°C		18		ns
t <sub>D</sub>	Break-Before- Make Time Delay	$V_{IS} = 0.8V,$ $R_{L} = 50\Omega,$ $C_{L} = 10pF,$ Test Circuit 3	+25°C		4		ns
t <sub>PD</sub>	Propagation Delay	$\begin{split} R_{\rm L} &= 50\Omega, \\ C_{\rm L} &= 10 p {\rm F} \end{split}$	+25°C		0.5		ns
O <sub>ISO</sub>	Off Isolation	Signal = 0dBm, $R_L = 50\Omega$ , f = 250MHz, Test Circuit 4	+25°C		-51		dB
X <sub>TALK</sub>	Channel-to- Channel Crosstalk	Signal = 0dBm, $R_L = 50\Omega$ , f = 250MHz, Test Circuit 5	+25°C		-26		dB
BW	-3dB Bandwidth	Signal = 0dBm, $R_L = 50\Omega$ , $C_L = 5pF$ , Test Circuit 6	+25°C		500		MHz
t <sub>skew</sub>	Channel-to- Channel Skew	$R_{\rm L} = 50\Omega,$ $C_{\rm L} = 10 \rm{pF}$	+25°C		130		ps
Q	Charge Injection Select Input to Common I/O	$V_{G} = GND,$ $C_{L} = 1.0nF,$ $R_{G} = 0\Omega,$ $Q = C_{L} \times$ $V_{OUT}, Test$ Circuit 7	+25°C		1.5		рС
Con	HSD+, HSD-, D+, D- ON Capacitance	f=1MHz	+25°C		11		pF
Power Requirements							
V <sub>CC</sub>	Power Supply Range		Full	1.8		4.3	V
I <sub>CC</sub>	Power Supply Current	$V_{CC} = 3.0V,$ $V_{S}, V_{OE} = 0V$ or $V_{CC}$	Full			1	μΑ



## **Block Diagram**



Figure 2 Block Diagram

## **Function Table**

OE	S	HSD1+,HSD1-	HSD2+,HSD2-
0	0	ON	OFF
0	1	OFF	ON
1	Х	OFF	OFF

NOTE: Switches shown for logic "0" input.



### **Application Information**

#### 1. Power-Off Protection

When D+ or D- is shorted to V BUS, there is a special protection circuit inside the SL7227, so that the device will not be damaged within 24 hours. In case of power-down or over-voltage event, the protection circuit can prevent the leakage signal on D+/D- pins to ensure the reliability of the system.,

#### 2. USB2.0 Signal Quality Compliance Test Results

Required Tests

> Overall result:
Pass!
> Signal eye:
Eye passes
> EOP width: 7.91 bits
EOP width passes
> Measured signaling rate: 480.0551MHz
Signal rate passes
> Rising Edge Rate:
889.18V/µs (719.77ps equivalent rise-time)
Passes

#### 3. Power-On Protection

The USB 2.0 specification requires USB device to ensure that the device will not be damaged even if V BUS short-circuit occurs during data transmission. Therefore, under over-voltage conditions, the SL7227 will limit the current flowing back to the V CC track, and the current will not exceed the safe operating range

#### **Additional Information**

Consecutive jitter range: -61.770ps to 39.668ps, RMS jitter 21.900ps Paired JK jitter range: -47.800ps to 42.890ps, RMS jitter 21.591ps Paired KJ jitter range: -50.590ps to 49.704ps, RMS jitter 23.281ps



## **Test Circuits**







Test Circuit 2 Switching Times (ton,toff)



Test Circuit 3 Break-Before-Make Time(t<sub>D</sub>)



## **Test Circuits**







Chanel-to-Chanel  $\bar{Crosstalk}$ =-20log(V<sub>HSDn</sub>/V<sub>OUT</sub>)





Test Circuit 6 -3dB Bandwidth



# **Test Circuits**



Test Circuit 7 Charge Injection (Q)



## **Package Information**

#### QFN1.8\*1.4-10L



#### MSOP-10

