Low Voltage Synchronous Boost Regulator

Features

- Input voltage — 0.7V to 4.5V
- Minimum start-up voltage — 0.85V
- Output voltage — fixed at 3.3V; adjustable from 1.8V to 5.0V
- Peak input current limit — 1.2A
- Output current at 3.3 V_{OUT} — 80mA with V_{IN} = 1.0V, 190mA with V_{IN} = 1.5V
- Forced PWM operation at all loads
- Efficiency up to 94%
- Internal synchronous rectifier
- No forward conduction path during shutdown
- Switching frequency — 1.2MHz
- Soft-start startup current limiting
- Shutdown current — 0.1µA (typ)
- Ultra-thin 1.5 × 2.0 × 0.6 (mm) MLPD-UT-6 package
- Lead-free and halogen-free
- WEEE and RoHS compliant

Applications

- MP3 players
- Smart phones and cellular phones
- Palmtop computers and handheld instruments
- PCMCIA cards and memory cards
- Digital cordless phones
- Personal medical products
- Wireless VoIP phones
- Small motors

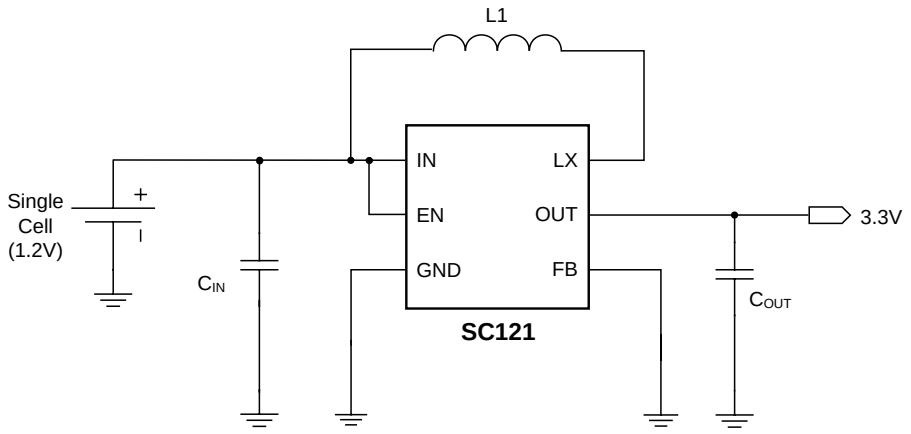
Description

The SC121 is a high efficiency, low noise, synchronous step-up DC-DC converter that provides boosted voltage levels in low-voltage handheld applications. The wide input voltage range allows use in systems with single NiMH or alkaline battery cells as well as in systems with higher voltage battery supplies. It features an internal 1.2A switch and synchronous rectifier to achieve up to 94% efficiency and to eliminate the need for an external Schottky diode. The output voltage can be set to 3.3V with internal feedback, or to any voltage within the specified range using a standard resistor divider.

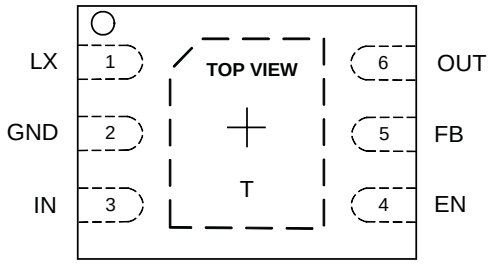
The SC121 operates exclusively in Pulse Width Modulation (PWM) mode for low ripple and fixed-frequency switching. Output disconnect capability is included to reduce leakage current, improve efficiency, and eliminate external components sometimes needed to disconnect the load from the supply during shutdown.

Low quiescent current is maintained with a high 1.2MHz operating frequency. Small external components and the space saving MLPD-UT-6, 1.5×2.0×0.6 (mm) package make this device an excellent choice for small handheld applications that require the longest possible battery life.

Typical Application Circuit



Pin Configuration — MLPD-UT



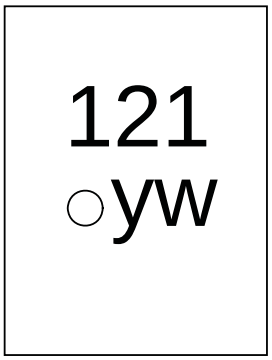
MLPD-UT; 1.5×2, 6 LEAD
θ_{JA} = 84°C/W

Ordering Information

Device	Package
SC121ULTRT[1][2]	MLPD-UT-6 1.5×2
SC121EVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Lead-free packaging, only. Device is WEEE and RoHS compliant, and halogen-free.

Marking Information — MLPD-UT



MLPD-UT; 1.5×2, 6 LEAD
yw = date code

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Absolute Maximum Ratings

IN, OUT, LX, FB (V) ..... -0.3 to +6.0
EN (V) ..... -0.3 to (V_{IN} + 0.3)
ESD Protection Level[1] (kV) 4

Recommended Operating Conditions

Ambient Temperature Range (°C)..... -40 to +85
V_{IN} (V) ..... 0.7 to 4.5
V_{OUT} (V) ..... 1.8 to 5.0

Thermal Information

Thermal Res. MLPD, Junction-Ambient[2] (°C/W) 84
Maximum Junction Temperature (°C) 150
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise noted V_{IN} = 2.5V, C_{IN} = C_{OUT} = 22µF, L_1 = 4.7µH, T_A = -40 to +85°C. Typical values are at T_A = 25°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		0.7		4.5	V
Minimum Startup Voltage	V_{IN-SU}	I_{OUT} < 1mA, T_A = 0°C to 85°C		0.85		V
Shutdown Current	I_{SHDN}	T_A = 25°C, V_{EN} = 0V		0.1	1	µA
Operating Supply Current[1]	I_Q	I_{OUT} = 0, V_{EN} = V_{IN}		3.5		mA
Internal Oscillator Frequency	f_{OSC}			1.2		MHz
Maximum Duty Cycle	D_{MAX}			90		%
Minimum Duty Cycle	D_{MIN}				20	%
Output Voltage	V_{OUT}	V_{FB} = 0V		3.3		V
Adjustable Output Voltage Range	V_{OUT_RNG}	For V_{IN} such that D_{MIN} < D < D_{MAX}	1.8		5.0	V
Regulation Feedback Reference Voltage Accuracy (Internal or External Programming)	$V_{Reg-Ref}$		-1.5		1.5	%
FB Pin Input Current	I_{FB}	V_{FB} = 1.2V			0.1	µA
Startup Time	t_{SU}			1		ms

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Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
P-Channel ON Resistance	R_{DSP}	V_{OUT} = 3.3V		0.6		Ω
N-Channel ON Resistance	R_{DSN}	V_{OUT} = 3.3V		0.5		Ω
N-Channel Current Limit	$I_{LIM(N)}$	V_{IN} = 3.0V	0.9	1.2		A
P-Channel Startup Current Limit	$I_{LIM(P)-SU}$	$V_{IN} > V_{OUT}$, $V_{EN} > V_{IH}$		150		mA
LX Leakage Current PMOS	I_{LXP}	T_A = 25°C, V_{LX} = 0V			1	µA
LX Leakage Current NMOS	I_{LXN}	T_A = 25°C, V_{LX} = 3.3V			1	µA
Logic Input High	V_{IH}	V_{IN} = 3.0V	0.85			V
Logic Input Low	V_{IL}	V_{IN} = 3.0V			0.2	V
Logic Input Current High	I_{IH}	$V_{EN} = V_{IN}$ = 3.0V			1	µA
Logic Input Current Low	I_{IL}	V_{EN} = 0V	-0.2			µA

NOTES:

(1) Quiescent operating current is drawn from OUT while in regulation. The quiescent operating current projected to IN is approximately $I_Q \times (V_{OUT}/V_{IN})$.

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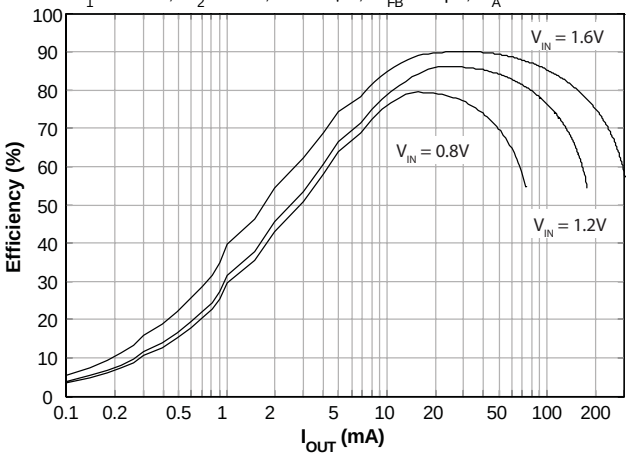
Typical Characteristics — V_{OUT} = 1.8V

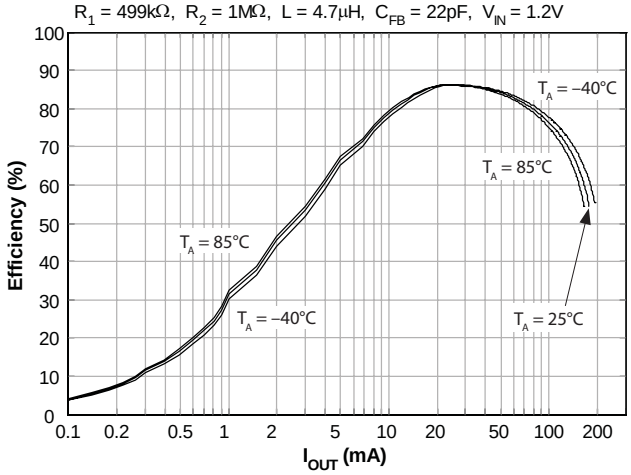
Efficiency vs. I_{OUT} (V_{OUT} = 1.8V)

R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, C_{FB} = 22pF, T_A = 25°C



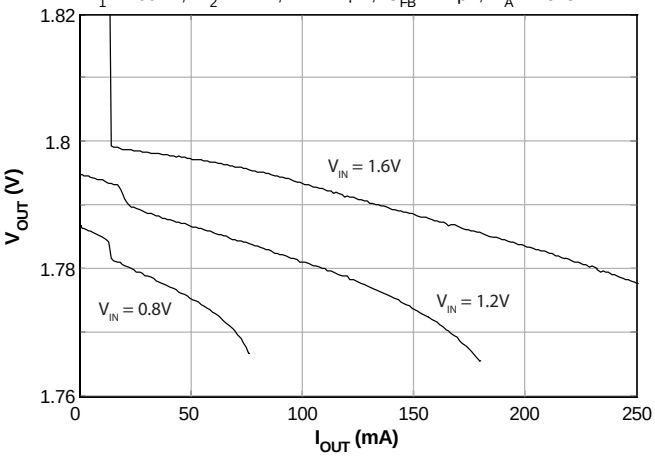
Efficiency vs. I_{OUT} (V_{OUT} = 1.8V)

R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, C_{FB} = 22pF, V_{IN} = 1.2V



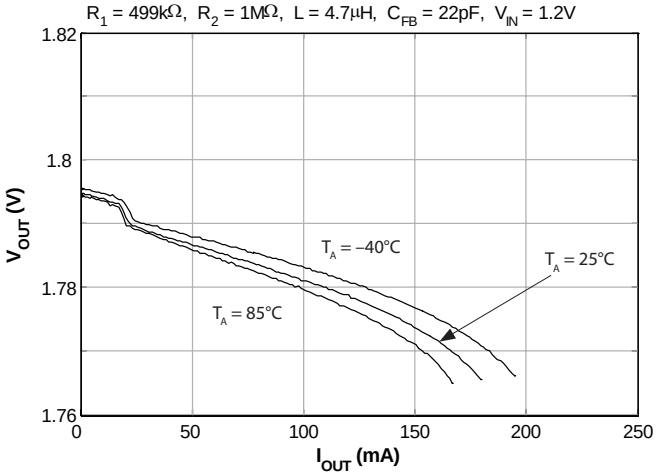
Load Regulation (V_{OUT} = 1.8V)

R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, C_{FB} = 22pF, T_A = 25°C



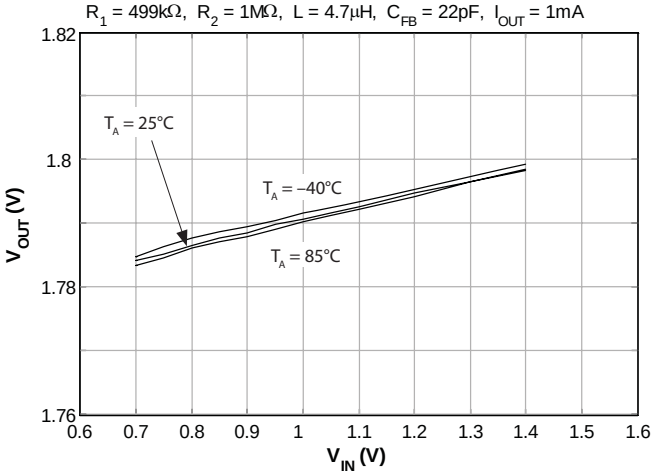
Load Regulation (V_{OUT} = 1.8V)

R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, C_{FB} = 22pF, V_{IN} = 1.2V



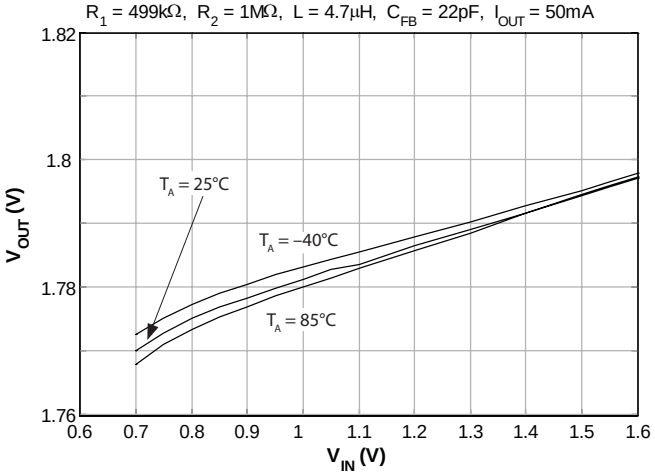
Line Regulation — Low Load (V_{OUT} = 1.8V)

R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, C_{FB} = 22pF, I_{OUT} = 1mA



Line Regulation — High Load (V_{OUT} = 1.8V)

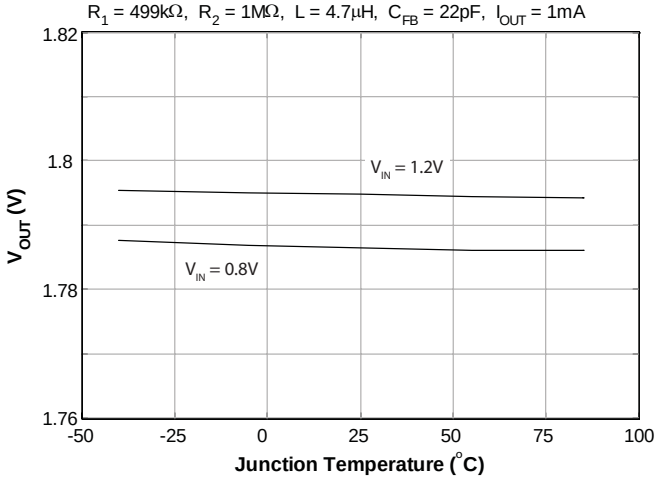
R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, C_{FB} = 22pF, I_{OUT} = 50mA



Typical Characteristics — V_{OUT} = 1.8V (continued)

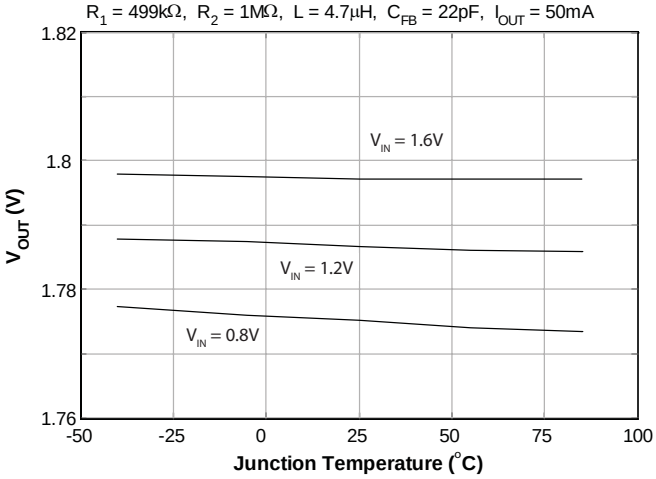
Temperature Reg. — Low Load (V_{OUT} = 1.8V)

R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, C_{FB} = 22pF, I_{OUT} = 1mA



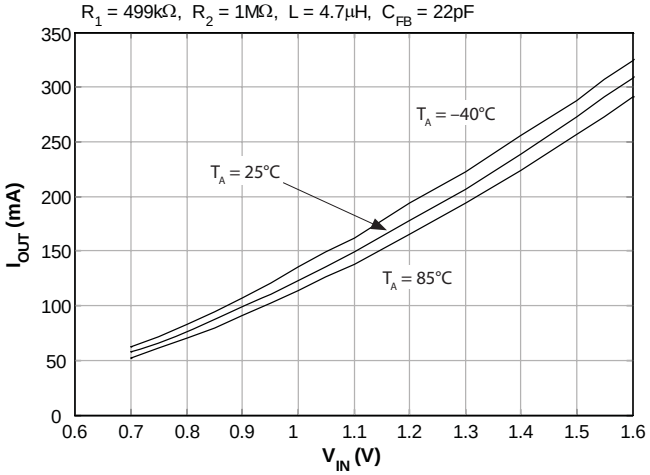
Temperature Reg. — High Load (V_{OUT} = 1.8V)

R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, C_{FB} = 22pF, I_{OUT} = 50mA



Max. I_{OUT} vs. V_{IN} (V_{OUT} = 1.8V)

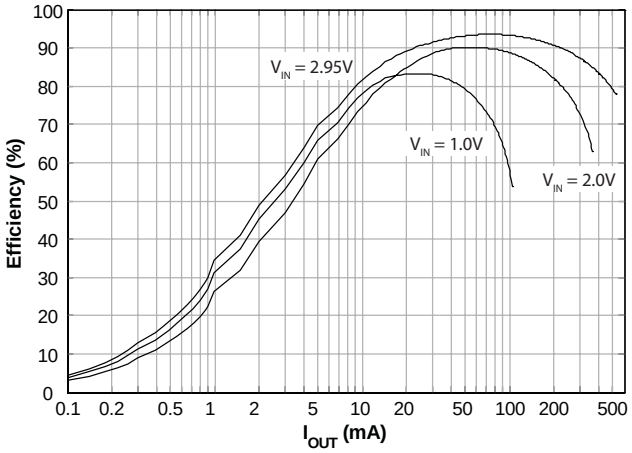
R_1 = 499kΩ, R_2 = 1MΩ, L = 4.7µH, C_{FB} = 22pF



Typical Characteristics — V_{OUT} = 3.3V

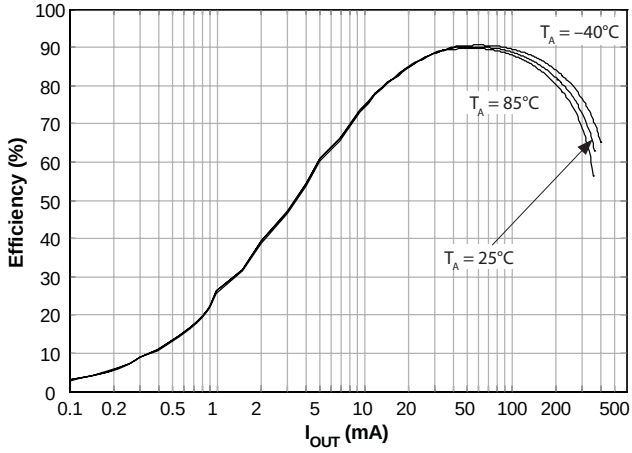
Efficiency vs. I_{OUT} (V_{OUT} = 3.3V)

FB grounded, L = 4.7µH, T_A = 25°C



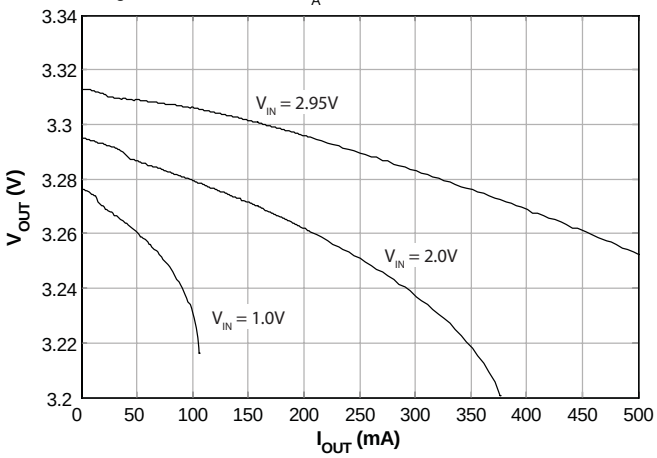
Efficiency vs. I_{OUT} (V_{OUT} = 3.3V)

FB grounded, L = 4.7µH, V_{IN} = 2V



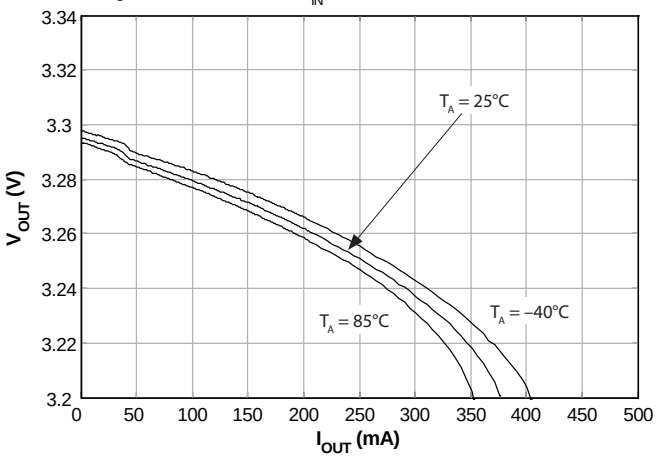
Load Regulation (V_{OUT} = 3.3V)

FB grounded, L = 4.7µH, T_A = 25°C



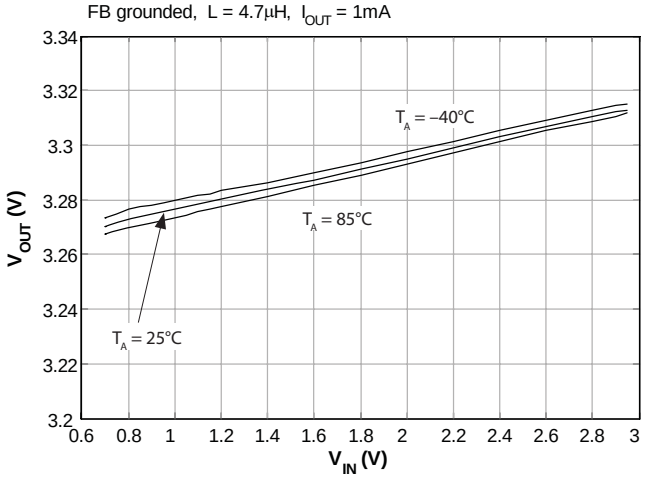
Load Regulation (V_{OUT} = 3.3V)

FB grounded, L = 4.7µH, V_{IN} = 2V



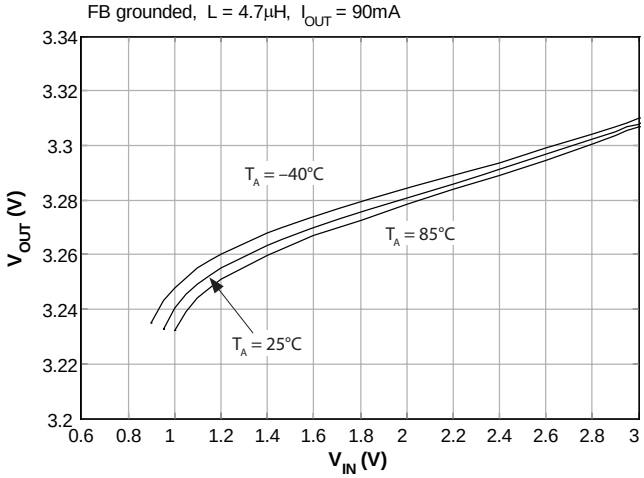
Line Regulation — Low Load (V_{OUT} = 3.3V)

FB grounded, L = 4.7µH, I_{OUT} = 1mA



Line Regulation — High Load (V_{OUT} = 3.3V)

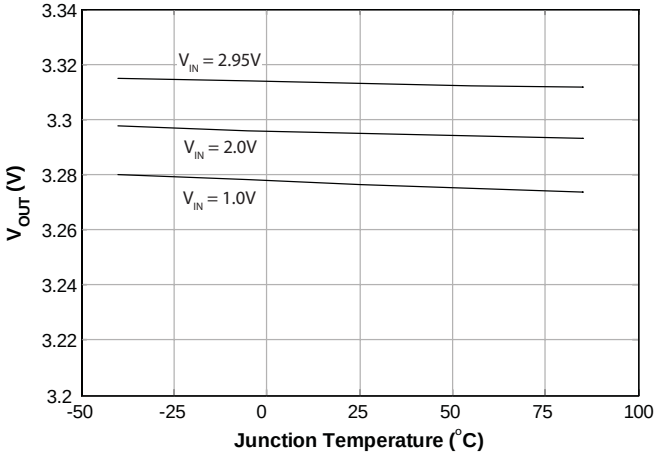
FB grounded, L = 4.7µH, I_{OUT} = 90mA



Typical Characteristics — V_{OUT} = 3.3V (continued)

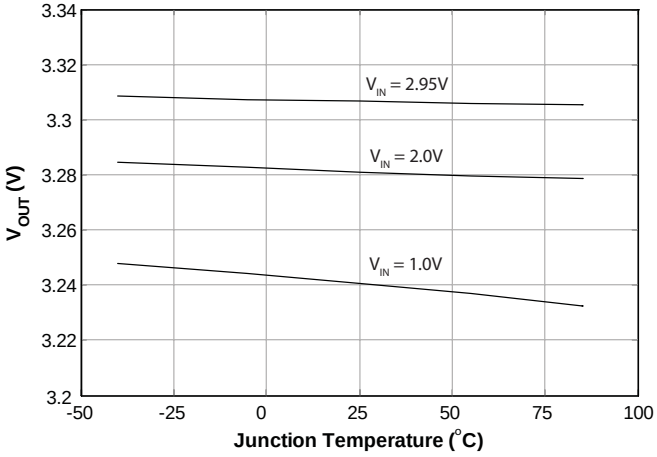
Temperature Reg. — Low Load (V_{OUT} = 3.3V)

FB grounded, L = 4.7µH, I_{OUT} = 1mA



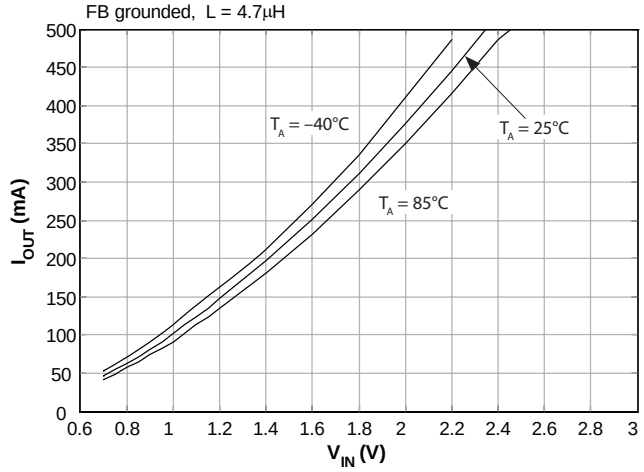
Temperature Reg. — High Load (V_{OUT} = 3.3V)

FB grounded, L = 4.7µH, I_{OUT} = 90mA



Max. I_{OUT} vs. V_{IN} (V_{OUT} = 3.3V)

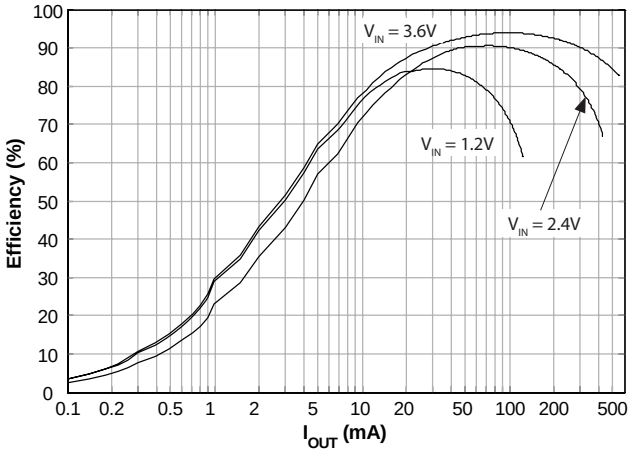
FB grounded, L = 4.7µH



Typical Characteristics — V_{OUT} = 4.0V

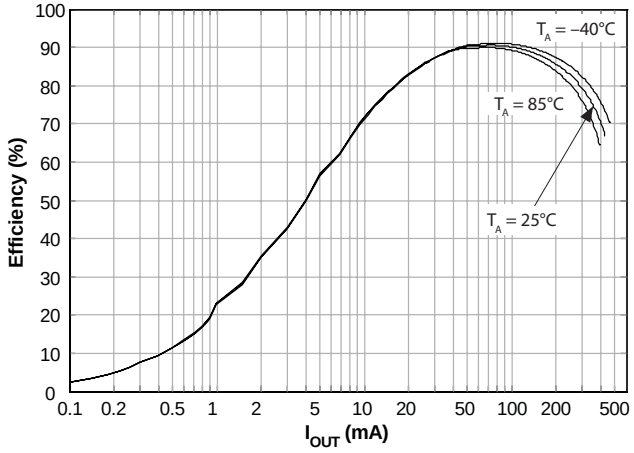
Efficiency vs. I_{OUT} (V_{OUT} = 4.0V)

R_1 = 976kΩ, R_2 = 412kΩ, L = 4.7µH, C_{FB} = 22pF, T_A = 25°C



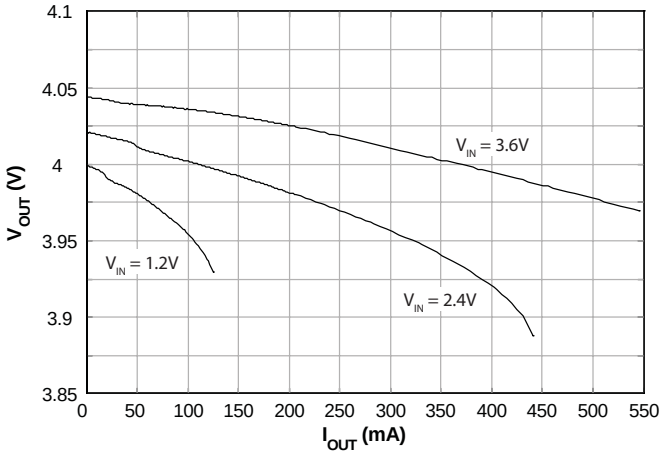
Efficiency vs. I_{OUT} (V_{OUT} = 4.0V)

R_1 = 976kΩ, R_2 = 412kΩ, L = 4.7µH, C_{FB} = 22pF, V_{IN} = 2.4V



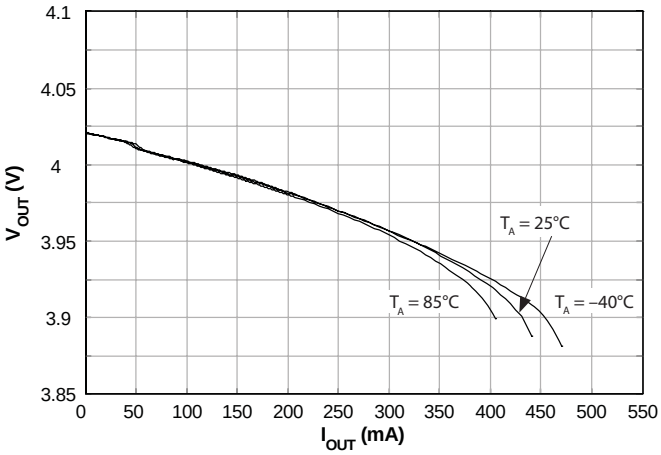
Load Regulation (V_{OUT} = 4.0V)

R_1 = 976kΩ, R_2 = 412kΩ, L = 4.7µH, C_{FB} = 22pF, T_A = 25°C



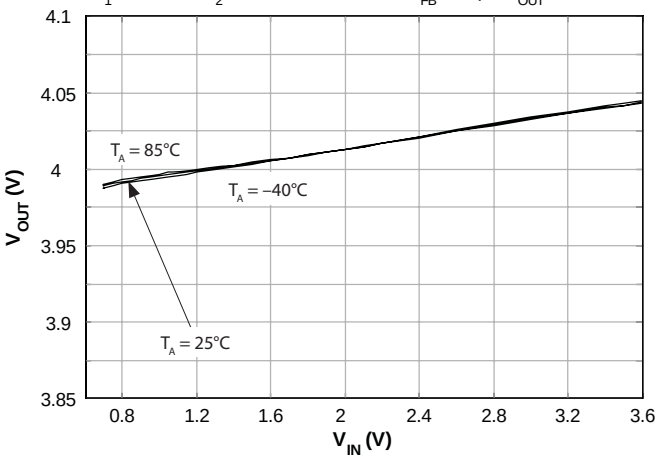
Load Regulation (V_{OUT} = 4.0V)

R_1 = 976kΩ, R_2 = 412kΩ, L = 4.7µH, C_{FB} = 22pF, V_{IN} = 2.4V



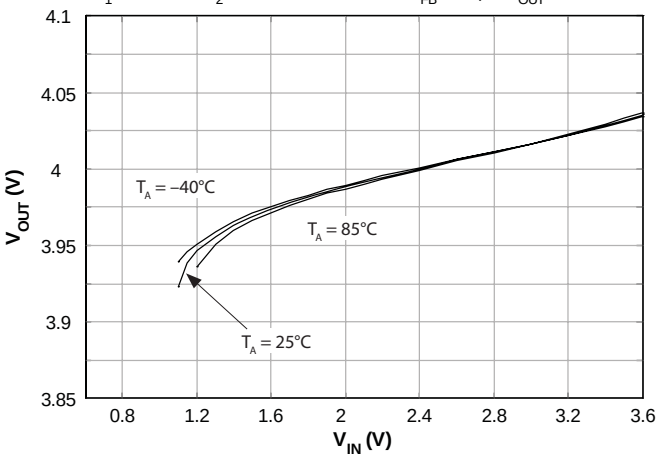
Line Regulation — Low Load (V_{OUT} = 4.0V)

R_1 = 976kΩ, R_2 = 412kΩ, L = 4.7µH, C_{FB} = 22pF, I_{OUT} = 1mA



Line Regulation — High Load (V_{OUT} = 4.0V)

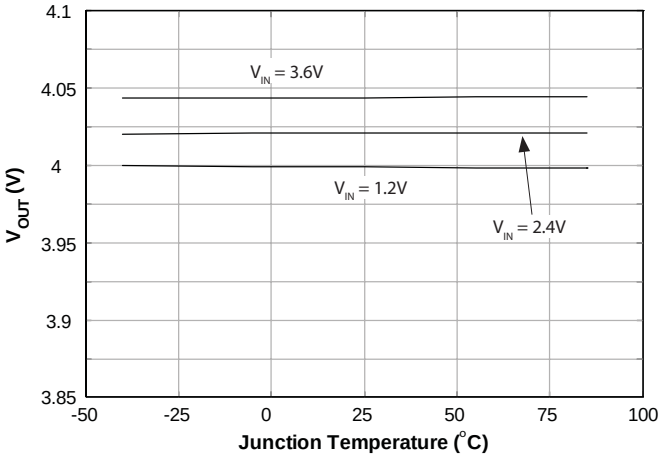
R_1 = 976kΩ, R_2 = 412kΩ, L = 4.7µH, C_{FB} = 22pF, I_{OUT} = 110mA



Typical Characteristics — V_{OUT} = 4.0V (continued)

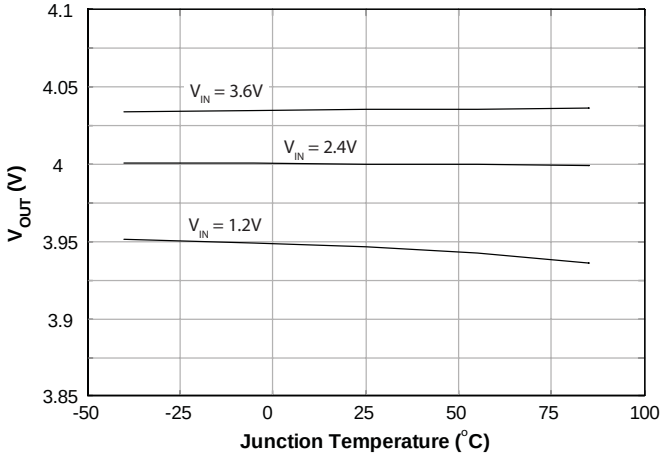
Temperature Reg. — Low Load (V_{OUT} = 4.0V)

R_1 = 976kΩ, R_2 = 412kΩ, L = 4.7µH, C_{FB} = 22pF, I_{OUT} = 1mA



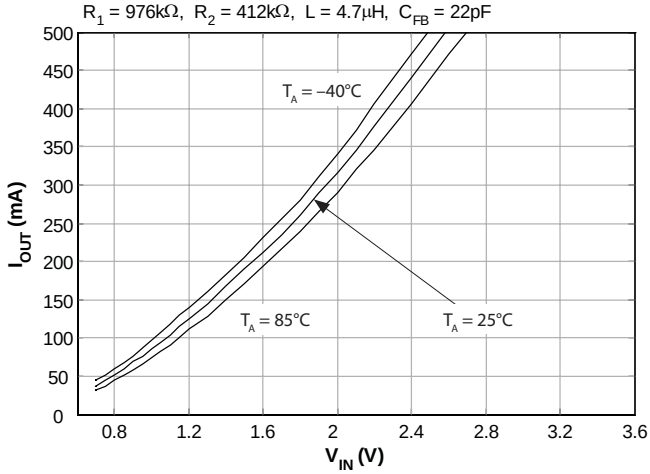
Temperature Reg. — High Load (V_{OUT} = 4.0V)

R_1 = 976kΩ, R_2 = 412kΩ, L = 4.7µH, C_{FB} = 22pF, I_{OUT} = 110mA



Max. I_{OUT} vs. V_{IN} (V_{OUT} = 4.0V)

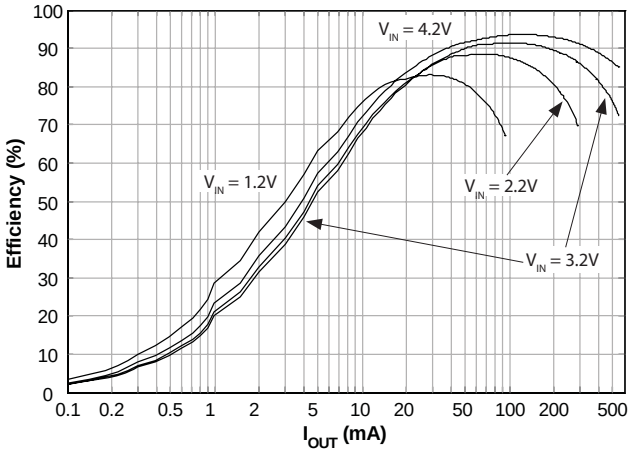
R_1 = 976kΩ, R_2 = 412kΩ, L = 4.7µH, C_{FB} = 22pF



Typical Characteristics — V_{OUT} = 5.0V

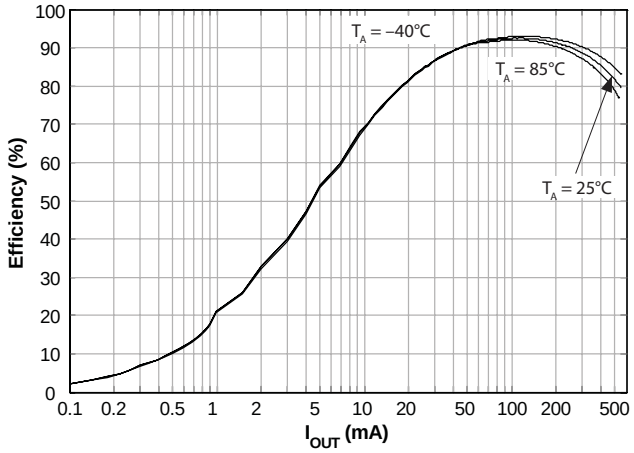
Efficiency vs. I_{OUT} (V_{OUT} = 5.0V)

R_1 = 931kΩ, R_2 = 294kΩ, L = 4.7µH, C_{FB} = 22pF, T_A = 25°C



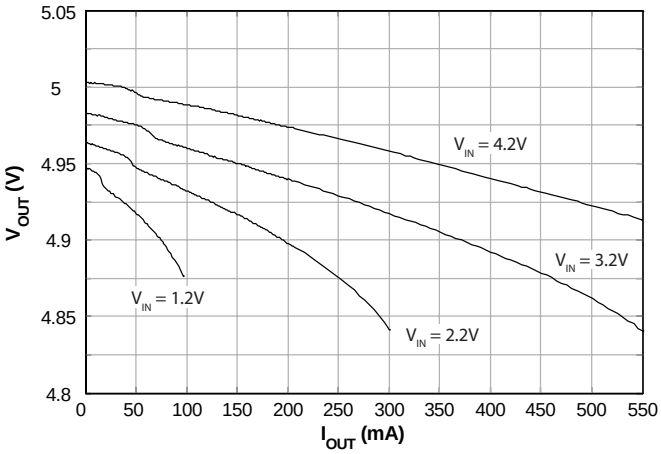
Efficiency vs. I_{OUT} (V_{OUT} = 5.0V)

R_1 = 931kΩ, R_2 = 294kΩ, L = 4.7µH, C_{FB} = 22pF, V_{IN} = 3.6V



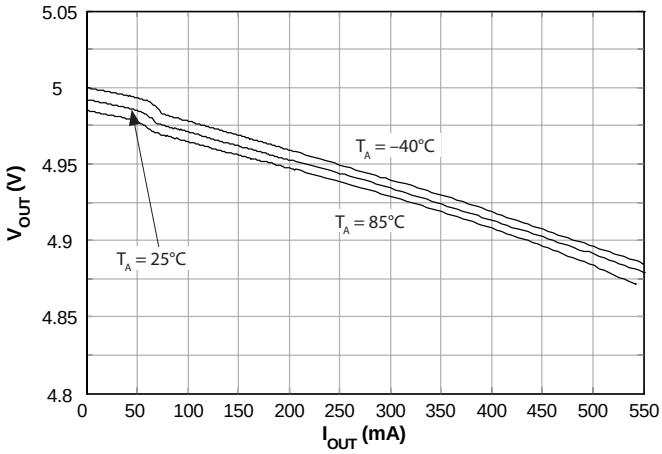
Load Regulation (V_{OUT} = 5.0V)

R_1 = 931kΩ, R_2 = 294kΩ, L = 4.7µH, C_{FB} = 22pF, T_A = 25°C



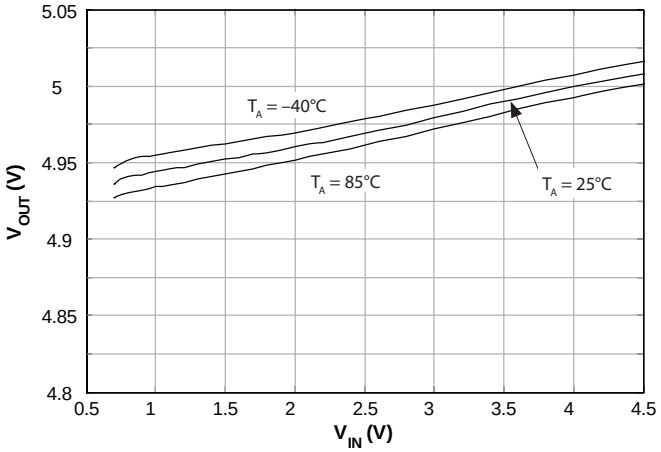
Load Regulation (V_{OUT} = 5.0V)

R_1 = 931kΩ, R_2 = 294kΩ, L = 4.7µH, C_{FB} = 22pF, V_{IN} = 3.6V



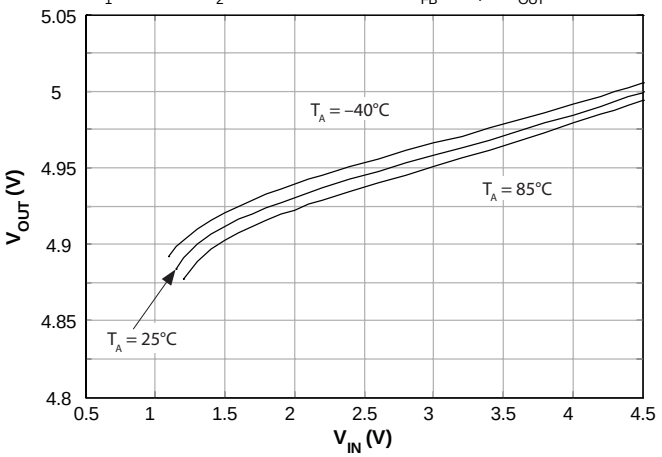
Line Regulation — Low Load (V_{OUT} = 5.0V)

R_1 = 931kΩ, R_2 = 294kΩ, L = 4.7µH, C_{FB} = 22pF, I_{OUT} = 1mA



Line Regulation — High Load (V_{OUT} = 5.0V)

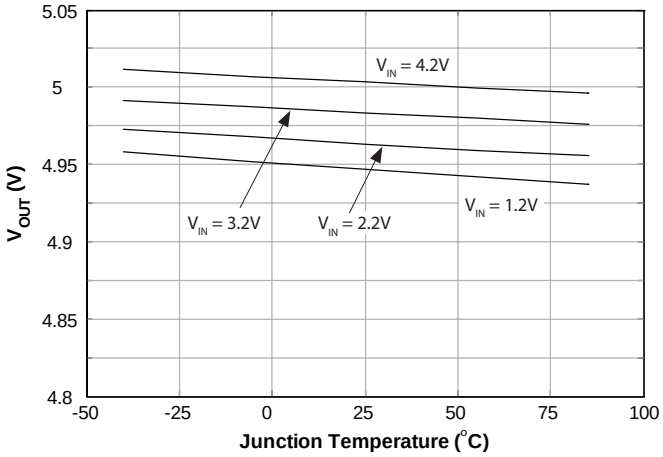
R_1 = 931kΩ, R_2 = 294kΩ, L = 4.7µH, C_{FB} = 22pF, I_{OUT} = 85mA



Typical Characteristics — V_{OUT} = 5.0V (continued)

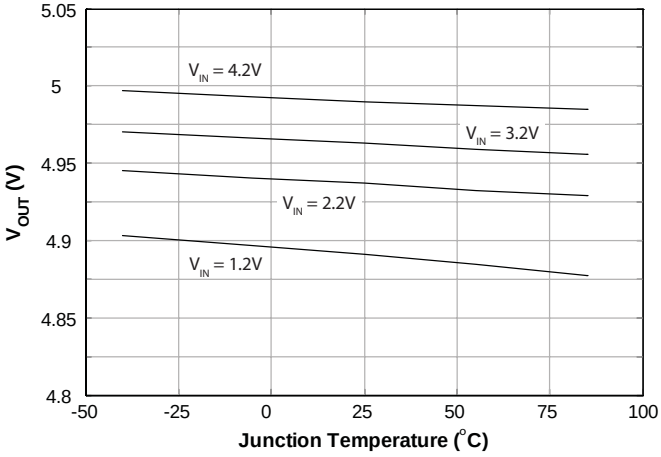
Temperature Reg. — Low Load (V_{OUT} = 5.0V)

R_1 = 931kΩ, R_2 = 294kΩ, L = 4.7µH, C_{FB} = 22pF, I_{OUT} = 1mA



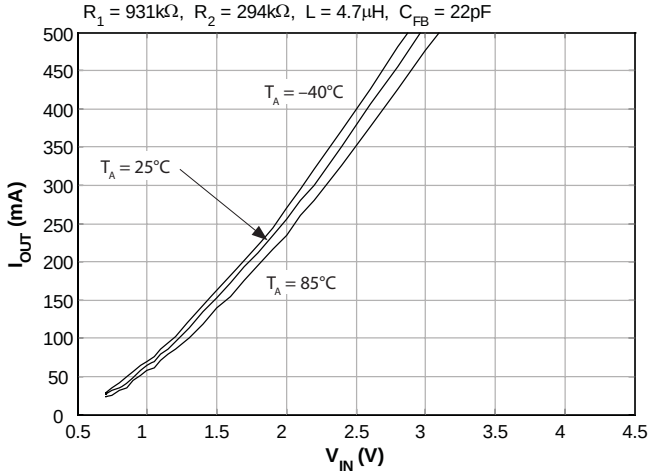
Temperature Reg. — High Load (V_{OUT} = 5.0V)

R_1 = 931kΩ, R_2 = 294kΩ, L = 4.7µH, C_{FB} = 22pF, I_{OUT} = 85mA



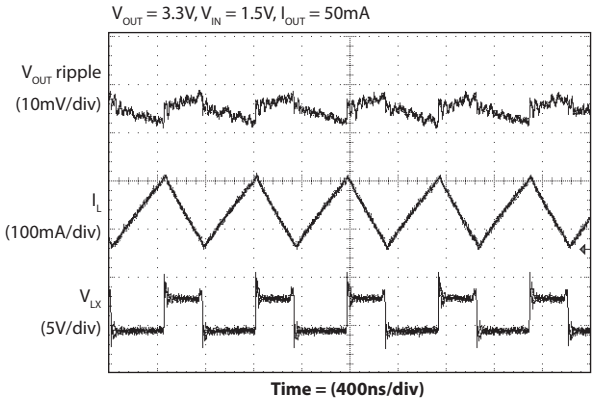
Max. I_{OUT} vs. V_{IN} (V_{OUT} = 5.0V)

R_1 = 931kΩ, R_2 = 294kΩ, L = 4.7µH, C_{FB} = 22pF

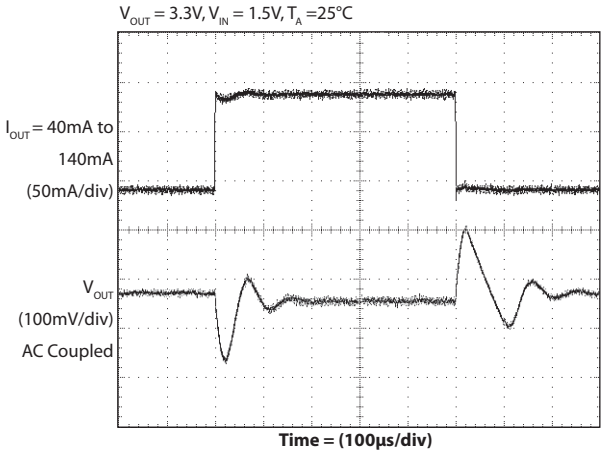


Typical Characteristics (continued)

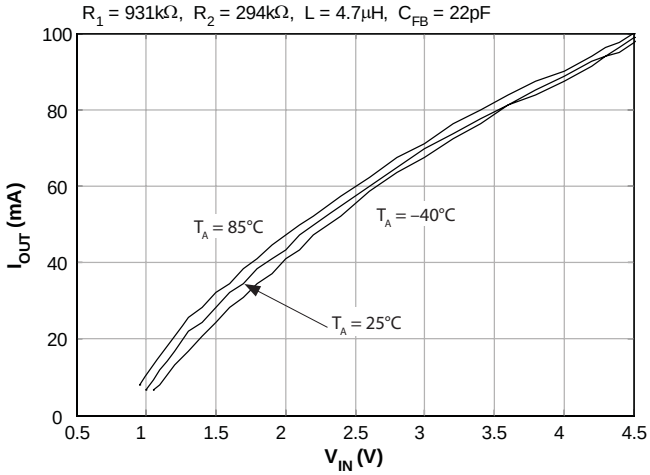
PWM Operation



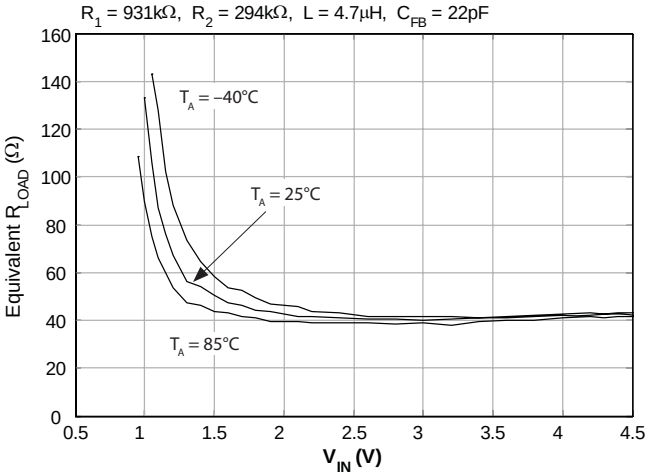
Load Transient



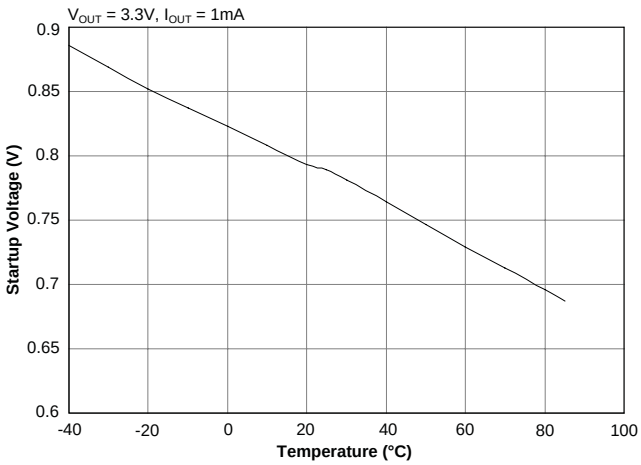
Startup Max Load Current vs. V_{IN} (Any V_{OUT})



Startup Min Load Res. vs. V_{IN} (Any V_{OUT})



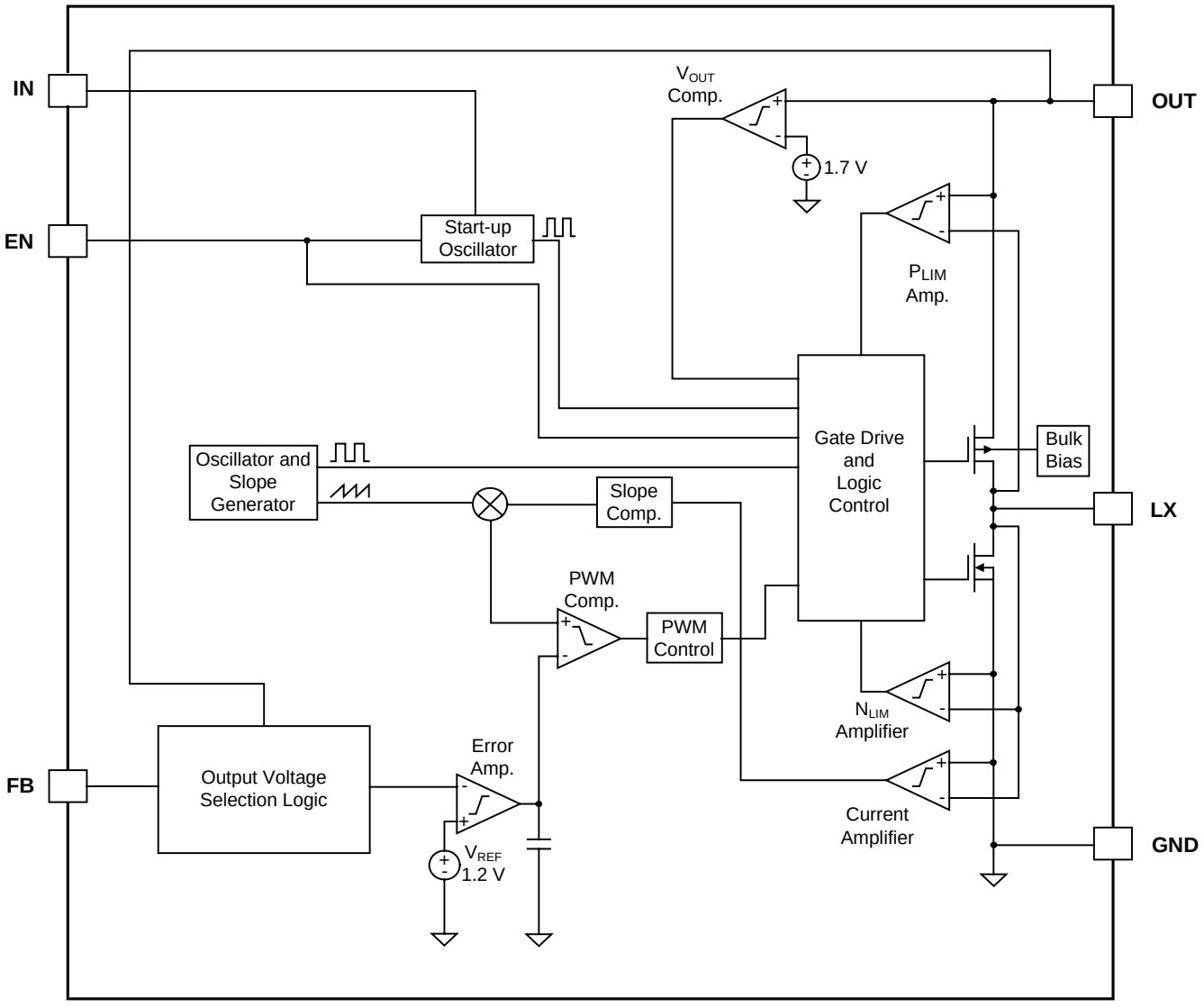
Min. Start-up Voltage vs. Temperature (Any V_{OUT})



Pin Descriptions

MLPD Pin #	Pin Name	Pin Function
1	LX	Switching node — connect an inductor from the input supply to this pin.
2	GND	Signal and power ground.
3	IN	Battery or supply input — requires an external 10µF bypass capacitor (capacitance evaluated while under V_{IN} bias) for normal operation.
4	EN	Enable digital control input — active high.
5	FB	Feedback input — connect to GND for preset 3.3V output. A voltage divider is connected from OUT to GND to adjust output from 1.8V to 5.0V.
6	OUT	Output voltage pin — requires an external 10µF bypass capacitor (capacitance evaluated while under V_{OUT} bias) for normal operation.
T	Thermal Pad	Thermal Pad is for heat sinking purposes — connect to ground plane using multiple vias — not connected internally.

Block Diagram



Applications Information

Detailed Description

The SC121 is a synchronous step-up fixed frequency Pulse Width Modulated (PWM) DC-DC converter utilizing a 1.2MHz fixed frequency current mode architecture. It is designed to provide output voltages in the range 1.8V to 5.0V from an input voltage as low as 0.7V, with a (output unloaded) start up input voltage of 0.85V. Quiescent current consumption is typically 3.5mA, entirely into the OUT pin during boost regulation. (See footnote 1 of the Electrical Characteristics table.)

The regulator control circuitry is shown in the Block Diagram. It is comprised of a programmable feedback controller, an internal 1.2MHz oscillator, an n-channel Field Effect Transistor (FET) between the LX and GND pins, and a p-channel FET between the LX and OUT pins. The current flowing through both FETs is monitored and limited as required for startup and PWM operation. An external inductor must be connected between the IN pin and the LX pin.

Output Voltage Selection

The SC121 output voltage can be programmed to an internally preset value or it can be programmed with external resistors. The output is internally programmed to 3.3V when the FB pin is connected to GND. Any output voltage in the range 1.8V to 5.0V can be programmed with a resistor voltage divider between OUT and the FB pin as shown in Figure 1.

The values of the resistors in the voltage divider network are chosen to satisfy the equation

$$V_{OUT} = 1.191 \times \left(1 + \frac{R_1}{R_2}\right) \quad (V)$$

A large value of R_2, ideally 590kΩ or larger, is preferred for stability for V_{IN} within approximately 400mV of V_{OUT}. For lower V_{IN}, lower resistor values can be used. The values of R_1 and R_2 can be as large as desired to achieve low quiescent current. C_{FB} = 22pF is recommended to improve transient response.

The Enable Pin

The EN pin is a high impedance logical input that can be used to enable or disable the SC121 under processor control. V_{EN} < 0.2V will disable regulation, set the LX pin in a high-impedance state (turn off both FET switches), and turn on an active discharge device to discharge the output capacitor via the OUT pin. Synchronous rectifier (p-channel FET) bulk switching prevents pass-through conduction from LX to OUT while disabled. V_{EN} > 0.85V will enable the output. The startup sequence from the EN pin is identical to the startup sequence from the application of input power.

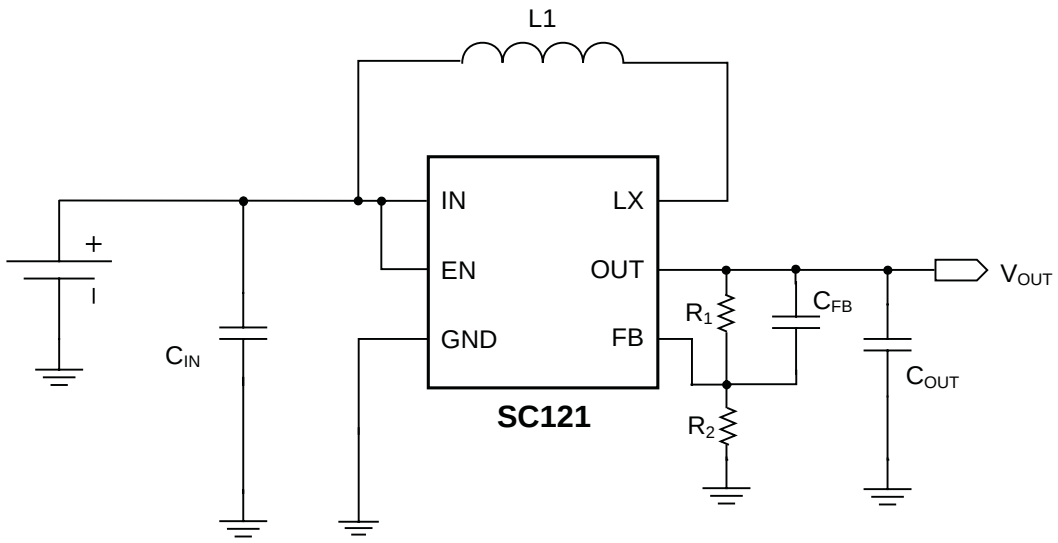


Figure 1 — Output Voltage Feedback Circuit

SEMTECH

Applications Information (continued)

PWM Operation

The PWM cycle runs at a fixed frequency (f_{osc} = 1.2MHz), with a variable duty cycle (D). PWM operation continually draws current from the input supply, except for low output loads in which current flows periodically from, and back into, the input. During the on-state of the PWM cycle, the n-channel FET is turned on, grounding the inductor at the LX pin. This causes the current flowing from the input supply through the inductor to ground to ramp up. During the off-state, the n-channel FET is turned off and the p-channel FET (synchronous rectifier) is turned on. This causes the inductor current to flow from the input supply through the inductor into the output capacitor and load, boosting the output voltage above the input voltage. The cycle then repeats to re-energize the inductor.

Ideally, the steady state (constant load) duty cycle is determined by $D = 1 - (V_{IN}/V_{OUT})$, but must be greater in practice to overcome dissipative losses. The SC121 PWM controller constrains the value of D such that $0.20 < D < 0.90$ (approximately).

The average inductor current during the off-state multiplied by (1-D) is equal to the average load current. The inductor current is alternately ramping up (on-state) and down (off-state) at a rate and amplitude determined by the inductance value, the input voltage, and the on-time ($T_{ON} = D \times T, T = 1/f_{OSC}$). Therefore, the instantaneous inductor current will be alternately larger and smaller than the average.

If the average output current is sufficiently small, the minimum inductor current can ramp down to zero during the off-state. Discontinuous mode operation (where both FETs turn off as the inductor current reaches zero) is not supported in the SC121, since this would result in a finite positive minimum current from input to output, which would cause an uncontrolled rise in output voltage in this case. Instead, the inductor current will reverse for the remainder of the off-state, flowing from the output capacitor into the OUT pin, through the p-channel FET to the LX pin, and through the inductor to the input capacitor. Negative inductor current ripple allows regulation even with zero output load. The energy returned to the input capacitor is not wasted, but dissipative conduction losses will inevitably occur.

The minimum on-time limitation imposes a minimum boost ratio, so if V_{IN} is too close to V_{OUT} ($V_{IN} > V_{OUT} - 400mV$, approximately), V_{OUT} will rise above the programmed value for a sufficiently small output load. A higher output load requires a higher duty cycle to overcome dissipative losses, such that regulation at programmed V_{OUT} will eventually be restored. But this regulation-restoration load rises rapidly with V_{IN}, so this phenomenon can be beneficially exploited in only rare circumstances. If operation with high V_{IN} and low load is required, please consider using the SC120, a pin compatible dual mode (PWM/PSAVE) boost converter. The SC120 will support zero load in PSAVE mode for V_{IN} up to V_{OUT} + 150mV.

Regulator Startup, Short Circuit Protection, and Current Limits

The SC121 permits power up at input voltages from 0.85V to 4.5V. Soft-start startup current limiting of the internal switching n-channel and p-channel FET power devices protects them from damage in the event of a short between OUT and GND. As the output voltage rises, progressively less-restrictive current limits are applied. This protection unavoidably prevents startup into an excessive load.

Upon enable, the p-channel FET between the LX and OUT pins turns on with its current limited to approximately 150mA, the short-circuit output current. When V_{OUT} approaches V_{IN} (but is still below 1.7V), the n-channel current limit is set to 350mA (the p-channel limit is disabled), the internal oscillator turns on (approximately 200kHz), and a fixed 75% duty cycle PWM operation begins. (See the section PWM Operation.) When the output voltage exceeds 1.7V, fixed frequency PWM operation begins, with the duty cycle determined by an n-channel FET peak current limit of 350mA. When this n-channel FET startup current limit is exceeded, the on-state ends immediately and the off-state begins. This determines the duty cycle on a cycle-by-cycle basis. When V_{OUT} is within 2% of the programmed regulation voltage, the n-channel FET current limit is raised to 1.2A, and normal voltage regulation PWM control begins.

Once normal voltage regulation PWM control is initiated, the output becomes independent of V_{IN} and output regulation can be maintained for V_{IN} as low as 0.7V, subject to the maximum duty cycle and peak current limits. The

Applications Information (continued)

duty cycle must remain between 20% and 90% for the device to operate within specification.

Note that startup with a regulated active load is not the same as startup with a resistive load. The resistive load output current increases proportionately as the output voltage rises until it reaches programmed V_{OUT}/R_{LOAD}, while a regulated active load presents a constant load as the output voltage rises from 0V to programmed V_{OUT}. Note also that if the load applied to the output exceeds an applicable V_{OUT}–dependent startup current limit or duty cycle limit, the criterion to advance to the next startup stage may not be achieved. In this situation startup may pause at a reduced output voltage until the load is reduced further.

Output Overload and Recovery

The PWM steady state duty cycle is determined by $D = 1 - (V_{IN}/V_{OUT})$, but must be somewhat greater in practice to overcome dissipative losses. As the output load increases, the dissipative losses also increase. The PWM controller must increase the duty cycle to compensate. Eventually, one of two overload conditions will occur, determined by V_{IN}, V_{OUT}, and the overall dissipative losses due to the output load current. Either the maximum duty cycle of 90% will be reached or the n-channel FET 1.2A (nominal) peak current limit will be reached, which effectively limits the duty cycle to a lower value. Above that load, the output voltage will decrease rapidly and in reverse order the startup current limits will be invoked as the output voltage falls through its various voltage thresholds. How far the output voltage drops depends on the load voltage vs. current characteristic.

A reduction in input voltage, such as a discharging battery, will lower the load current at which overload occurs. Lower input voltage increases the duty cycle required to produce a given output voltage. And lower input voltage also increases the input current to maintain the input power, which increases dissipative losses and further increases the required duty cycle. Therefore an increase in load current or a decrease in input voltage can result in output overload. Please refer to the Max. I_{OUT} vs. V_{IN} Typical Characteristics plots for the condition that best matches the application.

Once an overload has occurred, the load must be decreased to permit recovery. The conditions required for overload recovery are identical to those required for successful initial startup.

Component Selection

The SC121 provides optimum performance when a 4.7µH inductor is used with a 10µF output capacitor. Different component values can be used to modify input current or output voltage ripple, improve transient response, or to reduce component size or cost.

Inductor Selection

The inductance value primarily affects the amplitude of inductor peak-to-peak current ripple (ΔI_L). Reducing inductance increases ΔI_L and raises the inductor peak current, $I_{L\text{-}max} = I_{L\text{-}avg} + \Delta I_L/2$, where $I_{L\text{-}avg}$ is the inductor current averaged over a full on/off cycle. $I_{L\text{-}max}$ is subject to the n-channel FET current limit $I_{LIM(N)}$, therefore reducing the inductance may lower the output overload current threshold. Increasing ΔI_L also lowers the inductor minimum current, $I_{L\text{-}min} = I_{L\text{-}avg} - \Delta I_L/2$, thus raising the load current threshold below which inductor negative–peak current becomes zero.

Equating input power to output power and noting that input current is equal to inductor current, average the inductor current over a full PWM switching cycle to obtain

$$I_{L-avg} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}}$$

where η is efficiency.

Neglecting the n-channel FET $R_{DS\text{-}ON}$ and the inductor DCR, for duty cycle D, and with $T = 1/f_{osc}$,

$$\Delta I_{L-on} = \frac{1}{L}\int_0^{DT} V_{IN}\, dt = \frac{V_{IN} \times D \times T}{L}$$

This is the change in I_L during the on-state. During the off-state, again neglecting the p-channel FET $R_{DS\text{-}ON}$ and the inductor DCR,

$$\Delta I_{L-off} = \frac{1}{L}\int_{DT}^{T} (V_{IN} - V_{OUT})\, dt = \frac{(V_{IN} - V_{OUT}) \times T}{L}(1-D)$$

Applications Information (continued)

Note that this is a negative quantity, since $V_{OUT} > V_{IN}$ and $0 < D < 1$. For a constant load in steady-state, the inductor current must satisfy $\Delta I_{L\text{-}on} + \Delta I_{L\text{-}off} = 0$. Substituting the two expressions and solving for D, obtain $D = 1 - V_{IN}/V_{OUT}$. Using this expression, and the positive valued expression $\Delta I_L = \Delta I_{L\text{-}on}$ for current ripple amplitude, obtain expanded expression for $I_{L\text{-}max}$ and $I_{L\text{-}min}$.

$$I_{L-max,min} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \pm \frac{T}{2 \times L} \times \frac{V_{IN}}{V_{OUT}} \times (V_{OUT} - V_{IN})$$

From this result, obtain an alternative expression for ΔI_L.

$$\Delta I_L = I_{L-max} - I_{L-min} = \frac{T}{L} \times \frac{V_{IN}}{V_{OUT}} \times (V_{OUT} - V_{IN})$$

The inductor selection should consider the n-channel FET current limit for the expected range of input voltage and output load current. The largest $I_{L\text{-}avg}$ will occur at the expected smallest V_{IN} and largest I_{OUT}. Determine the largest expected ΔI_L. Then for the largest expected $I_{L\text{-}avg}$, ensure that the n-channel FET current limit is not exceed. That is, for the minimum n-channel FET current limit, worst case inductor tolerance, highest expected output current, and lowest expected V_{IN}, ensure that

$$I_{L\text{-}max} = I_{L\text{-}avg} + \Delta I_L/2 < I_{LIM(N)}.$$

Many of these equations include the parameter η, efficiency. Efficiency varies with V_{IN}, I_{OUT}, and temperature. Estimate η using the plots provided in this datasheet, or from experimental data, at the operating condition of interest.

Any chosen inductor should have low DCR compared to the $R_{DS\text{-}ON}$ of the FET switches to maintain efficiency, though for DCR << $R_{DS\text{-}ON}$, further reduction in DCR will provide diminishing benefit. The inductor I_{SAT} value should exceed the expected $I_{L\text{-}max}$. The inductor self-resonant frequency should exceed $5 \times f_{osc}$. Any inductor with these properties should provide satisfactory performance. L = 4.7µH should perform well for most applications.

The following table lists the manufacturers of recommended inductor options. The specification values shown are simplified approximations or averages of many device parameters under various test conditions. See manufacturers' documentation for full performance data.

Manufacturer/ Part #	Value (µH)	DCR (Ω)	Rated Current (mA)	Tolerance (%)	Dimensions LxWxH (mm)
Murata LQM31PN4R7M00	4.7	0.3	700	20	3.2 x 1.6 x 0.95
Coilcraft XFL2006-472	4.7	0.7	500	20	2 x 2 x 0.6

Capacitor Selection

Input and output capacitors must be chosen carefully to ensure that they are of the correct value and rating. The output capacitor requires a minimum capacitance value of 10µF at the programmed output voltage to ensure stability over the full operating range. This must be considered when choosing small package size capacitors as the DC bias must be included in their derating to ensure this required value. For example, a 10µF 0805 capacitor may provide sufficient capacitance at low output voltages but may be too low at higher output voltages. Therefore, a higher capacitance value may be required to provide the minimum of 10µF at these higher output voltages.

Low ESR capacitors such as X5R or X7R type ceramic capacitors are recommended for input bypassing and output filtering. Low-ESR tantalum capacitors are not recommended due to possible reduction in capacitance seen at the switching frequency of the SC121. Ceramic capacitors of type Y5V are not recommended as their temperature coefficients make them unsuitable for this application. The following table lists recommended capacitors. For smaller values and smaller packages, it may be necessary to use multiples devices in parallel.

Manufacturer/ Part Number	Value (µF)	Rated Voltage (VDC)	Type	Case Size	Case Height (mm)
Murata GRM21BR60J226ME39B	22	6.3	X5R	0805	1.25
Murata GRM31CR71A226KE15L	22	10	X7R	1206	1.6
Murata GRM185R60G475ME15	4.7	4	X5R	0603	0.5
TDK C2012X5R1A226M	22	10	X5R	0805	0.85
Taiyo Yuden JMK212BJ226MG-T	22	20	X5R	0805	1.25

Applications Information (continued)

PCB Layout Considerations

Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce, and resistive voltage losses. Poor regulation and instability can result.

The following simple design rules can be implemented to ensure good layout:

- Place the inductor and filter capacitors as close to the device as possible and use short wide traces between the power components.
- Route the output voltage feedback path away from the inductor and LX node to minimize noise and magnetic interference.
- Maximize ground metal on the component side to improve the return connection and thermal dissipation. Separation between the LX node and GND should be maintained to avoid coupling capacitance between the LX node and the ground plane.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

A suggested layout is shown in Figure 4.

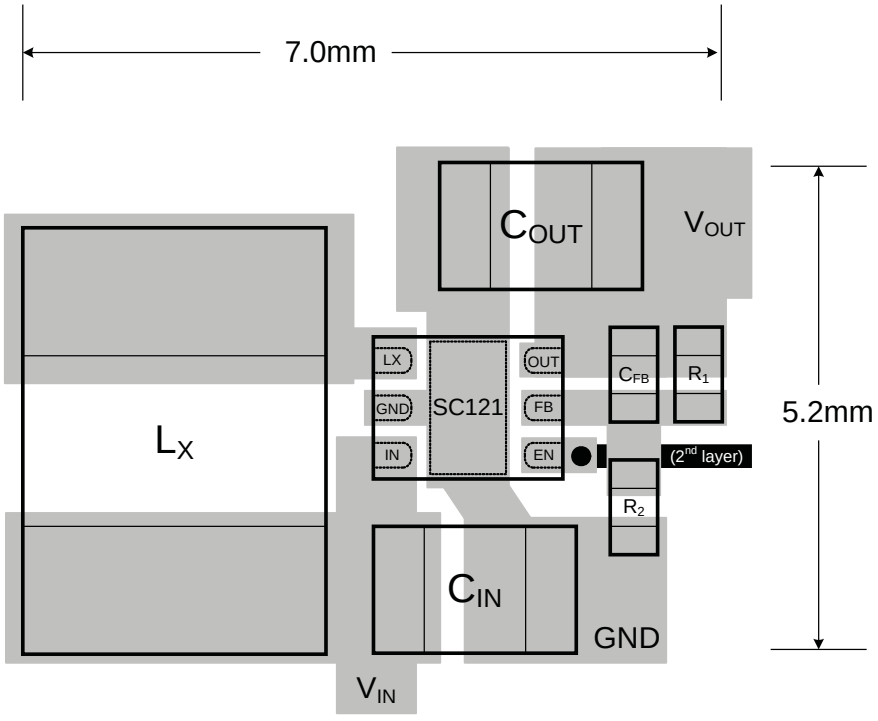
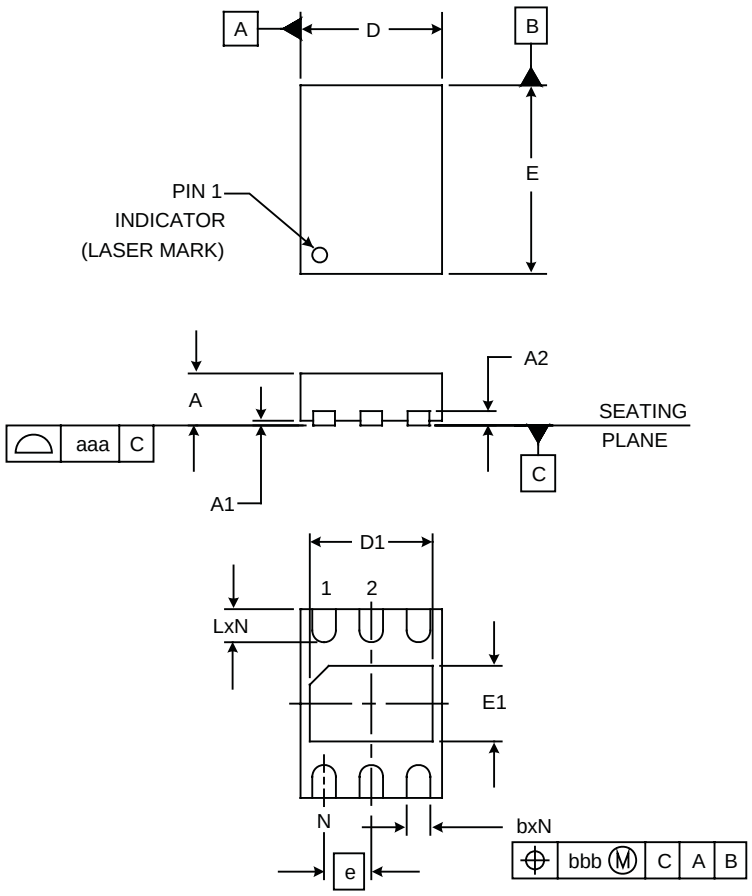


Figure 4 — Layout Drawing

Outline Drawing — MLPD-UT-6 1.5x2

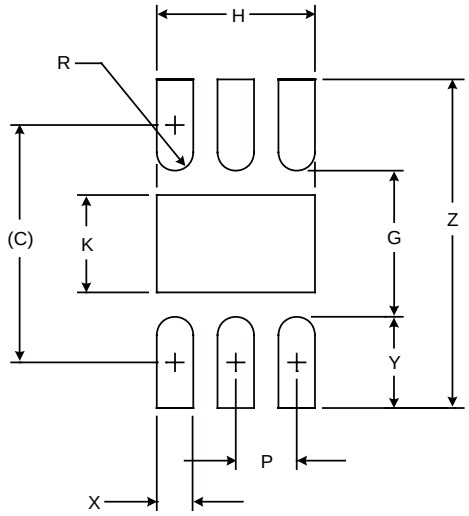


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(.152)	
b	.007	.010	.012	0.18	0.25	0.30
D	.055	.059	.063	1.40	1.50	1.60
D1	.035	-	.055	0.90	-	1.40
E	.075	.079	.083	1.90	2.00	2.10
E1	.026	.031	.035	0.65	0.80	0.90
e		.020 BSC			0.50 BSC	
L	.012	.014	.016	0.30	0.35	0.40
N		6			6	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Land Pattern — MLPD-UT-6 1.5x2



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.077)	(1.95)
G	.047	1.20
H	.051	1.30
K	.031	0.80
P	.020	0.50
R	.006	0.15
X	.012	0.30
Y	.030	0.75
Z	.106	2.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD
   SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
   FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR
   FUNCTIONAL PERFORMANCE OF THE DEVICE.

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