Features

- Transient protection for high-speed data lines
  - IEC 61000-4-2 (ESD) ±25kV (Air)
  - ±17kV (Contact)
  - IEC 61000-4-4 (EFT) 40A (5/50 ns)
  - Cable Discharge Event (CDE)
- Small package (2.9mm × 2.4mm × 1.0mm)
- Protects two data lines
- Low capacitance: 0.25pF Typical (I/O-I/O)
- Low leakage current: 0.1μA @ V_{RWM} (Typical)
- Low clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge

Description

TT0512TKX is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 0.25pF only, TT0512TKX is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), Level 4 (±15kV air, ±8kV contact discharge), IEC 61000-4-4 (electrical fast transient - EFT) (40A, 5/50 ns), very fast charged device model (CDM) ESD and cable discharge event (CDE), etc.

TT0512TKX uses small SOT-23 package . Each TT0512TKX device can protect two high-speed data lines. The combined features of low capacitance, small size and high ESD robustness make TT0512TKX ideal for high-speed data ports and high-frequency lines (e.g., USB2.0 & DVI) applications. The low clamping voltage of the TT0512TKX guarantees a minimum stress on the protected IC.

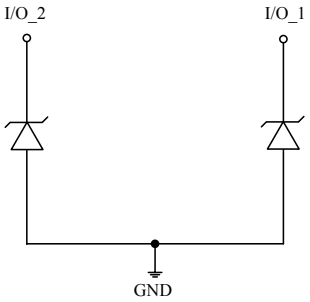
Applications

- Serial ATA
- PCI Express
- Desktops, Servers and Notebooks
- MDDI Ports
- USB2.0 Power and Data Line Protection
- Display Ports
- Digital Visual Interfaces (DVI)

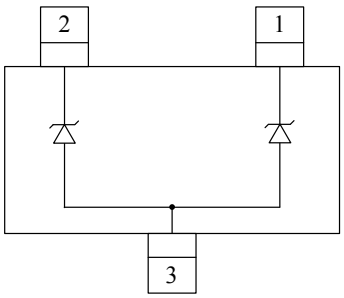
Mechanical Characteristics

- SOT-23
- Flammability Rating: UL 94V-0
- Marking: Part number
- Packaging: Tape and Reel

Circuit Diagram



Pin Configuration



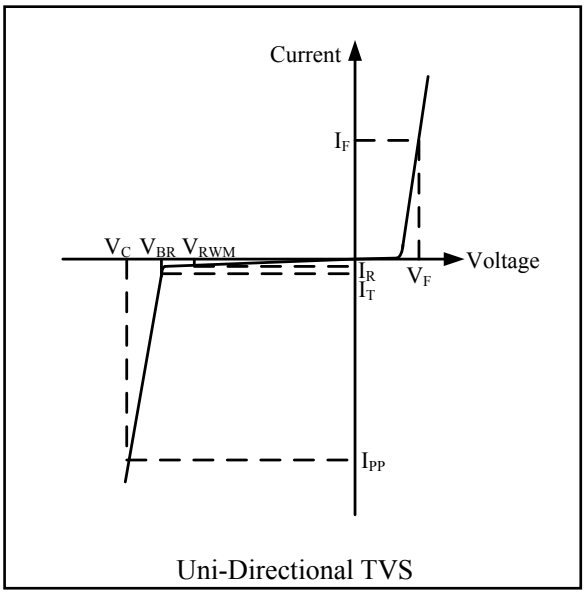
SOT-23
(Top View)

Absolute Maximum Rating

Symbol	Parameter	Value	Units
I_{PP}	Peak Pulse Current(tp=8/20us)(IO-GND)	3	A
V_{ESD}	ESD per IEC 61000-4-2(Air) ESD per IEC 61000-4-2 (Contact)	±25 ±17	kV
T_{OPT}	Operating Temperature	-55/+125	°C
T_{STG}	Storage Temperature	-55/+150	°C

Electrical Characteristics (T = 25°C)

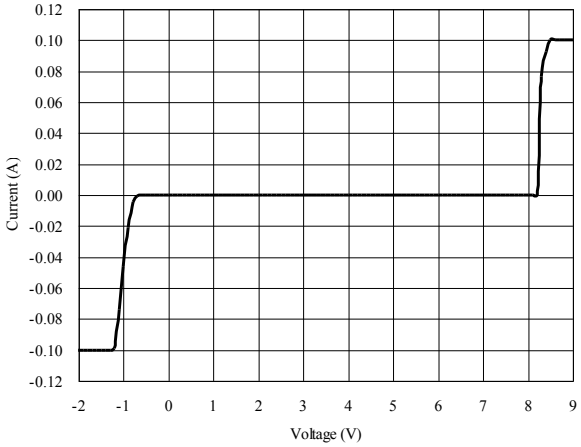
Symbol	Parameter
V_{RWM}	Nominal Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Reverse Breakdown Voltage @ I_T
I_T	Test Current for Reverse Breakdown
V_C	Clamping Voltage @ I_{PP}
I_{PP}	Maximum Peak Pulse Current
C_{ESD}	Parasitic Capacitance
V_R	Reverse Voltage
f	Small Signal Frequency
I_F	Forward Current
V_F	Forward Voltage @ I_F



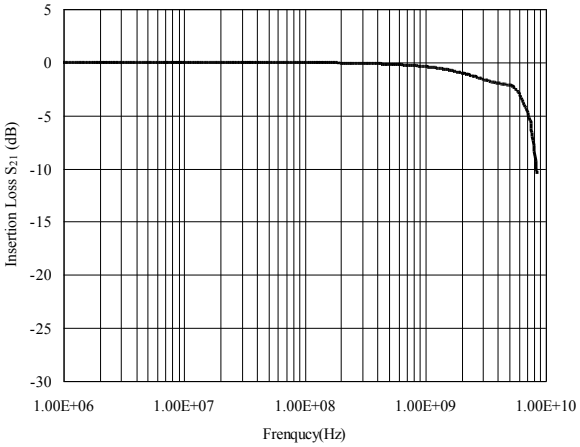
Uni-Directional TVS

Symbol	Test Condition	Minimum	Typical	Maximum	Units
V_{RWM}				5.0	V
I_R	V_{RWM} = 5V, T = 25°C Between I/O and GND		0.1	1.0	μA
V_{BR}	I_T = 1mA Between I/O and GND	6.0	8.0	10.0	V
V_C	I_{PP} = 1A, t_p = 8/20μs Between I/O and GND			12	V
C_{ESD}	V_R = 0V, f = 1MHz Between I/O and GND		0.8	1.2	pF
C_{ESD}	V_R = 0V, f = 1MHz Between I/O and I/O		0.25	0.5	pF

Voltage Sweeping of I/O to GND

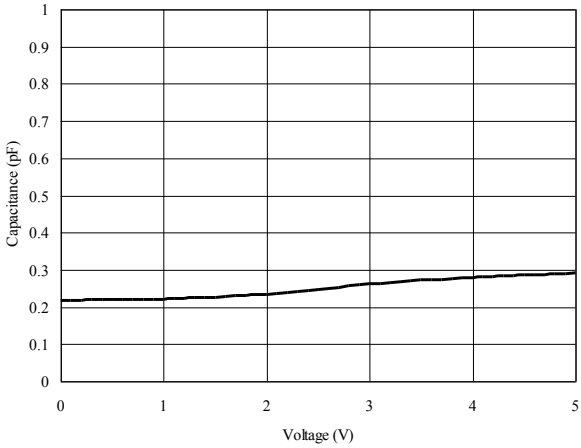


Insertion Loss S21 of I/O to GND

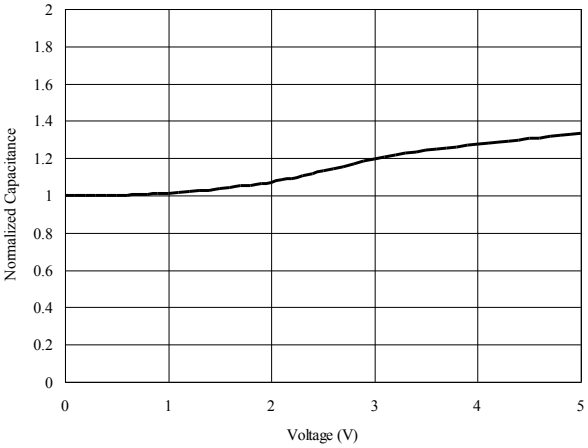


Capacitance *vs.* Voltage of I/O to I/O (f = 1MHz)

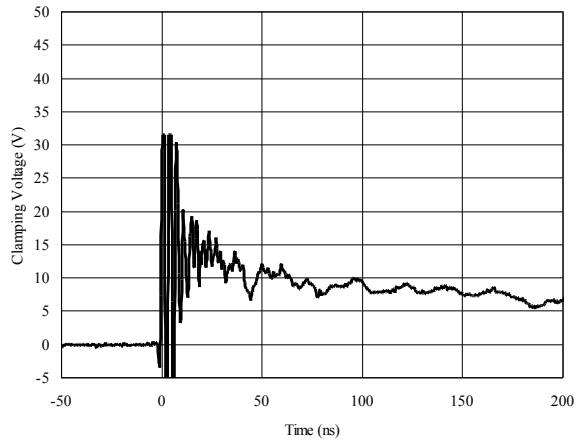
Capacitance *vs.* Reverse Voltage



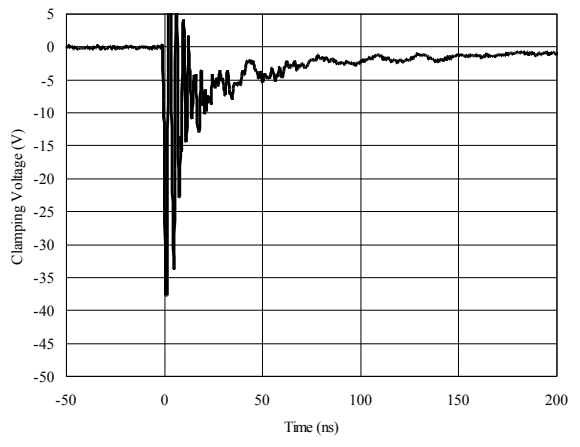
Normalized Capacitance *vs.* Reverse Voltage



ESD Clamping (+8kV Contact per IEC 61000-4-2)



ESD Clamping (-8kV Contact per IEC 61000-4-2)



Application Information

Pin Connection in PCB

TT0512TKX is capable to provide ESD protection for two data lines simultaneously. The pin connection is shown in Figure 1.

Two parallel data lines, from inner IC to I/O port connector, could connect to TT0512TKX two I/O pins directly. Pin 3 of TT0512TKX is the negative reference pin, which should connect to the GND of PCB. The connection wires should be as short as possible in order to minimize the parasitic inductance.

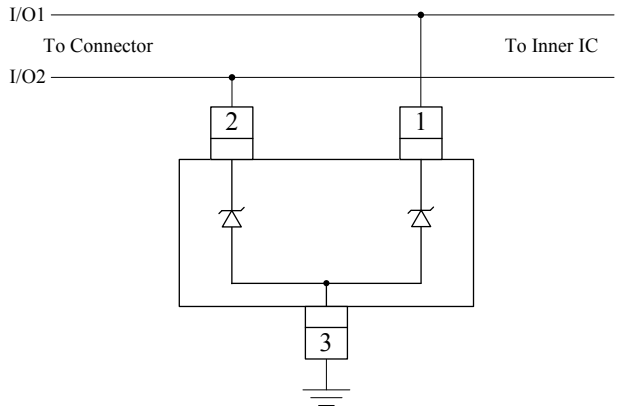


Figure 1 TT0512TKX pin connection in PCB

PCB Layout Guidelines

For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

- TT0512TKX GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND.
- The vias connecting TT0512TKX VCC & GND pins to the PCB VCC & GND should be wide.
- Place TT0512TKX as close to the connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.
- Avoid running critical signals near board edges.

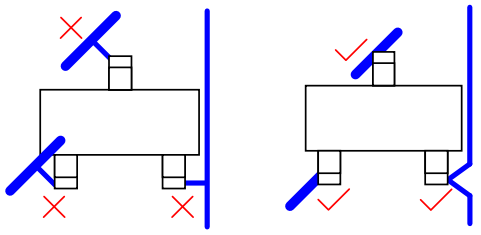


Figure 2 TT0512TKX Layout Guidelines

Universal Serial Bus ESD Protection

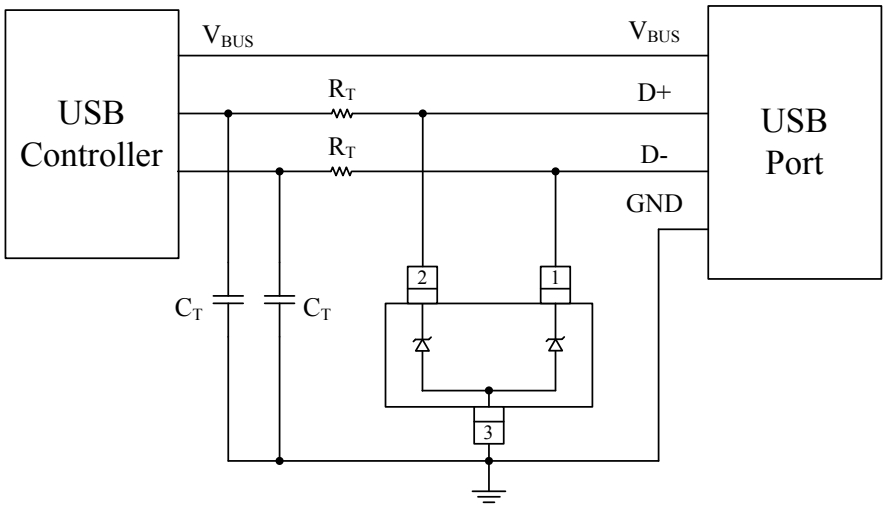
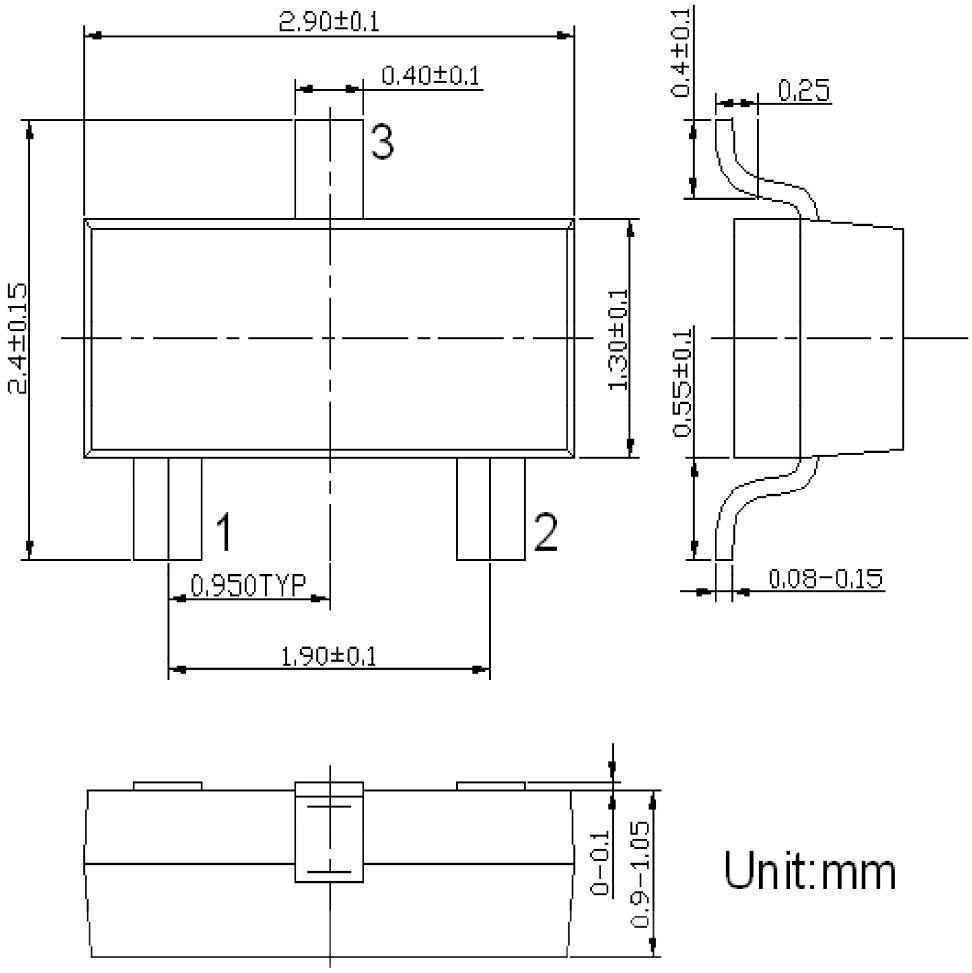


Figure 3 Schematic and Diagram for USB 2.0 Protection using TT0512TKX

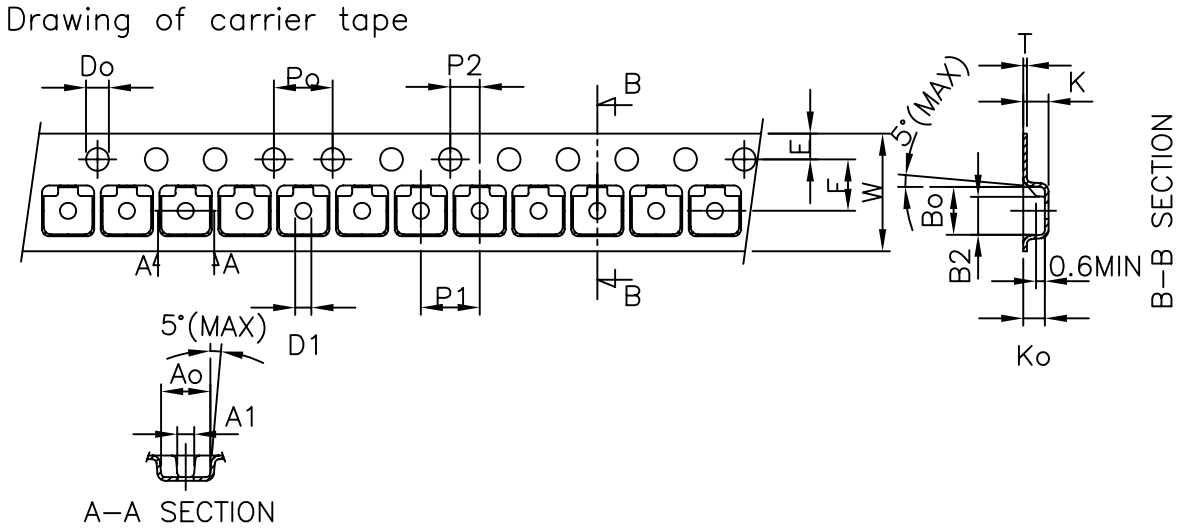
Package Outline

- SOT-23
- MSL-3



Carrier Dimensions

Drawing of carrier tape

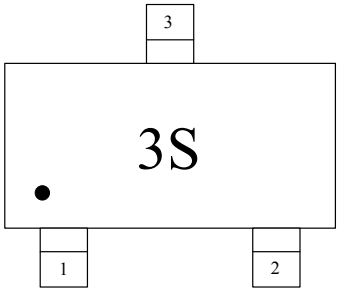


symbol	Ao	Bo	Ko	Po	P1	P2	T	A1
spec	3.1±0.2	$2.7^{+0.2}_{-0.1}$	1.20(MIN)	4.0±0.1	4.0±0.1	2.0±0.05	0.20±0.02	1.0±0.1
symbol	E	F	B2	Do	D1	W	10Po	K
spec	1.75±0.1	3.5±0.05	$2.1^{+0.25}_{-0.1}$	$1.50^{+0.1}_{-0.0}$	1.0MIN	$8.0^{+0.3}_{-0.1}$	40.0±0.2	1.5MAX

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is ±0.2mm
2. Carrier camber shall be not more than 1mm per 100mm through a length of 250mm.
3. Ao & Bo measured on a plane except corner radii.
4. Ko measured from a place on the inside bottom of the pocket to top surface of carrier.
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
6. Surface resistivity of carrier tape should be within $10^4 \sim 10^9$ ohms/sq at 65% ± 15% humidity and 24°C±5°C.

Marking Codes



Note:

(1) "3S" is part number,fixed.

Ordering Information

Part Number	Working Voltage	Quantity Per Reel	Reel Size
TT0512TKX	5.0V	3,000	7 Inch