

1. Features

- Proprietary New Planar Technology
- $R_{DS(ON)}=0.39\Omega(\text{typ.})@V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

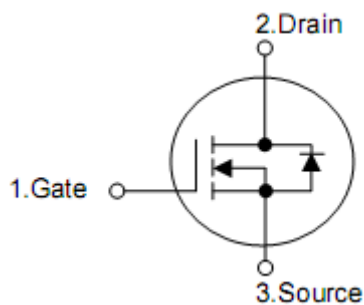
2. Applications

- Ballast and Lighting
- DC-AC Inverter
- Other Applications

3. Pin configuration



TO-220F



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KNF6145A	TO-220F	KIA

5. Absolute maximum ratings

(T_C= 25 °C, unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-to-Source Voltage ¹⁾		V _{DSS}	450	V
Gate-to-Source Voltage		V _{GSS}	±30	V
Continuous Drain Current	T _C =25°C	I _D	11	A
	T _C =100°C	I _D	Figure 3	A
Pulsed Drain Current at V _{GS} =10V ²⁾		I _{DM}	Figure 6	A
Single Pulse Avalanche Energy ²⁾		EAS	500	mJ
Peak Diode Recovery dv/dt ³⁾		dv/dt	5.0	V/ns
Power Dissipation		P _D	45	W
Derating Factor above 25°C		P _D	0.37	W/°C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds		T _L T _{PAK}	300 260	°C
Operating and Storage Temperature Range		T _J &T _{STG}	-55 to 150	°C

Caution: Stresses greater than those in the “Absolute Maximum Ratings” may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	R _{θJC}	2.7	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	100	°C/W

7. Electrical characteristics

(T_C=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	450	-	-	V
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} =450V, V _{GS} =0V	-	-	1	uA
		V _{DS} =360V, T _J =125°C	-	-	100	uA
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	-	-	±100	nA
Drain-to-Source ON Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =5A	-	0.39	0.5	Ω
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250uA	2.0	-	4.0	V
Forward Transconductance ⁴⁾	g _{fs}	V _{DS} =20V, I _D =10A	-	12	-	S
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =25V, f=1.0MHZ	-	1200	-	pF
Reverse Transfer Capacitance	C _{oss}		-	140	-	
Output Capacitance	C _{rss}		-	18	-	
Total Gate Charge	Q _g	V _{DD} =200V, I _D =10A, V _{GS} =0 to 10V	-	25	-	nC
Gate-to-Source Charge	Q _{gs}		-	6	-	
Gate-to-Drain (Miller) Charge	Q _{gd}		-	10	-	
Turn-on Delay Time	t _{d(ON)}	V _{DD} =200V, I _D =10A, R _G =12Ω, V _{GS} =10V	-	12	-	nS
Rise Time	t _{rise}		-	24	-	
Turn-Off Delay Time	t _{d(OFF)}		-	40	-	
Fall Time	t _{fall}		-	26	-	
Continuous Source Current	I _{SD}	Integral PN-diode in MOSFET	-	-	10	A
Pulsed Source Current	I _{SM}		-	-	40	A
Forward Voltage	V _{SD}	I _S =10A, V _{GS} =0V	-	-	1.5	V
Reverse recovery time	t _{rr}	I _F =10A, V _{GS} =0V diF/dt=100A/μs,	-	303	-	ns
Reverse recovery charge	Q _{rr}		-	1.8	-	uC

Note:

1) T_J=+25°C to +150

2) Repetitive rating; pulse width limited by maximum junction temperature.

3) I_{SD}=10A, di/dt<100A/us, V_{DD}<BV_{DSS}, T_J=+150°C.

4) Pulse width≤380us; duty cycle≤2%.

8. Typical Characteristics

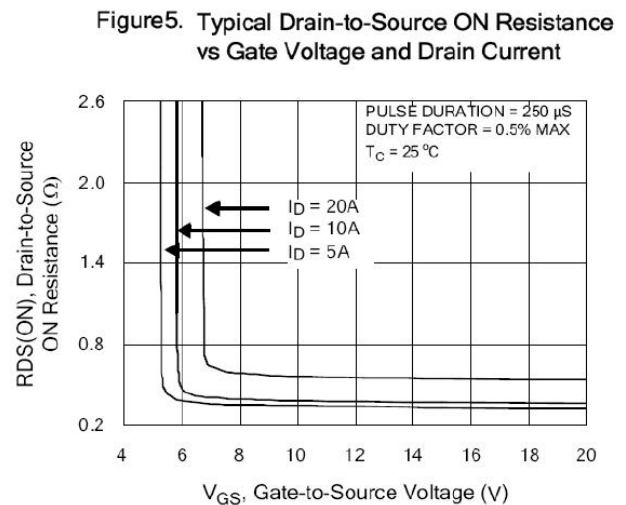
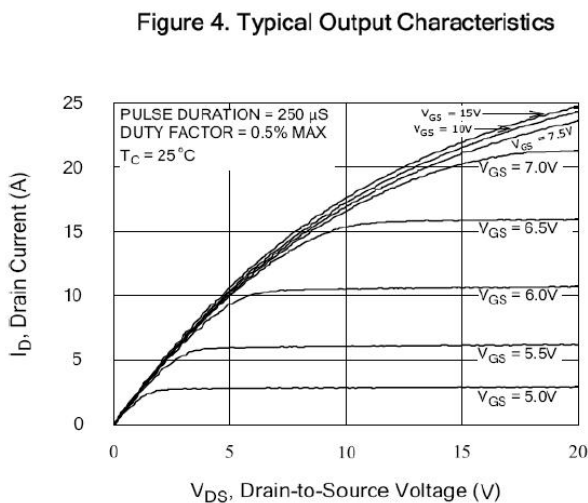
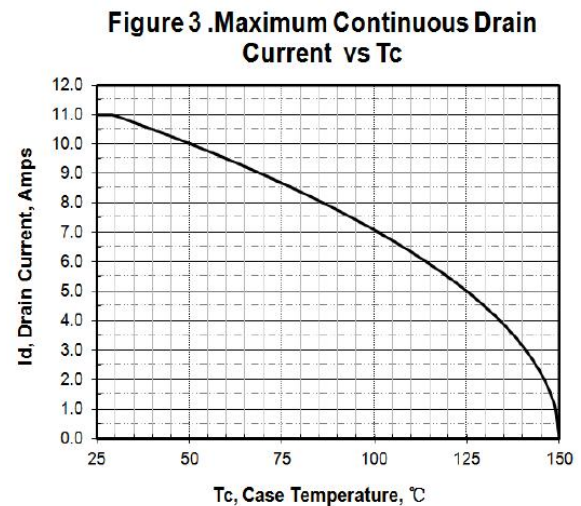
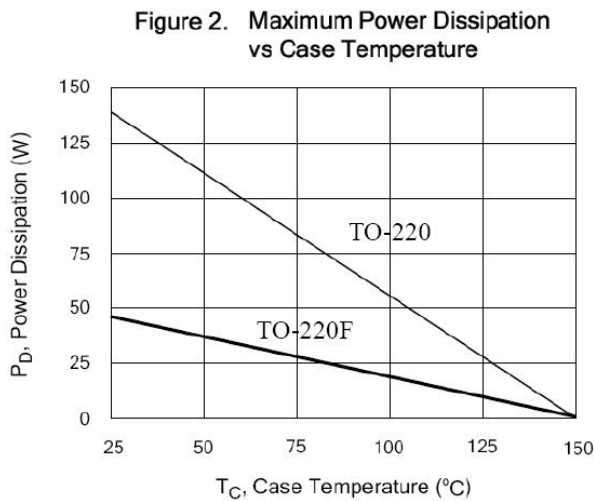
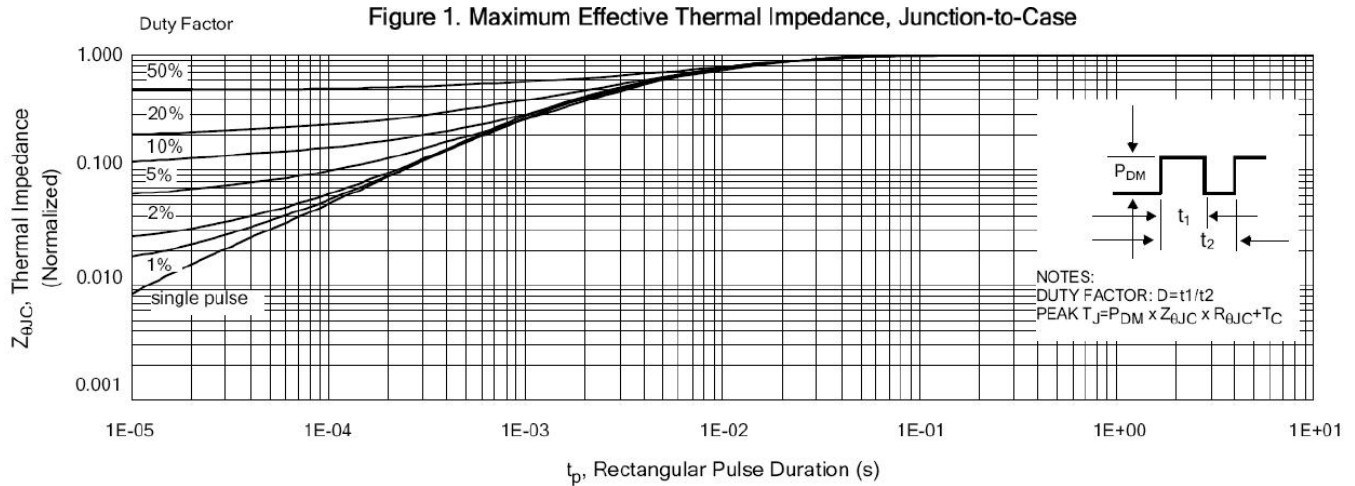


Figure 6. Peak Current Capability

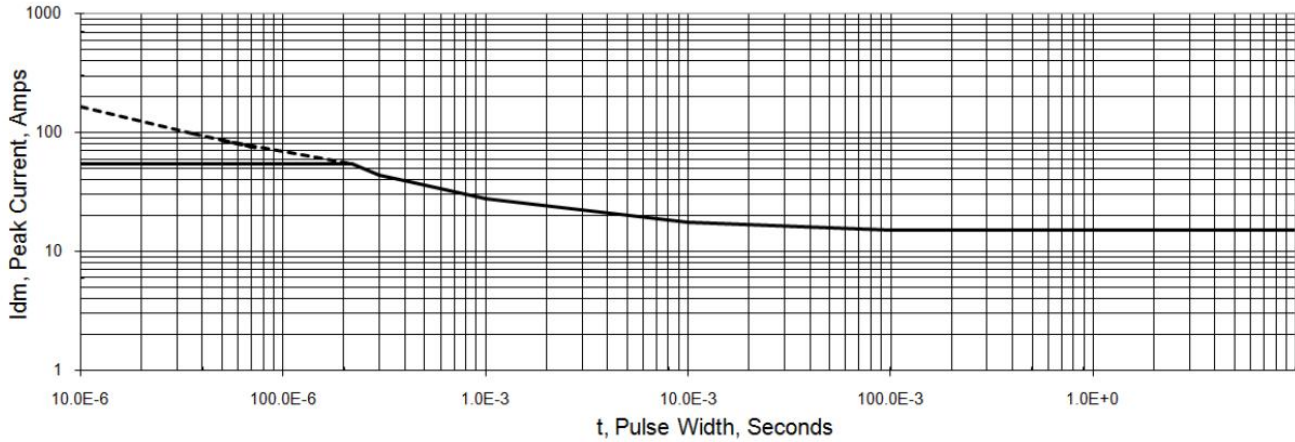


Figure 7. Typical Transfer Characteristics

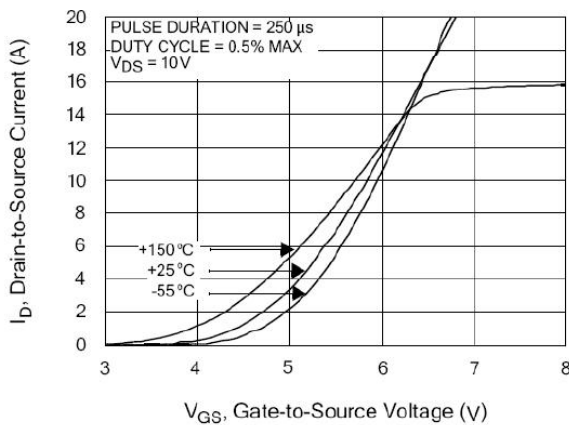


Figure 8. Unclamped Inductive Switching Capability

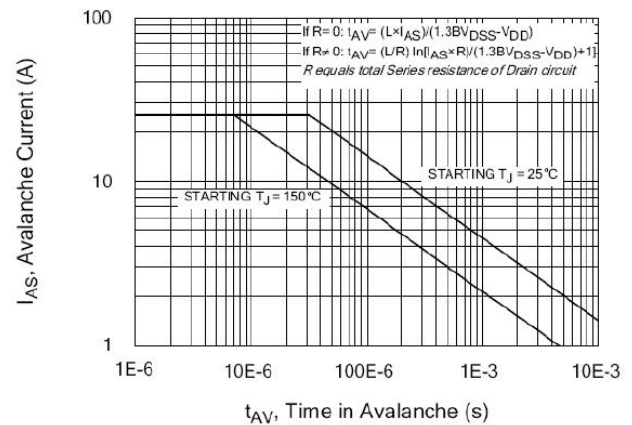


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

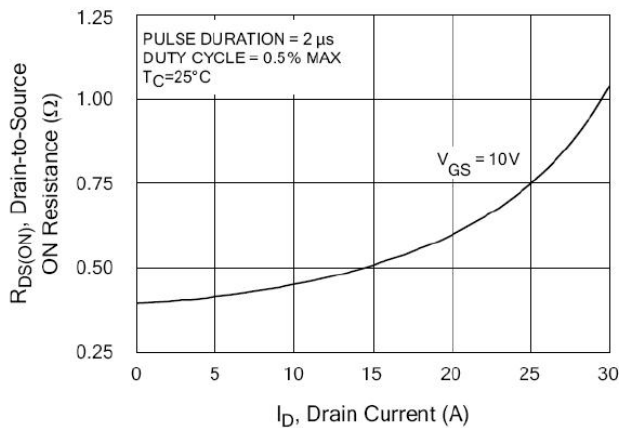


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

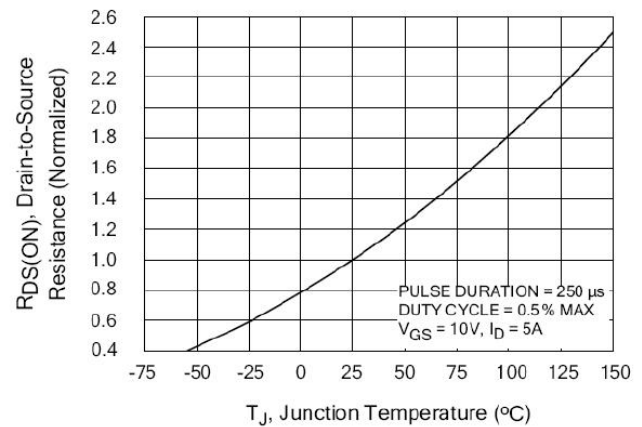


Figure 11. Typical Breakdown Voltage vs Junction Temperature

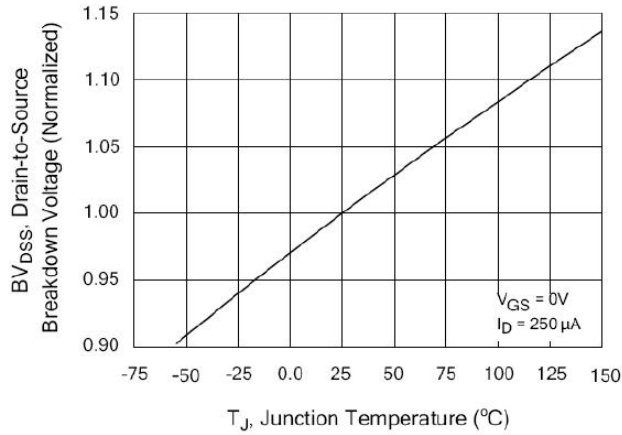


Figure 12. Typical Threshold Voltage vs Junction Temperature

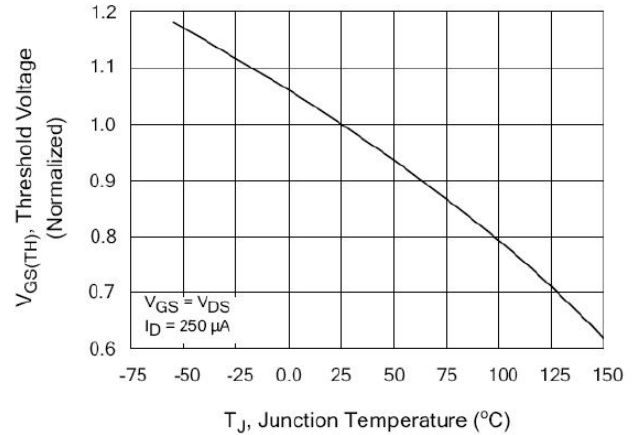


Figure 13. Maximum Safe Operating Area

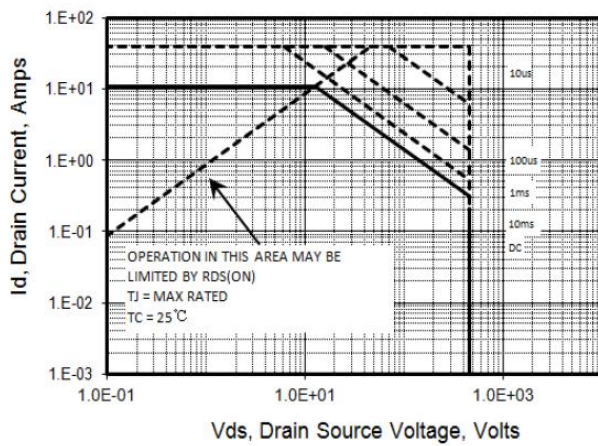


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

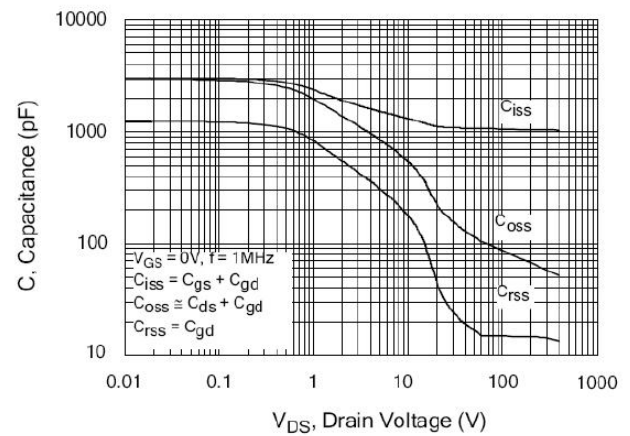


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

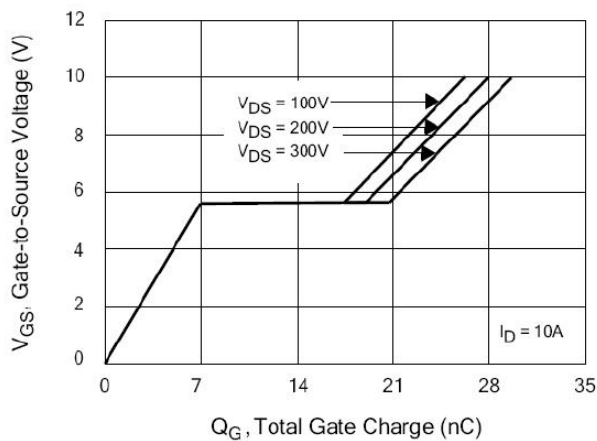
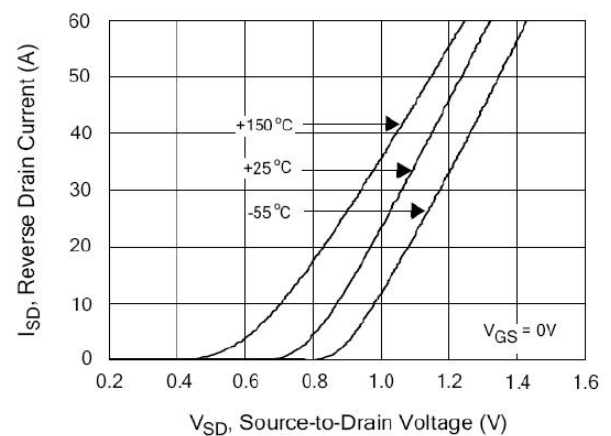


Figure 16. Typical Body Diode Transfer Characteristics



9. Test Circuits and Waveforms

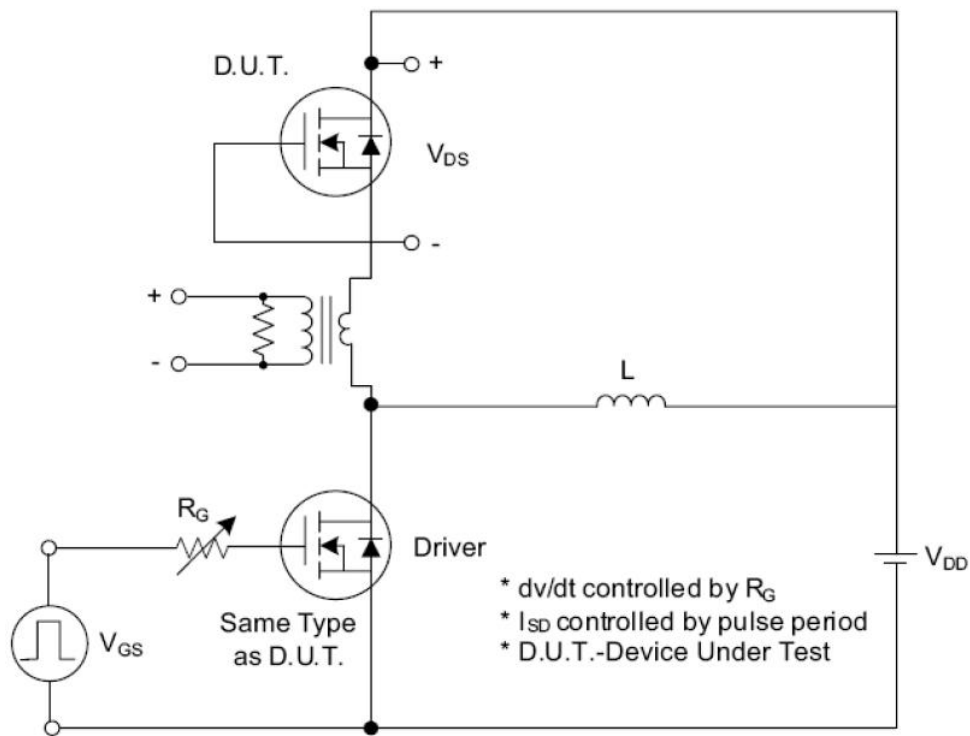


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

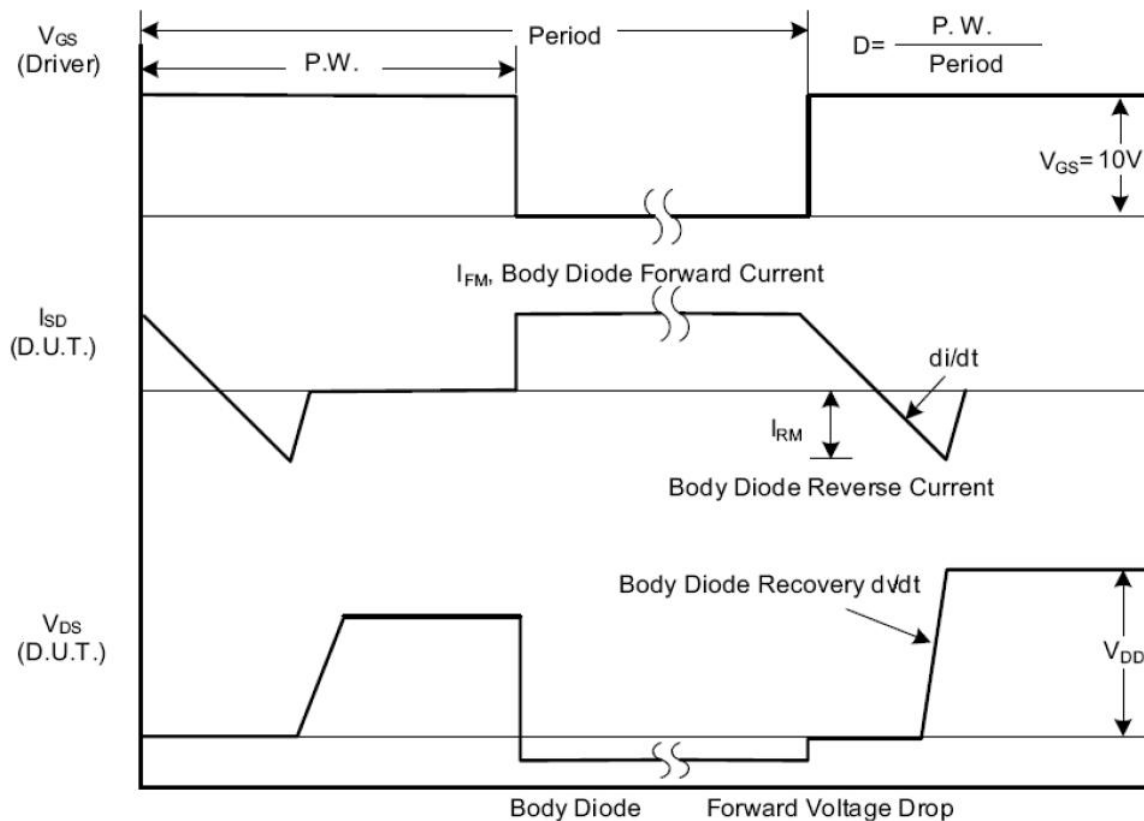


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

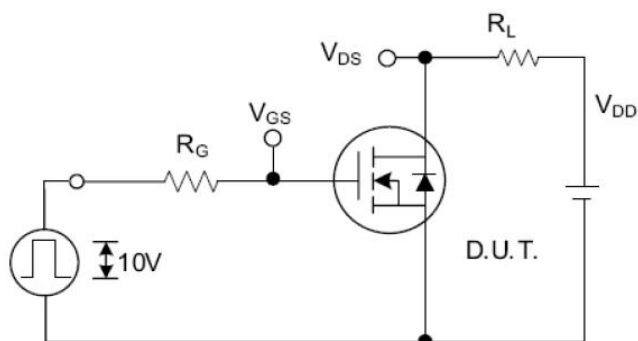


Fig. 2.1 Switching Test Circuit

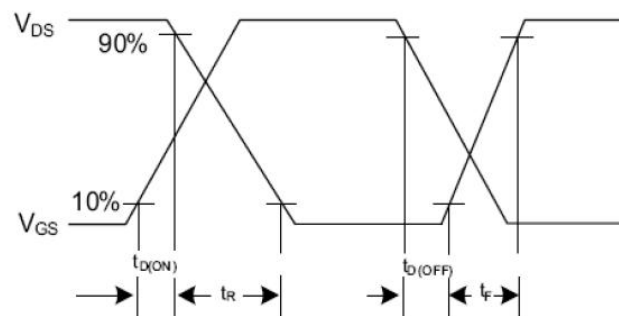


Fig. 2.2 Switching Waveforms

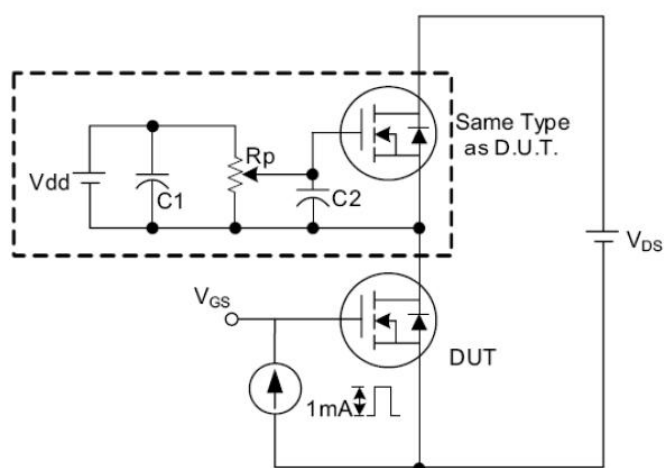


Fig. 3.1 Gate Charge Test Circuit

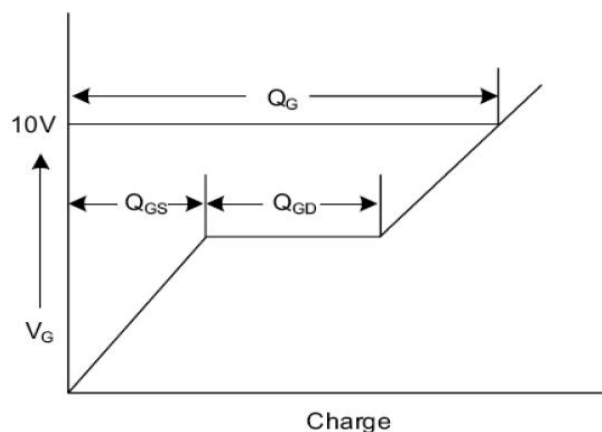


Fig. 3.2 Gate Charge Waveform

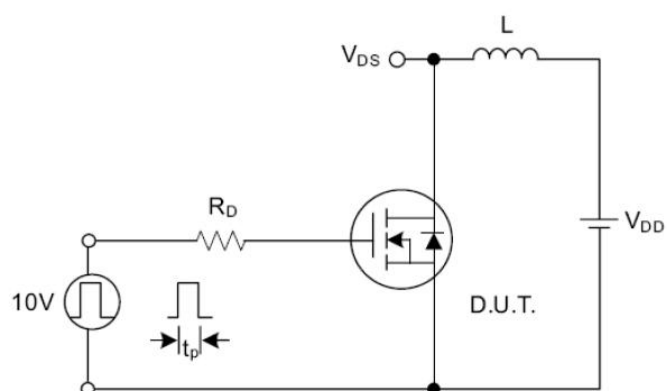


Fig. 4.1 Unclamped Inductive Switching Test Circuit

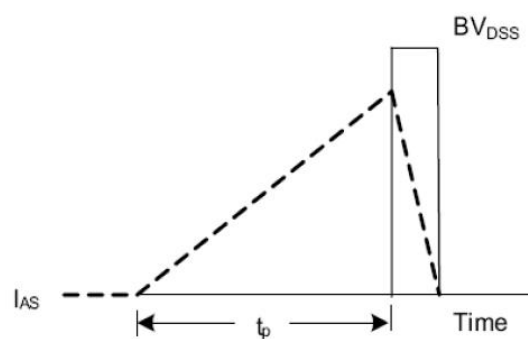


Fig. 4.2 Unclamped Inductive Switching Waveforms