# TMI8421 Stepper Motor Controller IC

#### **FEATURES**

- 6-V to 35-V Operating Supply Voltage Range
- . PWM Microstepping Stepper Motor Driver
  - Built-In Microstepping Indexer
  - Up to 1/16 Microstepping
- Multiple Decay Modes
  - Slow Decay
  - Mixed Decay
- Simple STEP/DIR Interface
- . Low Current Sleep Mode
- Built-In 5-V Reference Output
- Protection Features
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - VM Undervoltage Lockout (UVLO)
  - Fault Condition Indication Pin (nFAULT)
- Small Package and Footprint
  - QFN5x5-28L

#### **APPLICATIONS**

- . Automatic Teller Machines
- Video Security Cameras
- Printers and Scanners
- Money Handing Machines
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Robotics

### **GENERAL DESCRIPTION**

The TMI8421 is a complete microstepping motor driver with built-in translator for easy operation. It is designed to operate bipolar stepper motors in full-, half-, quarter-, eighth-, and sixteenth-step modes, with an output drive capacity of up to 35 V and ±2 A. Simply inputting one pulse on the STEP input drives the motor one microstep.

During stepping operation, the chopping control in the TMI8421 automatically selects the current decay mode, Slow or Mixed. In Mixed decay mode, the device is set initially to a fast decay for a proportion of the fixed off-time, then to a slow decay for the remainder of the off-time. Mixed decay current control results in reduced audible motor noise, increased step accuracy, and reduced power dissipation, Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation.

Internal circuit protection includes: thermal shutdown , undervoltage lockout (UVLO), and crossover-current protection. Fault conditions are indicated on nFAULT. Special power-on sequencing is not required.

The TMI8421 is supplied in a surface-mount QFN package(ES),  $5 \times 5$  mm, with a nominal overall package height of 0.90 mm and an exposed pad for enhanced thermal dissipation. It is lead (Pb) free(suffix-T), with 100% matter tin plated leadframes.

# **TYPICAL APPILCATION**

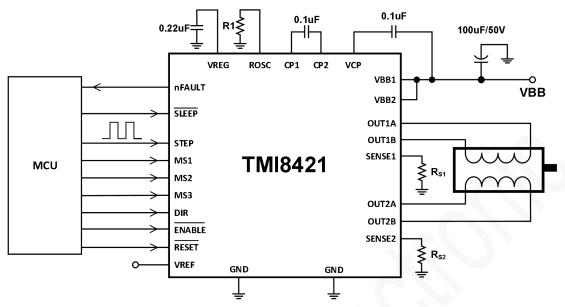


Figure 1. Basic Application Circuit

# ABSOLUTE MAXIMUM RATINGS (Note 1)

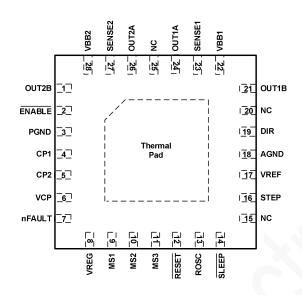
Parameter	Min	Max	Unit
Power supply voltage (VBB)	-0.3	45	V
Logic input voltage	-0.3	5.5	V
Reference input voltage (VREF)	-0.3	5.5	V
Continuous motor drive output current	0	2	Α
Operating ambient temperature	-40	85	°C
T <sub>J</sub> , operating virtual junction temperature (Note 2)	-40	150	°C
Storage temperature	-60	150	°C

### **ESD RATING**

Items	Description	Value	Unit
V <sub>ESD</sub>	Human Body Model for all pins	±2000	V

**JEDEC specification JS-001** 

# **PACKAGE/ORDER INFORMATION**



QFN5x5-28L (Top view)

TMI8421/XXXXX (TMI8421: Device Code, XXXXX: Inside Code) for TMI8421

Part Number	Package	Top mark	Quantity/ Reel
TMI8421	OENEVE 201	TMI8421	5000/盘
	QFN5x5-28L	XXXXX	5000/盃

The TMI8421 device is Pb-free and RoHS compliant.

# **PIN FUNCTIONS**

	PIN		Eurotion
Number	Name	I/O <sup>(1)</sup>	Function
3, 18	GND	-	Device ground.
22	VBB1	-	Bridge 1 power supply. Connect a 0.1µF bypass capacitor to ground, as well as a sufficient bulk capacitance rated for VBB1.
28	VBB2	-	Bridge 2 power supply. Connect a 0.1µF bypass capacitor to ground, as well as a sufficient bulk capacitance rated for VBB2.
8	VREG	0	Regulator decoupling terminal. Connect a 0.22µF ceramic capacitor to ground.
4	CP1	Ю	Charge pump flying capacitor.
5	CP2	Ю	Charge pump flying capacitor.
6	VCP	Ю	High-side gate drive voltage. Connect a 0.1µF ceramic capacitor to VBB.
7	nFAULT	OD	Fault. Logic low when in fault condition (overtemp, overcurrent).
2	ENABLE	I	Logic high to disable device outputs and indexer operation, logic low to enable. Internal pulldown.

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TMI8421 V1.3 2023.08

# PIN FUNCTIONS (Continued)

	PIN		Eurotion		
Number	Name	I/O <sup>(1)</sup>	Function		
14	SLEEP	I	Sleep mode input. Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown.		
12	RESET	I	Reset input. Logic low sets the translator to a predefined Home state(shown in Figures 3 through 7), and turns off all the FET outputs. All STEP inputs are ignored until the logic is set to high. Internal pulldown.		
16	STEP	I	Rising edge causes the indexer to move one step. Internal pulldown.		
19	DIR	I	Direction input. Level sets the direction of stepping. Internal pulldown.		
9	MS1	I	Microston mode/4/2/2\ MC4 MC2 act the stan mode, full 4/2		
10	10 MS2		Microstep mode(1/2/3). MS1 - MS3 set the step mode - full, 1/2, 1/4, 1/8 or 1/16 step. Internal pulldown.		
11	MS3	I	1/4, 1/0 or 1/10 step. Internal pulldown.		
13	ROSC	0	Timing set. Externally programmable Fixed Off-Time.		
17	VREF	I	Current set reference input.		
23	SENSE1	Ю	Bridge 1 ground / Isense. Connect to current sense resistor for bridge 1.		
27	SENSE2	Ю	Bridge 2 ground / Isense. Connect to current sense resistor for bridge 2.		
24	OUT1A	0	Bridge 1 output A .		
21	OUT1B	0	Bridge 1 output B.		
26	OUT2A	0	Bridge 2 output A .		
1	OUT2B	0	Bridge 2 output B .		
15, 20, 25	NC	NC	Not connected.		

<sup>(1)</sup> Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

# RECOMMENDED OPERATING CONDITIONS

Items	Description	Min	Max	Unit
VBB	Power supply voltage range	6.0	35	V
VREF	VREF input voltage	1	4	V

<sup>(1)</sup> All VBB pins must be connected to the same supply voltage.

<sup>(2)</sup> Operational at VREF between 0V and 1V, but accuracy is degraded.

# **ELECTRICAL CHARACTERISTICS**

# T<sub>A</sub> =25°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
VBB operating voltage	V <sub>BB</sub>	Operating	6	-	35	V
\/DD		VBB = 24V, f <sub>PWM</sub> < 50kHz			4	mA
VBB operating supply current	I <sub>VBB</sub>	Operating, outputs disabled			2	mA
VBB sleep mode supply		Ola an Maria			-	
current	I <sub>VBBQ</sub>	Sleep Mode			5	uA
VREG voltage	$V_{REG}$	I <sub>O</sub> = 0 to 1 mA, VBB = 24V, T <sub>J</sub> = 25°C		5		V
LOGIC-LEVEL INPUTS(SI	EEP, RESI	ET, EN, MS1, MS2, MS3, STE	P, DIR)			
Input low voltage	V <sub>IL</sub>				0.7	V
Input high voltage	V <sub>IH</sub>		1.5		5.5	V
Input hysteresis	V <sub>HYS</sub>			0.25		V
Input low current	I <sub>IL</sub>	VIN = 0V	-20	<1	20	μA
Input high current	I <sub>IH</sub>	VIN = 5V		50		μA
Internal pulldown resistance	R <sub>PD</sub>	Pull down to GND		100		kΩ
OPEN-DRIN OUTPUTS(nF	AULT)				1	
Output low voltage	V <sub>OL</sub>	I <sub>OD</sub> = 5mA			0.7	V
Output high leakage current	l <sub>oz</sub>	V <sub>OD</sub> = 5V			1	μA
MOTOR DRIVER						
HS FET on resistance	R <sub>DS(ON)</sub>	VBB = 24V, I <sub>O</sub> = 1.5A		300		mΩ
LS FET on resistance	R <sub>DS(ON)</sub>	VBB = 24V, I <sub>O</sub> = 1.5A		300		mΩ
Body diode forward voltage	V <sub>D</sub>	I <sub>O</sub> = 1.5 A		0.9	1.2	V
Current sense blanking time	t <sub>BLANK</sub>			3		μs
Fixed Off-Time	4	OSC = 5V or GND	20	30	40	μs
Fixed Oil-Time	toff	Rosc = 25 kΩ	23	30	37	μs
Rise time	t <sub>RISE</sub>	OUTx rising 10% to 90%	15		70	ns
Fall time	t <sub>FALL</sub>	OUTx falling 90% to 10%	25		45	ns
Dead time	t <sub>DEAD</sub>		100	475	800	ns
CURRENT CONTROL						
Reference input voltage	V <sub>REF</sub>		0		4	V
Reference input current	I <sub>REF</sub>		-3		3	μA
		VREF = 2 V, %ITripMAX = 38.27%			±15	%
Current trip-level error	errı	VREF = 2 V, %ITripMAX = 70.71%			±5	%
		VREF = 2 V, %ITripMAX = 100.00%			±5	%
Current sense amplifier gain	Aisense	Reference only		8		V/V

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TMI8421 V1.3 2023.08 5

# **ELECTRICAL CHARACTERISTICS** (Continued)

# T<sub>A</sub> = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER	SYMBOL	OL TEST CONDITIONS N		TYP	MAX	UNIT			
PROTECTION CIRCUITS									
VPP underveltage leekeut	Vuvlo_fall	VBB falls until UVLO triggers			4.7	V			
VBB undervoltage lockout	V <sub>UVLO_rise</sub>	VBB rises until operation recovers	4.9			V			
VBB undervoltage hysteresis	V <sub>UVLO_HYS</sub>			0.15		V			
Overcurrent protection trip level	I <sub>OCP</sub>			4.0		Α			
Thermal shutdown temperature	T <sub>SD (Note 3)</sub>			165		$^{\circ}$			
Thermal shutdown hysteresis	THYS (Note 3)			15		$^{\circ}\mathbb{C}$			

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:**  $T_J$  is calculated from the ambient temperature  $T_A$  and power dissipation  $P_D$  according to the following formula:  $T_J = T_A + P_D \times \theta_{JA}$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_{D \text{ (MAX)}} = (T_{J \text{(MAX)}} - T_A)/\theta_{JA}$ .

Note 3: Thermal shutdown threshold and hysteresis are guaranteed by design.

# **Functional Description**

#### Overview

The TMI8421 can be powered with a supply voltage between 6 V and 35 V and is capable of providing an output current up to 2 A full-scale.

The TMI8421 is a complete microstepping motor driver with a built-in translator for easy operation with minimal control lines. It is designed to operate bipolar stepper motors in full-, half-, quarter-, eighth, and sixteenth-step modes. The currents in each of the two output full-bridges and all of the N-channel DMOS FETs are regulated with fixed off-time PWM (pulse-width modulated) control circuitry.

At each step, the current for each full-bridge is set by the value of its external current sense resistor ( $R_{S1}$  and  $R_{S2}$ ), a reference voltage (VREF), and the output voltage of its DAC (which in turn is controlled by the output of the translator). At power-on or reset, the translator sets the DACs and the phase current polarity to the initial Home state (shown in Figures 3 through 7), and the current regulator to Mixed decay mode for both phases. When a step command signal occurs on the STEP input, the translator automatically sequences the DACs to the next level and current polarity. (See Table 2 for the current-level sequence.) The microstep resolution is set by the combined effect of the MSx inputs, as shown in Table 1.

When stepping, if the new output levels of the DACs are lower than their previous output levels, then the decay mode for the active full-bridge is set to Mixed. If the new output levels of the DACs are higher than or equal to their previous levels, then the decay mode for the active full-bridge is set to Slow. This automatic current decay selection improves microstepping performance by reducing the distortion of the current waveform that results from the back EMF of the motor.

#### Microstep Select (MSx)

The microstep resolution is set by the voltage on logic inputs MSx, as shown in Table 1. The MS1, MS2 and MS3 pins have a 100 k $\Omega$  pull-down resistance. When changing the step mode, the change does not take effect until the next STEP rising edge. If the step mode is changed without a translator reset, and absolute position must be maintained, it is important to change the step mode at a step position that is common to both step modes in order to avoid missing steps. When the device is powered down, or reset due to TSD or an overcurrent event, the translator is set to the home position which is by default common to all step modes.

Table 1. Microstepping Resolution Truth Table

MS1	MS2	MS3	Microstep Resolution	Excitation Mode
L	L	L	Full Step	2 Phase
Н	L	L	Half Step	1-2 Phase
L	Н	L	Quarter Step	W1-2 Phase
Н	Н	L	Eighth Step	2W1-2 Phase
Н	Н	Н	Sixteenth Step	4W1-2 Phase
L	L	Н	Full Step	2 Phase
Н	L	Н	Half Step	1-2 Phase
L	Н	Н	Quarter Step	W1-2 Phase

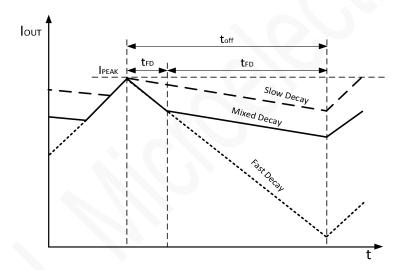
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TMI8421 V1.3 2023.08 7

#### **Mixed Decay Operation**

The bridge operates in Mixed decay mode, at power-on and reset, and during normal running according to the ROSC configuration and the step sequence, as shown in Figures 3 through 7. During Mixed decay mode, when the trip point is reached, the TMI8421 initially goes into a fast decay interval for 31.25% of the off-time, t<sub>OFF</sub>. After that, it switches to slow decay for the remainder of t<sub>OFF</sub>. A timing diagram for this feature appears in Figure 2.

Typically, mixed decay is only necessary when the current in the winding is going from a higher value to a lower value as determined by the state of the translator. For most loads, automatically selected mixed decay is convenient because it minimizes ripple when the current is rising and prevents missed steps when the current is falling. For some applications where microstepping at very low speeds is necessary, the lack of back EMF in the winding causes the current to increase in the load quickly, resulting in missed steps. By pulling the ROSC pin to ground, mixed decay is set to be active 100% of the time, for both rising and falling currents, and prevents missed steps. If this is not an issue, it is recommended that automatically selected mixed decay be used, because it will produce reduced ripple currents. Refer to the Fixed Off-Time section for details.



Symbol	Characteristic
t <sub>off</sub>	Device fixed off-time
I <sub>PEAK</sub>	Maximum output current
t <sub>SD</sub>	Slow decay interval
t <sub>FD</sub>	Fast decay interval
Іоит	Device output current

Figure 2: Current Decay Modes Timing Chart

#### **Low Current Microstepping**

Intended for applications where the minimum on-time prevents the output current from regulating to the programmed current level at low current steps. To prevent this, the device can be set to operate in Mixed decay mode on both rising and falling portions of the current waveform. This feature is implemented by shorting the ROSC pin to ground. In this state, the off-time is internally set to  $30 \, \mu s$ .

#### Step Input

A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs and the direc- tion of current flow in each winding. The size of the increment is determined by the combined state of the MSx inputs.

#### **Current Regulation**

Each full-bridge is con- trolled by a fixed off-time PWM current control circuit that limits the load current to a desired value,  $I_{TRIP}$ . Initially, a diagonal pair of source and sink FET outputs are enabled and current flows through the motor winding and the current sense resistor,  $R_{Sx}$ . When the voltage across  $R_{Sx}$  equals the DAC output voltage, the current sense comparator resets the PWM latch. The latch then turns off the appropriate source driver and initiates a fixed off time decay mode.

The maximum value of current limiting is set by the selection of RSx and the voltage at the VREF pin. The transconductance func- tion is approximated by the maximum value of current limiting, I<sub>TripMAX</sub> (A), which is set by

$$I_{TripMAX} = V_{REF} / (8 X R_s)$$

where  $R_S$  is the resistance of the sense resistor ( $\Omega$ ) and  $V_{REF}$  is the input voltage on the VREF pin (V).

The DAC output reduces the V<sub>REF</sub> output to the current sense comparator in precise steps, such that

$$I_{\text{trip}} = (\%I_{\text{TripMAX}} / 100) \times I_{\text{TripMAX}}$$

(See Table 2 for %I<sub>TripMAX</sub> at each step.)

It is critical that the maximum rating (0.5 V) on the SENSE1 and SENSE2 pins is not exceeded.

#### **Fixed Off-Time**

The internal PWM current control circuitry uses a one-shot circuit to control the duration of time that the DMOS FETs remain off. The off time, t<sub>OFF</sub>, is determined by the ROSC terminal. The ROSC terminal has three settings:

- 1. ROSC tied to 5V: off-time internally set to 30  $\mu$ s; decay mode is automatic Mixed decay except when in full step where decay mode is set to Slow decay.
- 2. ROSC tied directly to ground: off-time internally set to 30  $\mu$ s; current decay is set to Mixed decay for both increasing and decreasing currents for all step modes.
- 3. ROSC through a resistor to ground: off-time is determined by the following formula, the decay mode is automatic Mixed decay for all step modes except full-step which is set to Slow decay.

Where  $t_{OFF}$  is in  $\mu s$ .

Where Toff is in microseconds.

ROSC is allowed in the range  $5k\Omega$  to  $80k\Omega$ .

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#### VBB Undervoltage Lockout (UVLO)

If at any time the voltage on the VBB pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge will be disabled. Operation resumes when VBB rises above the UVLO threshold.

#### **Overcurrent Protection (OCP)**

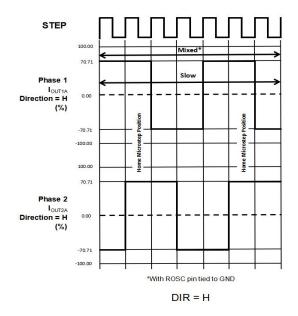
An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The device will remain disabled until either SLEEP pin is applied, or VBB is removed and re-applied.

Overcurrent conditions on both high and low side devices; that is, a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the ISENSE resistor value or VREF voltage.

#### Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

#### **Application Curves**



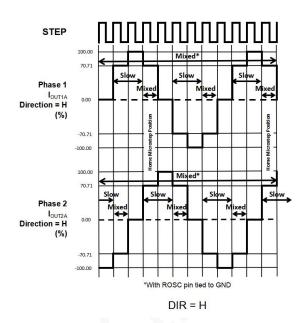


Figure 3: Decay Modes for Full-Step Increments

Figure 4: Decay Modes for Half-Step Increments

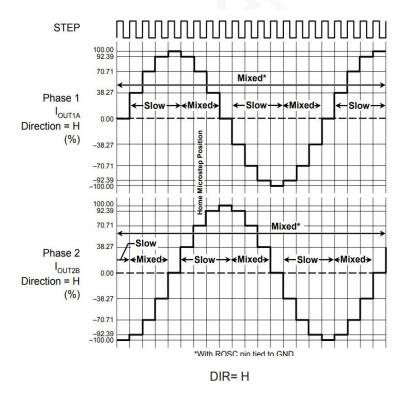


Figure 5: Decay Modes for Quarter-Step Increments

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TMI8421 V1.3 2023.08

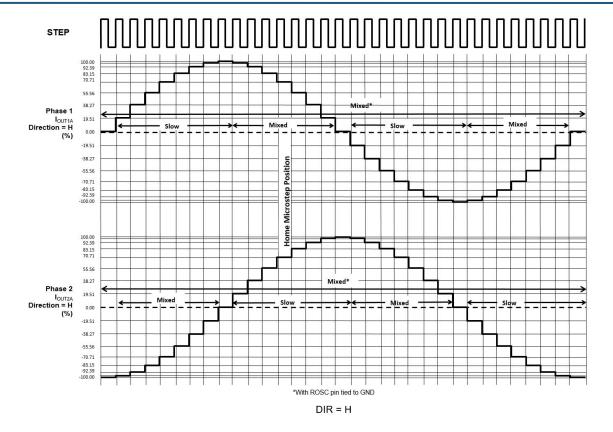


Figure 6: Decay Modes for Eighth-Step Increments

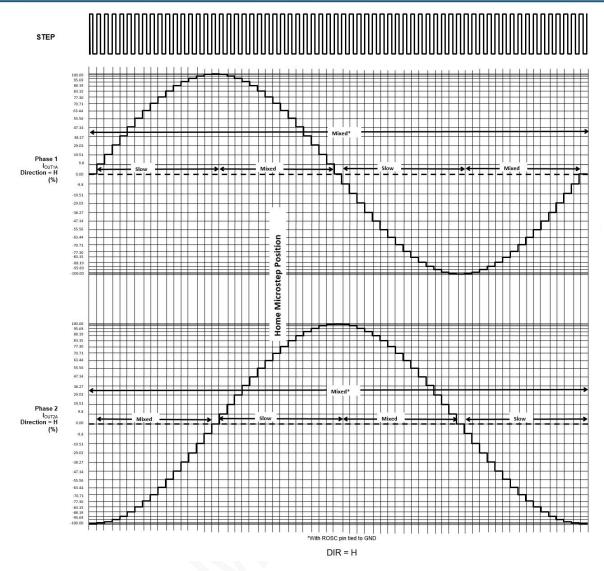


Figure 7: Decay Modes for Sixteenth-Step Increments

Table 2: Step Sequencing Settings
Home microstep position at Step Angle 45°; DIR = H

					Phase1	Phase2	
Full	Half	1/4	1/8	1/16	Current	Current	Step
Step	Step	Step	Step	Step	[% I <sub>tripMax</sub> ]	[% I <sub>tripMax</sub> ]	Angle
#	#	#	#	#	(%)	(%)	(°)
	1	1	1	1	100.00	0.00	0.0
				2	99.52	9.80	5.6
			2	3	98.08	19.51	11.3
				4	95.69	29.03	16.9
		2	3	5	92.39	38.27	22.5
				6	88.19	47.14	28.1
			4	7	83.15	55.56	33.8
				8	77.30	63.44	39.4
1	2	3	5	9	70.71	70.71	45.0
				10	63.44	77.30	50.6
			6	11	55.56	83.15	56.3
				12	47.14	88.19	61.9
		4	7	13	38.27	92.39	67.5
				14	29.03	95.69	73.1
			8	15	19.51	98.08	78.8
				16	9.80	99.52	84.4
	3	5	9	17	0.00	100.00	90.0
				18	-9.80	99.52	95.6
			10	19	-19.51	98.08	101.3
				20	-29.03	95.69	106.9
		6	11	21	-38.27	92.39	112.5
				22	-47.14	88.19	118.1
			12	23	-55.56	83.15	123.8
				24	-63.44	77.30	129.4
2	4	7	13	25	-70.71	70.71	135.0
				26	-77.30	63.44	140.6
			14	27	-83.15	55.56	146.3
				28	-88.19	47.14	151.9
		8	15	29	-92.39	38.27	157.5
				30	-95.69	29.03	163.1
			16	31	-98.08	19.51	168.8
				32	-99.52	9.80	174.4

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14

Table 2: Step Sequencing Settings<sub>(Continued)</sub>
Home microstep position at Step Angle 45°; DIR = H

	1	H-	ome micro	ostep posi	tion at Step Angle		
Full	Half	1/4	1/8	1/16	Phase1	Phase2	Step
Step	Step	Step	Step	Step	Current	Current	Angle
#	#	#	#	#	[% I <sub>tripMax</sub> ]	[% I <sub>tripMax</sub> ]	(°)
π	π	#	#	π	(%)	(%)	( )
	5	9	17	33	-100.00	0.00	180.0
				34	-99.52	-9.80	185.6
			18	35	-98.08	-19.51	191.3
				36	-95.69	-29.03	196.9
		10	19	37	-92.39	-38.27	202.5
				38	-88.19	-47.14	208.1
			20	39	-83.15	-55.56	213.8
				40	-77.30	-63.44	219.4
3	6	11	21	41	-70.71	-70.71	225.0
				42	-63.44	-77.30	230.6
			22	43	-55.56	-83.15	236.3
				44	-47.14	-88.19	241.9
		12	23	45	-38.27	-92.39	247.5
				46	-29.03	-95.69	253.1
			24	47	-19.51	-98.08	258.8
				48	-9.80	-99.52	264.4
	7	13	25	49	0.00	-100.00	270.0
				50	9.80	-99.52	275.6
			26	51	19.51	-98.08	281.3
				52	29.03	-95.69	286.9
		14	27	53	38.27	-92.39	292.5
				54	47.14	-88.19	298.1
			28	55	55.56	-83.15	303.8
				56	63.44	-77.30	309.4
4	8	15	29	57	70.71	-70.71	315.0
				58	77.30	-63.44	320.6
			30	59	83.15	-55.56	326.3
				60	88.19	-47.14	331.9
		16	31	61	92.39	-38.27	337.5
				62	95.69	-29.03	343.1
			32	63	98.08	-19.51	348.8
				64	99.52	-9.80	354.4
						1	

## **APPLICATION INFORMATION**

## **Application information**

The TMI8421 can be used to control a bipolar stepper motor. The STEP interface controls the outputs and current control can be implemented with the internal current regulation circuitry. Detailed fault reporting is provided with the internal protection circuits and nFAULT pin.

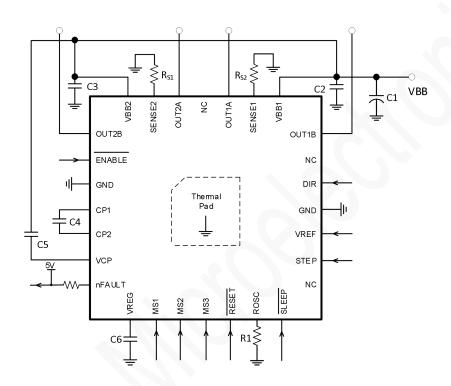


Figure 8. TMI8421 Typical Application

# **Block Diagram**

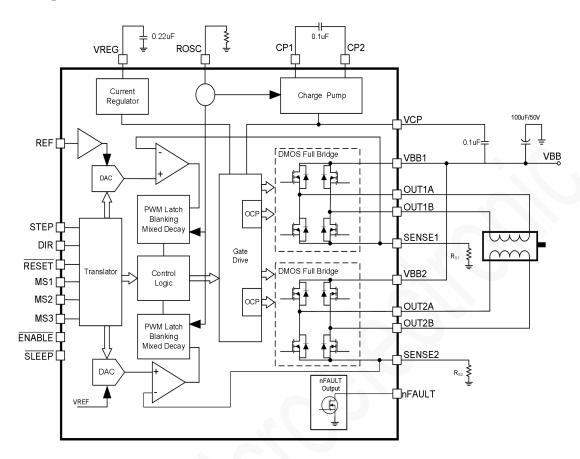
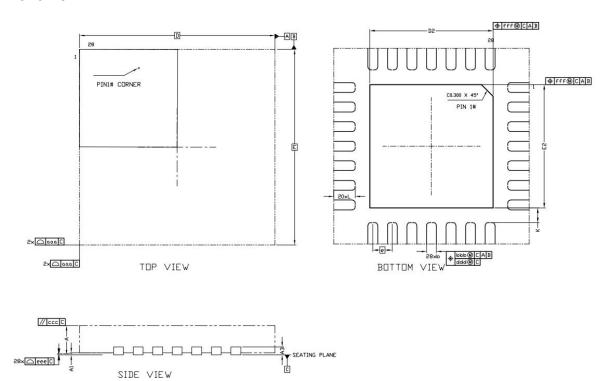


Figure 9. TMI8421 Block Diagram

## **PACKAGE INFORMATION**

#### QFN5x5-28L



Unit: mm

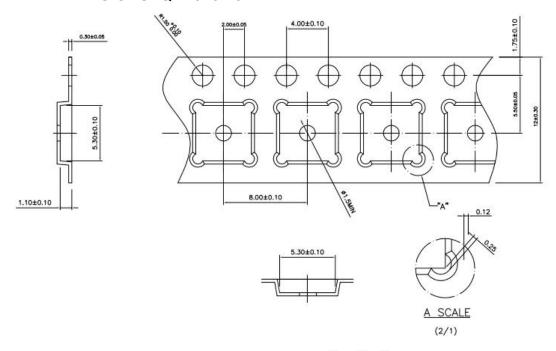
Symbol	Dimensions In Millimeters			Cymbal	Dimensions In Millimeters		
	Min	NOM	Max	Symbol	Min	NOM	Max
А	0.70	0.75	0.80	е	0.50BSC		
	0.80	0.85	0.90	L	0.50	0.55	0.60
A1	0	0.02	0.05	K	0.20	-	-
A3	-	0.20 REF	-	aaa	0.10		
b	0.18	0.25	0.30	bbb	0.10		
D	5.00BSC			ccc	0.10		
E	5.00BSC			ddd	0.05		
D2	3.05	3.15	3.25	eee	0.08		
E2	3.05	3.15	3.25	fff	0.10		

#### Note:

- 1) All dimensions are in millimeters.
- 2) Package length does not include mold flash, protrusion or gate burr.
- 3) Package width does not include inter lead flash or protrusion.
- 4) Lead popularity (bottom of leads after forming) shall be 0.10 millimeters max.
- 5) Pin 1 is lower left pin when reading top mark from left to right.

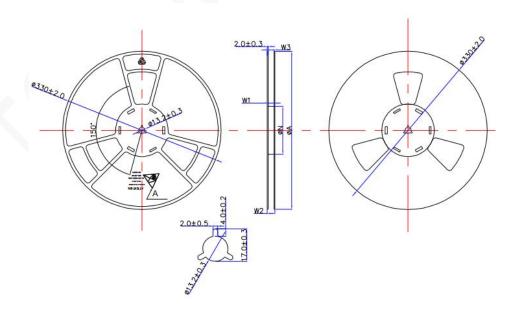
# **TAPE AND REEL INFORMATION**

## **TAPE DIMENSIONS: QFN5x5-28L**



Symbol	Dimensions	Symbol	Dimensions	Symbol	Dimensions	Symbol	Dimensions
A0	6.70±0.10	θ	5° TYP	E	1.75±0.10	D1	1.55MIN
В0	10.05±0.10	t	0.30±0.05	F	7.50±0.10	P0	0.30±0.10
K0	1.50±0.10	W	16.00±0.30	P2	2.00±0.10	10P0	40.00±0.20
K1	1.35±0.10	Р	8.00±0.10	D	1.50±0.10		

#### **REEL DIMENSIONS: QFN5x5-28L**



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19

TMI8421 V1.3 2023.08

Unit: mm

ØA	ØN	W1(+2/0)	W2(Max)	W2(Max)
330±2.0	100±1.0	12.4	18.4	11.9/15.4

#### Note:

- 1) All Dimensions are in Millimeter
- 2) Quantity of Units per Reel is 5000
- 3) MSL level is level 3.

# **Important Notification**

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