TECH PUBLIC
台舟电子

FDS6910-TP

Dual N-Channel Enhancement Mode Power MOSFET

www.sot23.com.tw

GENERAL FEATURES

$R_{DS(ON)}$ ≦16 mΩ@VGS=10V

- $R_{DS(ON)}$ ≦20 mΩ@VGS=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

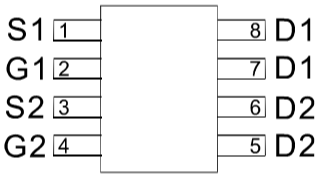
Application

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

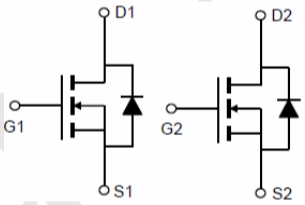
Package and Pin Configuration

(SOP-8)

Top View

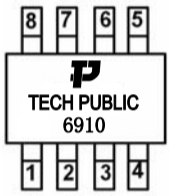


Circuit diagram



Schematic diagram

Marking:



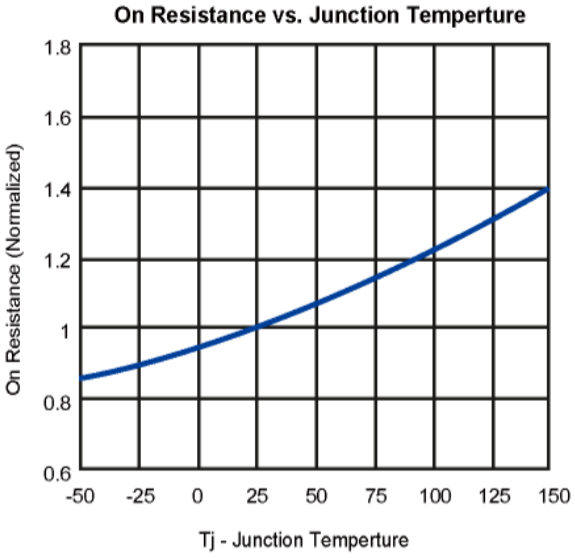
Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

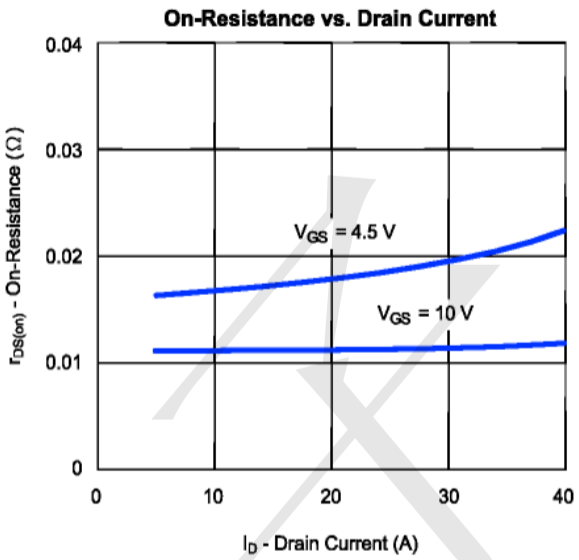
Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25℃	I_D	10	A
	T_A=70℃		8.3	
Pulsed Drain Current		I_{DM}	38	A
Maximum Power Dissipation	T_A=25℃	P_D	2	W
	T_A=70℃		1.2	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	52.0	℃/W

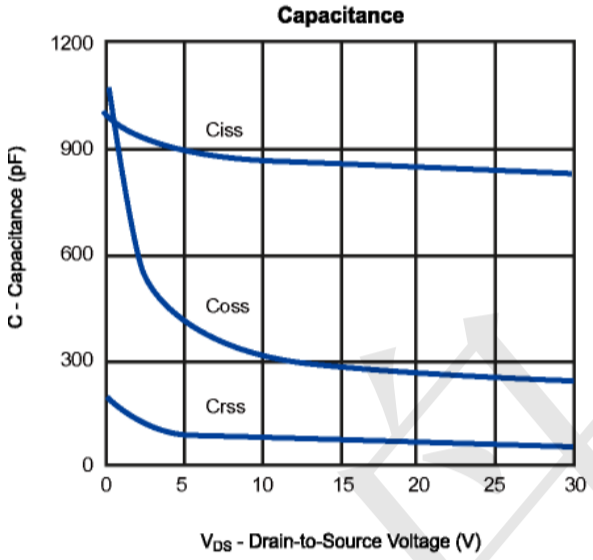
Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

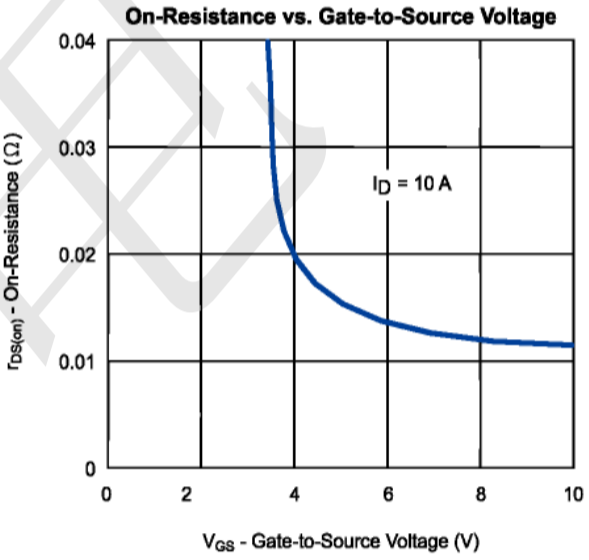
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance [a]	V_{GS}=10V, I_D= 10A		11.2	16	mΩ
		V_{GS}=4.5V, I_D= 8A		15.6	20	
V_{SD}	Diode Forward Voltage	I_S=8.2A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Rg	Gate Resistance	f=1MHz		1		Ω
Qg	Total Gate Charge	V_{DS}=10V, V_{GS}=4.5V, I_D=8.2A		9.5		nC
Qgs	Post-Vth Gate-Source Charge			3.6		
Qgd	Gate-Drain Charge			3.4		
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		841		pF
Coss	Output Capacitance			250		
Crss	Reverse Transfer Capacitance			71		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L=15Ω I_D=1A, V_{GEN}=10V, R_G=6Ω		14		ns
tr	Turn-On Rise Time			12		
$t_{d(off)}$	Turn-Off Delay Time			43		
tf	Turn-Off Fall Time			4		

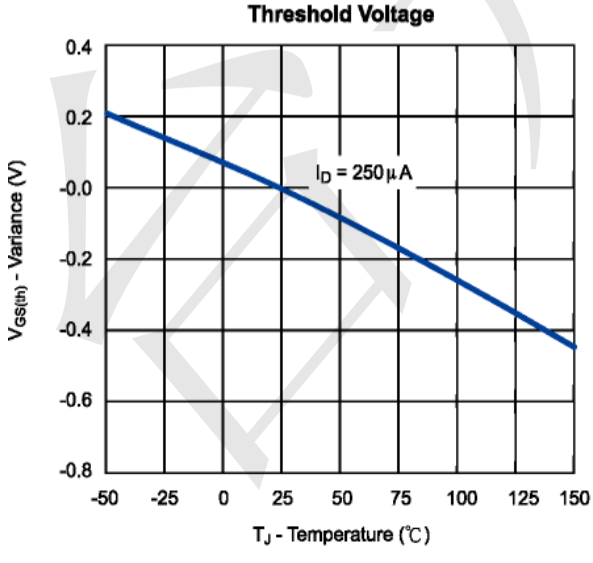
Notes: a. pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice

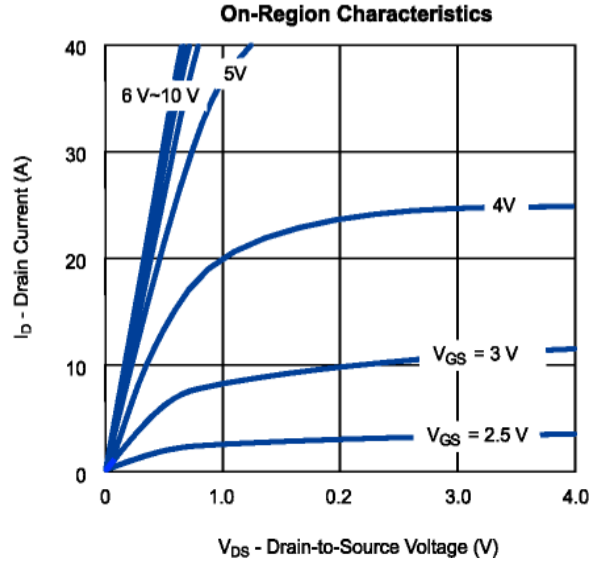

On Resistance vs. Junction Temperture
On Resistance (Normalized)
1.8
1.6
1.4
1.2
1
0.8
0.6
-50 -25 0 25 50 75 100 125 150
Tj - Junction Temperture


On-Resistance vs. Drain Current
rDS(on) - On-Resistance (Ω)
0.04
0.03
0.02
0.01
0
VGS = 4.5 V
VGS = 10 V
0 10 20 30 40
ID - Drain Current (A)

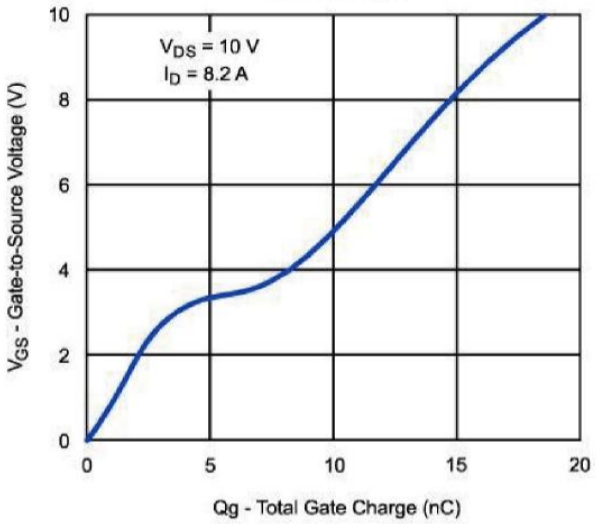

Capacitance
C - Capacitance (pF)
1200
900
600
300
0
Ciss
Coss
Crss
0 5 10 15 20 25 30
VDS - Drain-to-Source Voltage (V)


On-Resistance vs. Gate-to-Source Voltage
rDS(on) - On-Resistance (Ω)
0.04
0.03
0.02
0.01
0
ID = 10 A
0 2 4 6 8 10
VGS - Gate-to-Source Voltage (V)

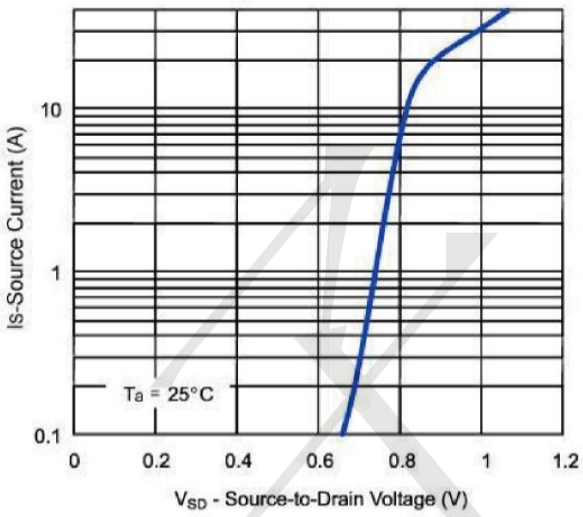

Threshold Voltage
VGS(th) - Variance (V)
0.4
0.2
-0.0
-0.2
-0.4
-0.6
-0.8
ID = 250μA
-50 -25 0 25 50 75 100 125 150
TJ - Temperature (℃)


On-Region Characteristics
ID - Drain Current (A)
40
30
20
10
0
6 V~10 V
5V
4V
VGS = 3 V
VGS = 2.5 V
0 1.0 0.2 3.0 4.0
VDS - Drain-to-Source Voltage (V)

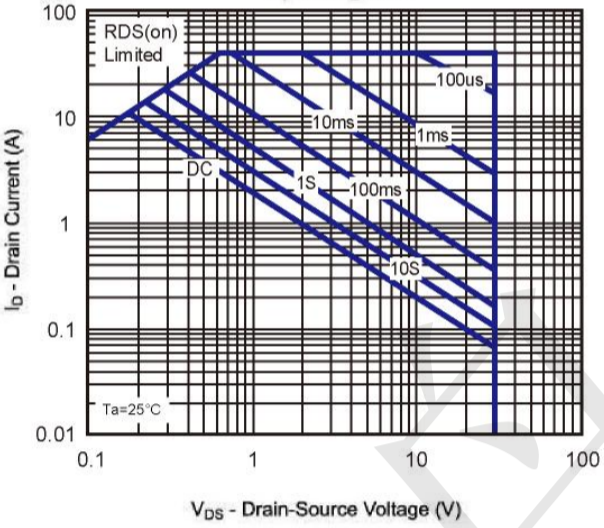
Gate Charge



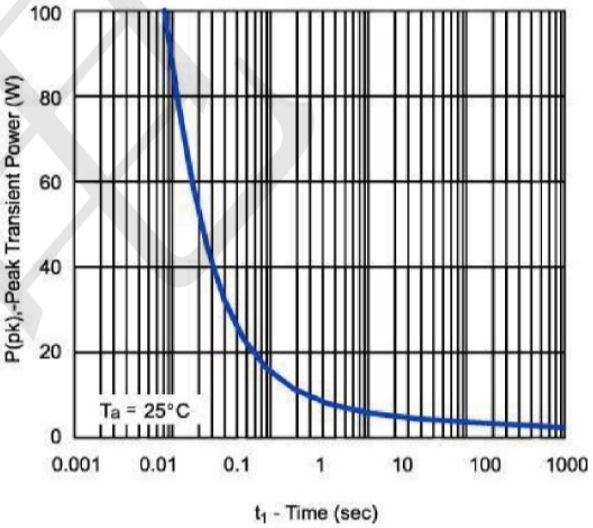
Body-diode characteristics



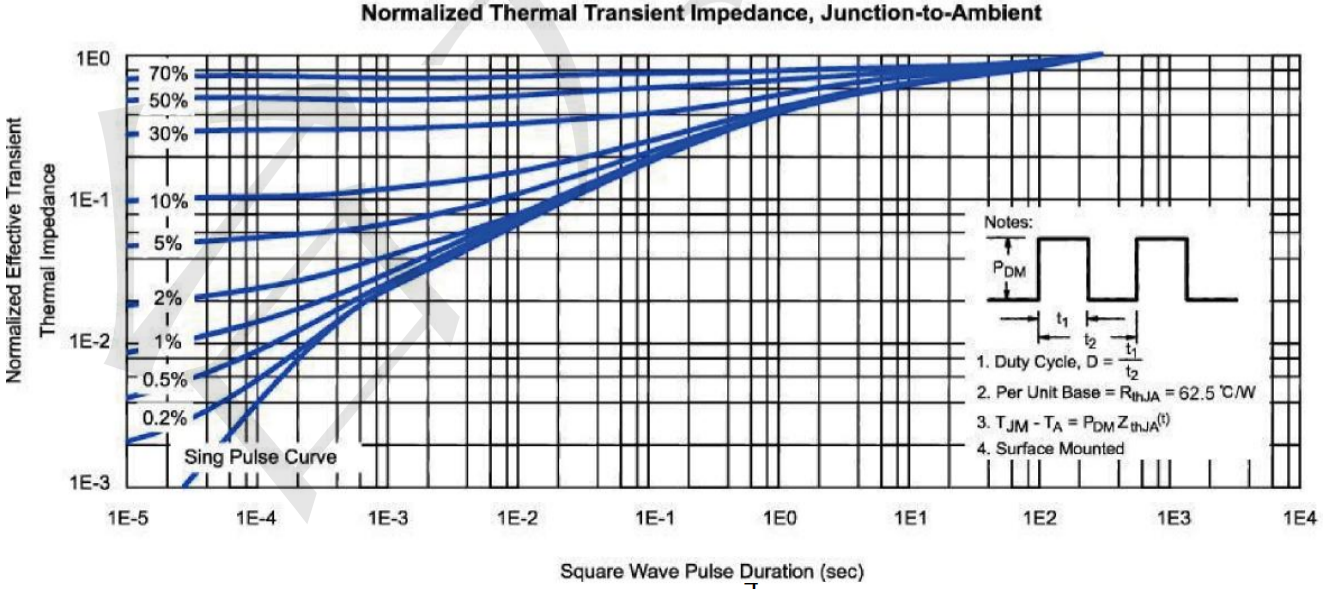
Maximum Forward Biased Safe Operating Area



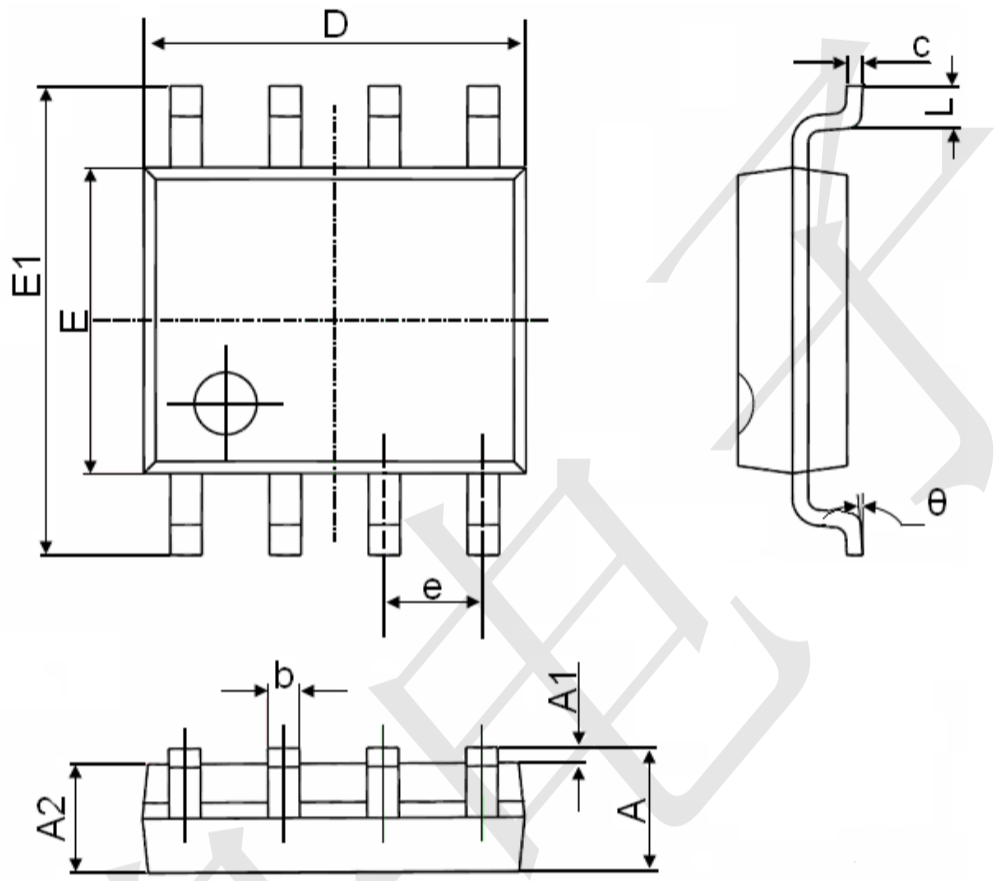
Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°