SYT664

High Current Over Voltage Protection Switch with
High Current Bi-directional DC/DC Regulator And Capacitance Measurement

General Description

SYT664 is a power management IC for the applications of power backup in Solid-State Driver or other backup power supplies which can achieve backup power storage and release functions. The energy is transferred bi-directionally between the BUS side and the energy storage side with high efficiency by bi-directional DC/DC regulator. Fast transient response and excellent stability are achieved by the quasi-fixed frequency constant off time control strategy.

A reverse blocking switch is integrated at the input side to prevent from energy leaking when the input power source is removed or inserted with inverse polarity. The reverse blocking switch also has the programmable current limit function with the program range from 1.2A to 6.2A. Three different BUS over voltage protection (OVP) thresholds are selectable by OVP pin for the applications with different kind of input power source.

I^2C interface is internally integrated in SYT664 to reduce the amount of external components. Control parameters such as input current limit, switching frequency, and boost peak current limit can be programmed by I^2C.

Storage capacitance measurement and abnormal storage capacitor ESR detection circuit are integrated inside of SYT664. The measurement results are stored in internal read only data registers for MCU reading by I^2C interface.

SYT664 along with QFN4×4-25 package provides compact PCB layout to save circuit area for the increase of SSD memory capacity.

Ordering Information

SYT664 □(□□)□

└ Temperature Code

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SYT664RGC	QFN4×4-25	

Features

- Low $R_{DS(ON)}$ for Internal Switches
  - Input Reverse Blocking Switch: 24mΩ (Typical)
  - High-side and Low-side Switches of Bi-directional DC/DC Regulator: 70mΩ /70mΩ (Typical)
  - Disconnect Switch: 40mΩ (Typical)
- 2.6V-16V Input Voltage Range
- Storage Voltage Rating Up to 36V
- Programmable Input Current Limit from 1.2A to 6.2A
- Selectable Over Voltage Protection: 3.8V, 5.7V, and 13.3V
- Reverse Blocking at Input Side to Prevent From Leakage Current
- Programmable Reverse Blocking Switch Turn On Delay Time
- Programmable Reverse Blocking Switch Soft-start Time
- Integrated High-efficiency Bi-directional DC/DC Regulator: Boost Charging Mode and Buck Discharging Mode Auto-alternating According to the Programmed BUS Voltage Detection and Regulation Level
- Programmable Quasi-Fixed Frequency Constant OFF Time Control for Steady-State Operation
- Programmable Boost Charging Peak Current and Adaptive Charging Current Fold-back
- Programmable Storage Voltage
- MTP(Multi-Times Programming) Available for Control Parameters Programming by I^2C
- Short-circuit Protection at Energy Storage Side
- Storage Capacitance Measurement and Abnormal ESR Detection
- Enable Control
- RoHS Compliant and Halogen Free
- Compact Package: QFN4×4-25

Applications

- Solid-state Drivers
- Backup Power Supply

Typical Applications

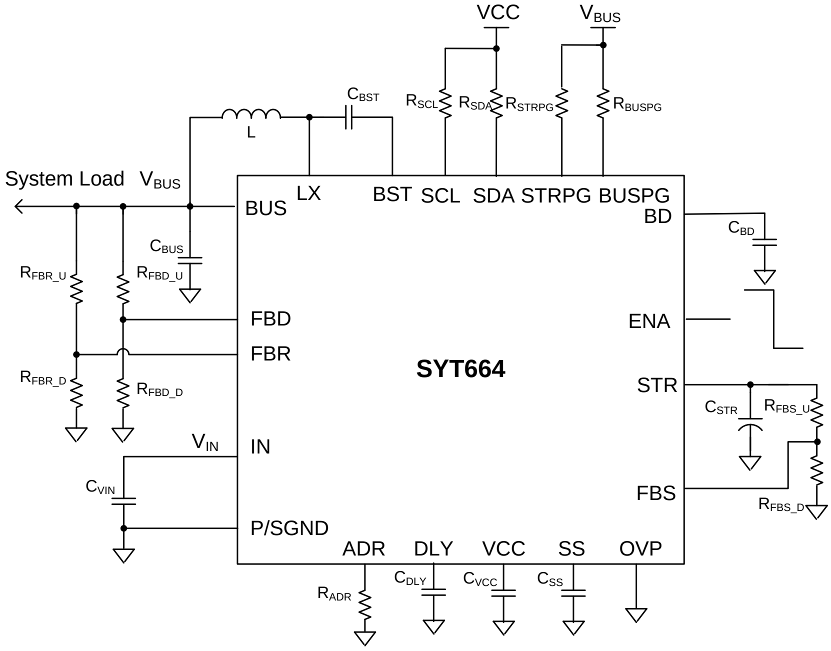


Figure1. Schematic Diagram

Block Diagram

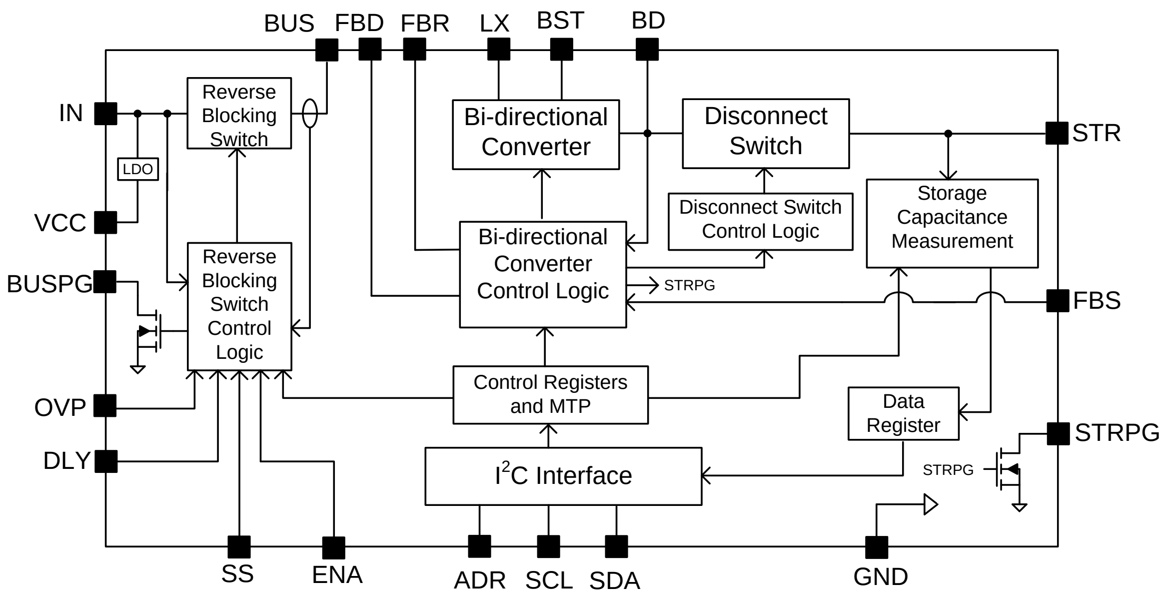
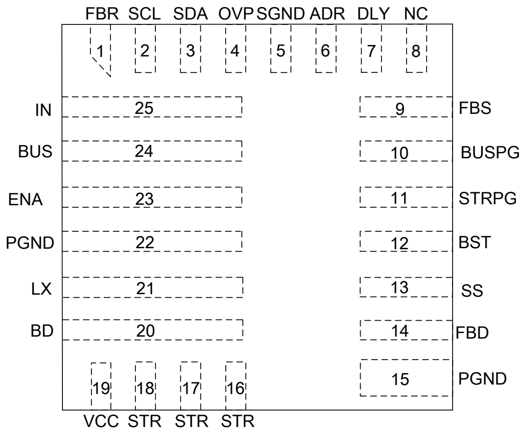


Figure2. Block Diagram

Pinout (top view)



(QFN4×4-25)

Top Mark: BJR*xyz* (device code: BJR, ***x=year code, y=week code, z= lot number code)***

<table>
<tr><td>Pin Name</td><td>Pin Number</td><td>Pin Description</td></tr>
<tr><td>FBR</td><td>1</td><td>Buck mode regulation voltage feedback pin. Using external resistor divider to program the buck regulation point. The internal voltage reference is 0.6V.</td></tr>
<tr><td>SCL</td><td>2</td><td>I^2C interface clock pin.</td></tr>
<tr><td>SDA</td><td>3</td><td>I^2C interface data pin.</td></tr>
<tr><td>OVP</td><td>4</td><td>Output clamp voltage selection for the applications with different input voltage. Pull OVP pin to IN directly to have HIGH logic, or pull OVP pin to GND directly to have LOW logic, or float OVP Pin to select different output clamping thresholds.
<table>
<tr><td rowspan="2">OVP</td><td rowspan="2" colspan="2">IN</td><td colspan="3">Clamping Threshold</td></tr>
<tr><td>Min</td><td>Typ</td><td>Max</td></tr>
<tr><td>Low</td><td>3.3V</td><td>Over 4V</td><td>3.6V</td><td>3.8V</td><td>4.0V</td></tr>
<tr><td>High</td><td>5V</td><td>Over 6V</td><td>5.4V</td><td>5.7V</td><td>6.0V</td></tr>
<tr><td>Float</td><td>12V</td><td>Over 14V</td><td>12.6V</td><td>13.3V</td><td>14V</td></tr>
</table></td></tr>
<tr><td>SGND</td><td>5</td><td>Signal Ground pin.</td></tr>
<tr><td>ADR</td><td>6</td><td>I^2C address selection pin. Pull ADR pin to HIGH by connecting a resistor to IN, or pull ADR pin to LOW by connecting a resistor to ground, or float ADR Pin to select different I^2C address. If ADR pin is pulled high, the I^2C address is 59H. If ADR pin is pulled low, the I^2C address is 5AH. If ADR pin is floated, the I^2C address is 5BH;</td></tr>
<tr><td>DLY</td><td>7</td><td>Reverse blocking switch turn on delay time program pin. Connect a capacitor to GND to program reverse blocking switch turn-on delay time. The approximate programming formula is: $t_{DLY}=C_{DLY}\times2.8\times10^5$.</td></tr>
<tr><td>FBS</td><td>9</td><td>Energy storage capacitor voltage feedback pin. Connect resistor divider to this pin to program the storage voltage. The internal reference is 1.2V. If the resistor connected between FBS and GND is R1, the resistor connected between STR and FBS is R2, then the programmed STR voltage is $V_{STR}=1.2(1+R2/R1)$.</td></tr>
<tr><td>BUSPG</td><td>10</td><td>BUS voltage power good indicator pin. This pin is an open drain output. BUSPG is pulled low if voltage on FBD pin falls below 0.6V, and is pulled high when voltage on FBR pin exceeds 0.63V.</td></tr>
</table>

STRPG	11	STR voltage power good indicator pin. This pin is an open drain output. STRPG is pulled low if voltage on FBS pin falls below 1.08V, and is pulled high when voltage on FBS pin exceeds 1.17V.
BST	12	Boost-Strap pin for bi-directional DC/DC converter to supply high side FET's gate driver. Connect a MLCC cap at least 0.1uF from this pin to LX.
SS	13	Reverse blocking switch soft start program pin. Using external capacitor to program the soft start time.
FBD	14	Buck mode detection feedback pin. The bi-directional converter will enter buck mode when voltage on FBD falls to below 0.6V. Using external resistor divider to program the buck mode detection point.
PGND	15,22	Power Ground pin.
STR	16,17,18	Energy storage capacitor pin. Connect to the energy storage capacitor. Decouple this pin to GND with at least 1uF MLCC cap.
VCC	19	Output of internal 3.3V LDO. Decouple this pin to GND with at least 0.1uF MLCC cap.
BD	20	Connect to the Drain of internal Disconnect FET. Also the input pin of step down DC/DC converter. Decouple this pin to GND with at least 2.2uF MLCC cap.
LX	21	Switching node pin. Connect to external inductor.
ENA	23	Enable Control for both reverse blocking switch and bi-directional converter. High logic to enable the part. It has OR logic with the internal ENA bit.
BUS	24	BUS voltage output pin. Decouple this pin to GND pin with at least 22uF MLCC cap.
IN	25	Input power supply. Decouple this pin to GND with at least 0.1uF MLCC cap.

Absolute Maximum Ratings (Note 1)

STR, BD, LX, BST, FBS--- -0.3V to 38V
IN, BUS, BUSPG, OVP, STRPG, DLY, ADR, FBD, FBR, ENA, BD-STR--------------------------------- -0.3V to 18V
SS, SCL, SDA-- -- -0.3V to 6V
VCC, BST-LX-- -0.3V to 4V
Power Dissipation, PD @ TA = 25℃ QFN4×4-25 --- 1.5W
Package Thermal Resistance (Note 2)

θ JA -- 82℃/W

θ JC -- 10.7℃/W

Junction Temperature Range --- 150℃
Lead Temperature (Soldering, 10 sec.) -- 260℃
Storage Temperature Range -- -65℃ to 150℃

Recommended Operating Conditions (Note 3)

STR, BD, LX, BST, FBS-- -0.3V to 36V
IN, BUS, BUSPG, OVP, STRPG, DLY, ADR, FBD, FBR, ENA, BD-STR--------------------------------- -0.3V to 16V
SS, SCL, SDA--- -0.3V to 5V
VCC, BST-LX-- -0.3V to 3.3V
Junction Temperature Range -- -40℃ to 125℃
Ambient Temperature Range --- -40℃ to 85℃

Electrical Characteristics

(V_{IN} = 5V, V_{SYS} = 5V, L = 4.7µH, V_{BD}=V_{CSTR}=12V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OVP Switch Part						
Input Voltage Range	V_{IN}		2.6		16	V
Input UVLO Rising Threshold	V_{UVLOR}			2.5	2.6	V
Input UVLO Hysteresis	$V_{UVLOHYS}$			300		mV
On Resistance of Reverse Blocking FET	$R_{DS(ON)R}$			24	30	mΩ
Reverse Blocking Current	I_{RB}	V_{IN}=0V, V_{BUS}=16V, V_{ENA}=0V		2	5	µA
Bias Current	I_{BIAS}	V_{IN}=5V, V_{ENCON}=0V		750		µA
Reverse blocking Range	V_{RB}				16	V
Clamping Output Voltage	V_{CLP}	OVP=LOW	3.6	3.8	4.0	V
		OVP=HIGH	5.4	5.7	6.0	V
		OVP=Float	12.6	13.3	14.0	V
Switch Turn On Delay Time	t_{DLY}	C_{DLY}=105nF(Note 5)		29.4		ms
Soft-start Time	T_{SS}	C_{SS}=105nF(Note 6)		14.7		ms
Current Limit Program Range	I_{LIM}		1.2		6.2	A
Current Limit Accuracy			-10%I_{LIM}			
BUSPG Threshold	V_{BUSPGH}	V_{FBR} Rising		0.63		V
	V_{BUSPGL}	V_{FBD} Falling		0.6		V
Internal LDO Output Voltage	V_{VCC}	V_{IN}>3.3V		3.3		V
		V_{IN}<=3.3V		V_{IN}		
ENA Logic	V_{ENAH}		1.5			V
	V_{ENAL}				0.4	V
Bi-Directional DC/DC Regulator Part						
Operation Voltage Range	V_{BUSOP}		2.6		16	V
BUS Operation Rising UVLO Threshold	$V_{BUSUVLO}$		2.2	2.4	2.6	V
BUS Operation UVLO Hysteresis	$V_{BUSHYSF}$			0.25		V
Buck Operation Voltage Range	V_{STROP}		2.6		36	V
Boost Minimum Peak Current	I_{PMIN}			300		mA
Switching Frequency	f_{SWBST}	SF[1:0]=01		500		kHz
LSFET Min ON Time	$t_{OFF,MINL}$			80		ns
HSFET Min ON Time	$t_{ON,MINL}$	I_{PMIN}>1A		80		ns
		I_{PMIN}<1A		40		ns
Boost OVP Threshold	V_{OVPBST}	V_{FBS} Rising		1.2		V
Boost OVP Release Threshold	V_{OVPBST}	V_{FBS} Falling		1.17		V
Mode Change Threshold	V_{MCHGH}	V_{FBR} Rising	0.62	0.635	0.65	V
	V_{MCHGL}	V_{FBD} Falling	0.588	0.6	0.612	V

Buck Detection Voltage Reference	V_{BUCK_DET}		0.588	0.6	0.612	V
Buck Regulation Voltage Reference	V_{BUCK_REG}		0.593	0.6	0.607	V
Maximum Buck Peak Current				8		A
STRPG Threshold	V_{STRPGH}	V_{FBS} Rising		1.17		V
	V_{STRPGL}	V_{FBS} Falling		1.08		V
STR Short Circuit Threshold	V_{STRSC}			0.7		V
Pre-charge Current	I_{PRECHG}			175		mA
$R_{DS(ON)}$ of High Side FET	$R_{DS(ON)H1}$		50	70	80	mΩ
$R_{DS(ON)}$ of Low Side FET	$R_{DS(ON)L1}$		50	70	80	mΩ
$R_{DS(ON)}$ of Disconnect FET	$R_{DS(ON)D}$			37		mΩ
Capacitance Measurement Part						
Capacitance Measurement Discharge Current	$I_{DISCHARGE}$	DCP[7:6]=11		20		mA
Internal Counter Clock	f_{CLK}			500		Hz
Abnormal ESR Detection Discharge Current	I_{ESR}			1		A
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Recovery Hysteresis	T_{HYS}			15		℃

Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Exposed pad of QFN4x4-25 packages is the case position for θJC measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: V_{STR-P} is programmed STR voltage.

Note5: Recommended Delay Time Program Table

DLY cap (nF)	None	10	55	105
Delay time (ms)	1.4	2.8	15.4	29.4

Note6: Recommended Soft-start Time Program Table

SS cap (nF)	None	10	55	105
Rise time (ms)	1	1.4	7.7	14.7

Recommended Formula for C_{SS} & Soft-start Time Calculation

$$T_{SS} = \begin{cases} T_{SS\_DLT}, & \text{No external } C_{SS} \\ \dfrac{C_{SS}}{I_{INT\_SS}}, & T_{SS} > T_{SS\_DLT} \end{cases},$$

Where, TSS_DLT is the internally fixed default soft-start time, about 1ms, which means there's no any external C_{SS}; I_{INT_SS} is the internal current source, about 7.2uA.

Note 7: The typical value of thermal shut down recovery hysteresis is design guaranteed. Recommend to leave enough margin for the application design consideration.

Control Parameters Programming Block Diagram, Register and Data

Block Diagram

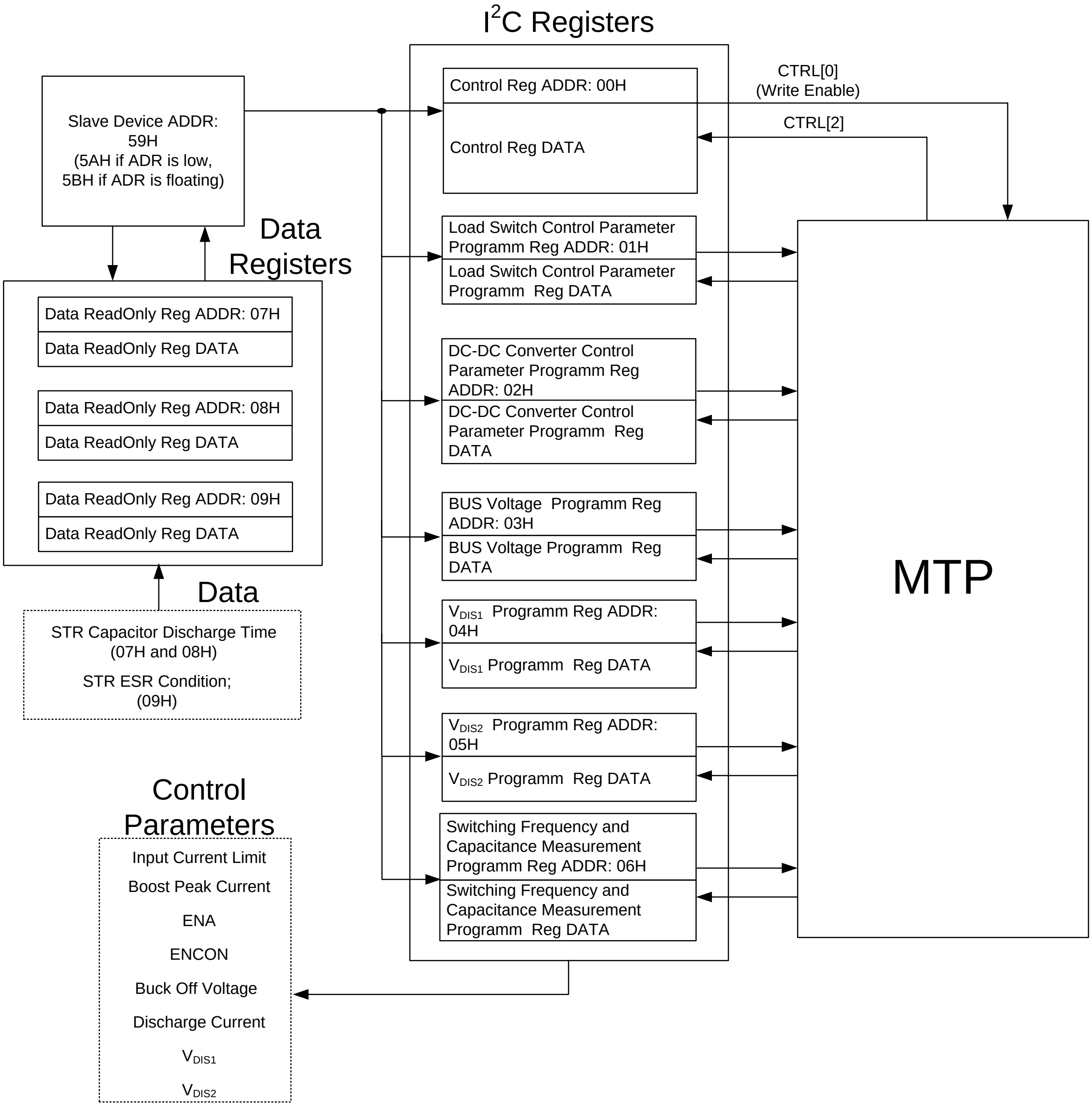
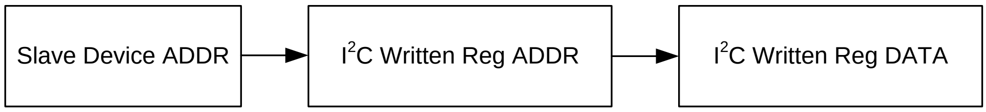


Figure3. Block Diagram

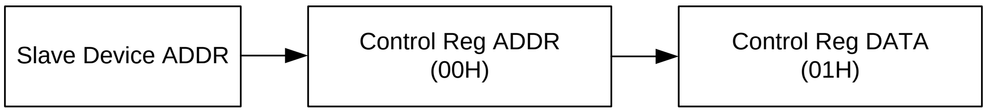
NOTE: Internal current source discharge STR capacitor during capacitance measurement. The counter starts counting when STR voltage falls to V_{DIS1} and stops counting when STR voltage falls to V_{DIS2}.

Control Parameters Programming Sequence

Sequence of Writing DATA to I^2C Registers



Sequence of Writing Register DATA to MTP



NOTE: All the data in I^2C registers is written to MTP when CTRL[0] is set to 1. All the data reserved in MTP is loaded to I^2C registers when IC power up. Please make sure CTRL[2] is 0 before writing data to MTP.

Register and Data

- **Slave Device Address: 59H(5AH or 5BH)+W/R**
- **MTP Control Register Address: 00H**

BIT		**DESCRIPTION**
MTP Read/Write and MUX Selection Control		
Bit 7	CTRL[7]	Reserved
Bit 6	CTRL[6]	Reserved
Bit 5	CTRL[5]	Reserved
Bit 4	CTRL[4]	Reserved
Bit 3	CTRL[3]	Reserved
Bit 2	CTRL[2]	MTP Writing Status, Read Only CTRL[2]=1: MTP Writing Busy CTRL[2]=0: MTP Writing NOT Busy
Bit 1	CTRL[1]	Reserved
Bit 0	CTRL[0]	MTP Write Control CTRL[0]=1: MTP Write Enable CTRL[0]=0: MTP Write Disable Default: 0

◆ **Load Switch Control Parameter Program Register Address: 01H**

BIT		**DESCRIPTION**	
Load Switch Control Parameter Programming			
Bit 7	LSP[7]	Reserved	Default: 38H: Reverse blocking switch and DC/DC are disabled; Current Limit is 6A.
Bit 6	LSP[6]		
Bit 5	LSP[5]	Current Limit Threshold	
Bit 4	LSP[4]		
Bit 3	LSP[3]		
Bit 2	LSP[2]	Reserved	
Bit 1	LSP[1]		
Bit 0	LSP[0]	ENA	

◆ **DC/DC Converter Control Parameter Program Register Address: 02H**

BIT		**DESCRIPTION**	
DC/DC Converter Control Parameters Programming Data			
Bit 7	DCP[7]	Capacitance Measurement Discharge Current	Default: C5H: Converter is enable; boost peak current is 600mA; capacitor health detect discharge current is 20mA
Bit 6	DCP[6]		
Bit 5	DCP[5]	Reserved	
Bit 4	DCP[4]		
Bit 3	DCP[3]	Boost Peak Current	
Bit 2	DCP[2]		
Bit 1	DCP[1]		
Bit 0	DCP[0]	ENCON	

◆ **Buck Off Voltage Program Register Address: 03H**

BIT		**DESCRIPTION**	
Buck Off Voltage Programming Data			
Bit 7	OFF[7]		Default: 37H, V_{BUCK_OFF}=2.64V
Bit 6	OFF[6]		
Bit 5	OFF[5]		
Bit 4	OFF[4]		
Bit 3	OFF[3]		
Bit 2	OFF[2]		
Bit 1	OFF[1]		
Bit 0	OFF[0]		

◆ V_{DIS1} Program Register Address: 04H

BIT		DESCRIPTION	
V_{DIS1} Programming Data			
Bit 7	VDIS1 [7]		Default: 46H, V_{DIS1}=10.5V
Bit 6	VDIS1 [6]		
Bit 5	VDIS1 [5]		
Bit 4	VDIS1 [4]		
Bit 3	VDIS1 [3]		
Bit 2	VDIS1 [2]		
Bit 1	VDIS1 [1]		
Bit 0	VDIS1 [0]		

◆ V_{DIS2} Program Register Address: 05H

BIT		DESCRIPTION	
V_{DIS2} Programming Data			
Bit 7	VDIS2 [7]		Default: 2FH, V_{DIS2}=7.05V
Bit 6	VDIS2 [6]		
Bit 5	VDIS2 [5]		
Bit 4	VDIS2 [4]		
Bit 3	VDIS2 [3]		
Bit 2	VDIS2 [2]		
Bit 1	VDIS2 [1]		
Bit 0	VDIS2 [0]		

◆ Switching Frequency Program Register Address: 06H

BIT		DESCRIPTION	
Switching Frequency and ESR Abnormal Threshold Programming Data for MTP (CTRL[5:3]=101)			
Bit 7	SF [7]	Reserved	Default: 01H, f_{SW}=500kHz; ESR Abnormal threshold is 50mV.
Bit 6	SF [6]	Reserved	
Bit 5	SF [5]	Capacitance Measurement Enable Capacitance measurement starts when SF[5] changes from 0 to 1. Default: 0	
Bit 4	SF [4]	Reserved	
Bit 3	SF [3]	ESR Detection Threshold	
Bit 2	SF [2]		
Bit 1	SF [1]	Switching Frequency	
Bit 0	SF [0]		

◆ ENA Program Table

LSP[0]	Description
0	Reverse blocking switch and DC/DC converter are disable
1	Reverse blocking switch and DC/DC converter are enable

◆ Input Current Limit Program Table

LSP[5]	LSP[4]	LSP[3]	Input Current Limit
0	0	0	1.2A
0	0	1	2A
0	1	0	2.5A
0	1	1	3A
1	0	0	3.5A
1	0	1	4A
1	1	0	4.5A
1	1	1	6.2A

◆ **ENCON Program Table**

DCP[0]	Description
0	DC/DC converter is disabled
1	DC/DC converter is enabled

◆ **Boost Peak Current Program Table**

DCP[3]	DCP[2]	DCP[1]	Boost Peak Current
0	0	0	300mA
0	0	1	500mA
0	1	0	600mA
0	1	1	800mA
1	0	0	1A
1	0	1	1.5A
1	1	0	2A
1	1	1	2.5A

◆ **Capacitance Measurement Discharge Current Program Table**

DCP[7]	DCP[6]	Capacitance Measurement Discharge Current
0	0	2mA
0	1	5mA
1	0	10mA
1	1	20mA

◆ **Switching Frequency Program Table**

SF[1]	SF[0]	Switching Frequency
0	0	250kHz
0	1	500kHz
1	0	1MHz
1	1	1.5MHz

◆ **ESR Detection Threshold Program Table**

SF[3]	SF[2]	ESR Abnormal Threshold
0	0	50mV
0	1	100mV
1	0	150mV
1	1	200mV

◆ **Buck Off Voltage Programming Data Calculation**

$V_{BUCKOFF}$ = REG03 * 0.048 V
For example, if REG03 = 0x37H, then $V_{BUCKOFF} = (3 * 16^1 + 7 * 16^0) * 0.048 = 2.64V$
The buck off voltage program range is 2.64V to 12V.

◆ **V_{DIS1} (V_{DIS2})Voltage Programming Data Table**

V_{DIS1} = REG04 * 0.15 V
For example, if REG04 = 0x0AH, then $V_{DIS1} = (0 * 16^1 + 10 * 16^0) * 0.15 = 1.5V$
The V_{DIS1} voltage program range is 1.5V to 36V.
V_{DIS2} = REG05 * 0.15 V
For example, if REG05 = 0x0AH, then $V_{DIS2} = (0 * 16^1 + 10 * 16^0) * 0.15 = 1.5V$
The V_{DIS2} voltage program range is 1.5V to 36V.

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A reverse blocking switch is integrated at the input side to prevent from energy leaking when the input power source is removed or inserted with inverse polarity. The reverse blocking switch also has the programmable current limit function with the program range from 1.5A to 6A. Three different BUS over voltage protection (OVP) thresholds are selectable by OVP pin for the applications with different kind of input power source.

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Storage capacitance measurement and abnormal storage capacitor ESR detection circuit are integrated inside of SYT664. The measurement results are stored in internal read only data registers for MCU reading by I^2C interface.

SYT664 along with QFN4X4-25 package provides compact PCB layout to save circuit area for the increase of SSD memory capacity.

Function Description

Startup Sequence

When voltage on IN pin is higher than UVLO level and load switch is enabled which means ENA bit (LSP[0]) is 1 or external ENA pin is pulled high, soft start period begins and the capacitor on BUS pin is charged with a current which slowly ramps up from 0 to the programmed current limit after the programmed switch turn on delay time. The soft start time is programmed by the capacitor on SS pin. Capacitor on BD pin will also be charged during the soft start period. When the voltage on BUS pin rises above boost threshold and ENCON (DCP [0]) is 1, pre-charge period starts. The BD voltage is regulated at around 120% - 135% of the BUS voltage and the capacitor on STR pin is charged with around 150mA pre-charge current. The pre-charge period ends when the voltage across the disconnection switch located from BD pin to STR pin is lower than an internal threshold and then the disconnection switch will be fully turned on. Boost converter starts to detect FBS voltage when pre-charge ends.

Bi-directional DC/DC Regulator

DC/DC converter starts working to charge STR capacitor when the pre-charge period is done. Quasi-fixed frequency constant off time control is used and the peak current is programmed by I^2C interface. Burst mode is used to minimize power loss. The maximum storage voltage is programmed by FBS pin. Boost converter stops working when voltage on FBS pin reaches 1.2V and starts to charge the storage capacitor again when FBS voltage falls below around 1.17V.

Buck mode is triggered immediately when the voltage on FBD pin falls below 0.6V. Quasi-fixed frequency constant off time control is also used in buck mode to achieve fast dynamic response. Regulated voltage on BUS pin is programmed by FBR pin. The maximum peak current of buck converter is internally clamped at around 8A. Buck mode will change to boost mode when FBR voltage rise above 0.63V. If STR voltage falls below buck off threshold which is programmed by I^2C interface, buck converter will stop working.

Input Load Switch

Input current limit, over voltage protection and reverse blocking functions are all integrated in reverse blocking switch control module. BUS voltage will be clamped when IN voltage exceed OVP threshold. Clamped voltage and OVP threshold are programmed by OVP pin. Input current limit is set by I^2C interface. Reverse blocking FET will be turned off if any of the following conditions happens:

1. IN voltage falls below UVLO;

2. ENA (LSP[0]) is 0 and ENA pin is pulled to GND;
3. V_{BUS} is higher than V_{IN} (V_{BUS}-V_{IN}>20mV);
4. Bi-directional DC/DC converter works in buck mode.

Short Circuit Protection

If short circuit happens on BUS pin, DC/DC converter will work in buck mode and discharge STR capacitor with maximum peak current till STR voltage is not enough for buck operation or BUS voltage falls to below UVLO. Reverse blocking switch will limit the input current at the programmed level. Thermal shutdown will be active if the inside temperature is higher than the internal threshold.

After pre-charge process last for around 75ms, IC will start to detect STR voltage. If STR voltage cannot be charged above 0.7V during this interval, STR short circuit is detected. The disconnection switch will be turned off and the DC/DC will be latched off. The minimum blanking time is 63ms and the minimum precharge current is 100mA, the 0.7V threshold has +-0.2V tolerance. So the maximum capacitance on STR side is: 100mA * 63ms / 0.9V = 7mF. If STR voltage drops below 0.7V when DC/DC converter is active, STR short circuit will also be detected. The converter will stop working firstly and then disconnect switch will be turned off. Especially, when DC/DC converter operates in boost mode and after the 75ms blanking time, the voltage drop between STR and BUS detection starts and if V_{STR}-V_{BUS}<0.2V is detected, the STR side is treated as short circuit condition. Then, the converter will be latched off firstly and the disconnect switch will be turned off.

STR short circuit detection is disabled during the STR capacitance measurement period. Additionally, the voltage drop detection between STR and BUS is disabled when DC/DC converter operates in buck mode.

Storage Capacitance Measurement

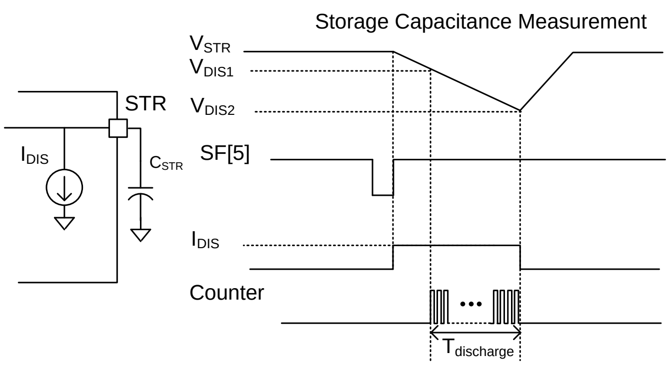
Storage capacitance measurement starts when a rising edge on SF[5] is detected. MCU can start measuring by setting SF[5] to 0 firstly and then setting SF[5] to 1. Firstly, the capacitor ESR detection starts and an internal 1A current source discharges STR for around 15us. At the end of discharging period, STR voltage with voltage drop on ESR is detected. After the discharge current is off, STR voltage without voltage drop on ESR is detected subsequently. If the difference between such two detected voltage values is higher than the programmed ESR detection threshold, ESR error is triggered and the last bit of ESR condition register (address 09H) will be set to 1.

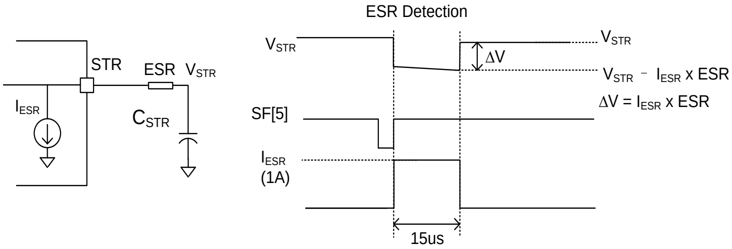
Programmed discharge current I_{DIS} starts to discharge STR capacitors after the ESR detection is finished. Internal 500Hz counter calculates the discharge time starting from when STR voltage falls below $V_{DIS1}$to when STR voltage falls below V_{DIS2}. The discharge time data $T_{DISCHARGE}$ is stored to data register REG07 and REG08. For example, if data read from REG07 is 0x12H, data read from REG08 is 0x34H, the $T_{DISCHARGE}$ should be calculated below:

$T_{DISCHARGE}$=0X1234H= $(1*16^3+2*16^2+3*16^1+4*16^0)*2ms=9320ms$

And then, the capacitance can be calculated below:

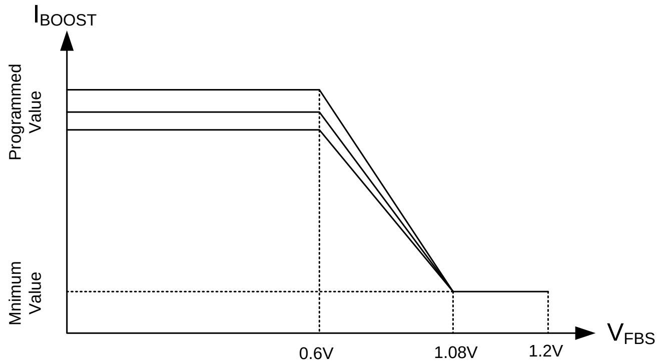
$C_{STR}=I_{DIS}*T_{DISCHARGE}/(V_{DIS1}-V_{DIS2})$





Adaptive Boost Peak Current Fold-back

If FBS voltage is lower than 0.6V, the programmed boost peak current is employed to shorten the STR charging time. As long as the FBS voltage is higher than 1.08V, the boost peak current starts to be fold back to the minimum value(600mA) softly to leave enough current limit margin for the load on BUS side.



If boost peak current is programmed lower than 800mA (300mA, 500mA or 600mA), HSFET will not be turned on in boost mode to reduce the negative inductor current. If boost peak current is programmed higher than 800mA there's negative inductor current because of the min on time of the high side MOSFET. The STR voltage could not be charged up to the programmed voltage level due to the negative inductor current. In order to charge the STR capacitors to desired value, it is recommended to set the boost peak current at a proper level. The maxim T_{MINON} value of HSFET is 160ns when boost peak current is programmed at 1.5A, 2A and 2.5A. The maxim T_{MINON} value of HSFET is 60ns when boost peak current is programmed at 800mA and 1A. The formula is presented below for proper boost peak current setting reference.

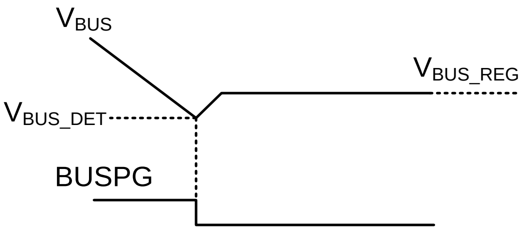
V_{STR}-V_{IN}=L dI / dT → dI=(V_{STR}-V_{IN})*dT / L=(V_{STR}-V_{IN})*T_{MINON} / L;

$I_{PEAK} \geqq dI / 2 \rightarrow I_{PEAK} \geqq (V_{STR}-V_{IN})*T_{MINON} / 2*L$;

Application Information

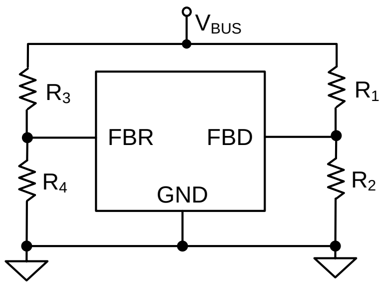
Feedback Resistor Dividers

Choose R_1 and R_2 to program proper BUS detection voltage V_{BUS_DET}. Choose R_3 and R_4 to program proper BUS regulation voltage V_{BUS_REG}. When BUS voltage falls to below V_{BUS_DET}, SYT664 enters buck mode and regulates the BUS voltage at V_{BUS_REG} as shown below. BUSPG is pulled low when SYT664 enters buck mode:



It is recommended to set the V_{BUS_DET} be lower than V_{BUS_REG}.

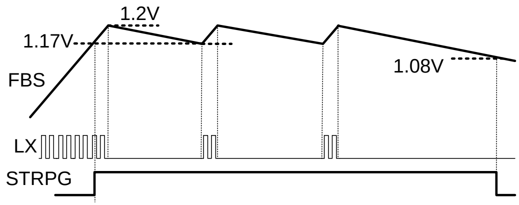
To minimize the power consumption under light load condition, it is recommended to choose relatively large resistance values for R_1, R_2, R_3 and R_4. A value of between 10kΩ and 1MΩ is more suitable for all resistors. If V_{BUS_DET} is programmed at 3.8V, R_1=250k is given, then using following equation, R_2 can be calculated to be 47k; If V_{BUS_REG} is programmed at 4.2V, R_3=250k is given, then using following equation, R_2 can be calculated to be 42k :



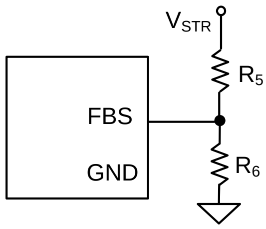
$$R_2 = \frac{0.6\,V}{V_{SYS\_DET} - 0.6\,V} R_1 .$$

$$R_4 = \frac{0.6\,V}{V_{SYS\_REG} - 0.6\,V} R_3$$

Choose R_5 and R_6 to program STR OVP level. Boost converter stops working when FBS voltage rises up to be higher than 1.2V and starts working again when FBS voltage falls below 1.17V. STRPG is pulled high when FBS voltage rises up to be higher than 1.17V and is pulled low when FBS voltage falls below 1.08V as shown below:



To minimize the power consumption, it is recommended to choose relatively large resistance values for R_5 and R_6 both. A value of between 10kΩ and 1MΩ is more suitable for both resistors. If V_{STR} OVP is programmed at 12V, R_5=400k is given, then using following equation, R_6 can be calculated to be 44k:



$$R_6 = \frac{1.2\,V}{V_{CSTR\_OVP} - 1.2\,V} R_5 .$$

Input Capacitor C_{IN}

To minimize the potential noise problem, place MLCC cap with X5R or a better grade really close to the IN and GND pins to decouple the high frequency noise. Be careful to minimize the loop size formed by C_{IN}, and IN/GND pins. A 0.1uF low ESR ceramic capacitor is recommended to minimum the input inrush current.

BUS Capacitor C_{BUS}

The BUS capacitor is the input capacitor of boost converter and also the output capacitor of buck converter. Both steady state ripple and transient requirements must be taken into account to select proper capacitor. For most applications, MLCC cap which has total capacitance greater than 66uF with X5R or better grade can work well. The real capacitance derating with DC voltage must be considered.

STR Capacitor C_{STR}

The STR capacitor is used to store energy and transfers it to BUS side when the power supply at input side is plugged out. BUS voltage can be hold for a long while if larger STR capacitance is used. The total capacitance is calculated below:

$$C_{STR} = \frac{2V_{BUS\_REG} \times I_{BUS} \times t_{HOLD}}{(V_{STR}{}^2 - V_{BUS\_REG}{}^2) \times \eta}$$

where C_{STR} is total capacitance of STR capacitors, V_{BUS_REG} is the programmed BUS regulation voltage, I_{BUS} is BUS load current, t_{HOLD} is desired BUS voltage hold time after IN is plug out, and V_{STR} is programmed STR OVP voltage. ŋ is the efficiency of the Buck regulator, choose ŋ =80% to leave enough margin.

Selection of Inductor L

Choose proper inductance to achieve the desired ripple current. If ripple current equals to 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where Fsw is the switching frequency; $I_{OUT,MAX}$ is the maximum BUS load current; V_{OUT} is programmed BUS output voltage and $V_{IN,MAX}$ is programmed STR OVP voltage.

External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSFET. A low ESR MLCC capacitor is connected between BST pin and LX pin.

When BST capacitor voltage slowly discharges during Boost converter in burst process, in order to enter buck mode successfully, its ended discharge voltage must be higher than BST capacitor UVLO threshold which can make sure HSFET driver has enough voltage.

The total discharge current on STR is around 320uA. The discharge voltage during boost burst mode is 0.025*Vstr. So the BST capacitor discharge time Tdis is:

Tdis = Cstr * 0.025 * Vstr / 320uA

The internal leakage current of SYT664 is lower than 100nA in high temp condition. Rp is the equivalent paralleled resistor of the BS cap. The leakage current of BS cap is 3.3V / Rp.

The maximum BST-LX voltage is around 3.3V and buck may fail when BST-LX voltage drop to 1.5V. So the maximum acceptable voltage drop during the discharge time is 3.3-1.5=1.8V.

The minimum BST capacitance needed is:

Cbst = (100nA + 3.3V/Rp) * Tdis / 1.8 = (100nA + 3.3V / Rp) * Cstr * 0.025 * Vstr / (1.8 * 320uA)

It is recommended to use X7R or above grade capacitance for better temperature tolerance and smaller leakage current. The DC derating of the capacitance should be taken into consideration.

Boost Inductor Peak Current Limit

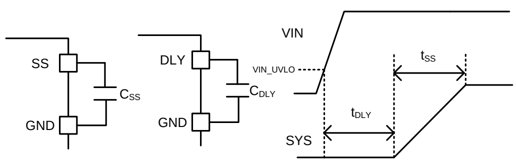
There's negative inductor current because of the min on time of the high side MOSFET when boost peak current is programmed higher than 800mA. The STR voltage could not be charged up to the programmed voltage level due to the negative inductor current. In order to charge the STR capacitors to desired value, it is recommended to set the boost peak current at a proper level. The maxim T_{MINON} value of HSFET is 160ns when boost peak current is programmed at 1.5A, 2A and 2.5A. The maxim T_{MINON} value of HSFET is 60ns when boost peak current is programmed at 800mA and 1A. The formula is presented below for proper boost peak current setting reference.

$V_{STR}-V_{IN}=L\ dI / dT \rightarrow dI=(V_{STR}-V_{IN})*dT / L=(V_{STR}-V_{IN})*T_{MINON} / L$;

$I_{PEAK} \geqq dI / 2 \rightarrow I_{PEAK} \geqq (V_{STR}-V_{IN})*T_{MINON} / 2*L$;

Delay Time and Soft-start Time Program

Connect a capacitor between DLY pin and GND to program the load switch turn on delay time. Connect a capacitor between SS pin and GND to program the load switch soft start time.



The turn on delay time calculation formula is shown below:

$$t_{DLY} = \begin{cases} t_{DLY\_DLT}, & \text{No external } C_{DLY} \\ \dfrac{C_{DLY}}{I_{INT\_DLY}}, & t_{DLY} > t_{DLY\_DLT} \end{cases},$$

Where, t_{DLY_DLT} is the internally fixed default soft-start time, about 1.4ms, which means there's no any external C_{DLY}; I_{INT_DLY} is the internal current source, about 3.6uA.

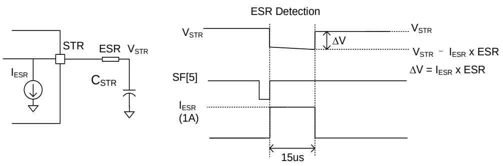
The soft start time calculation formula is shown as below:

$$t_{SS} = \begin{cases} t_{SS\_DLT}, & \text{No external } C_{SS} \\ \dfrac{C_{SS}}{I_{INT\_SS}}, & t_{SS} > t_{SS\_DLT} \end{cases},$$

Where, t_{SS_DLT} is the internally fixed default soft-start time, about 1ms, which means there's no any external C_{SS}; I_{INT_SS} is the internal current source, about 7.2uA.

<u>STR Capacitance Measurement and Abnormal ESR Detection</u>:

Storage capacitance measurement starts when a rising edge on SF[5] is detected. MCU can start measuring by setting SF[5] to 0 firstly and then setting SF[5] to 1. Firstly, the capacitor ESR detection starts and an internal 1A current source discharges STR for around 15us. At the end of discharging period, STR voltage with voltage drop on ESR is detected. After the discharge current is off, STR voltage without voltage drop on ESR is detected subsequently. If the difference between such two detected voltage values is higher than the programmed ESR detection threshold, ESR error is triggered and the last bit of ESR condition register (address 09H) will be set to 1.

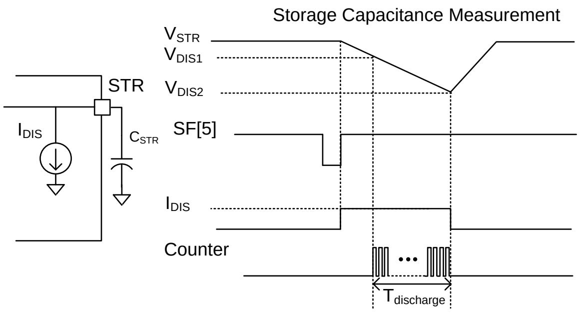


Programmed discharge current I_{DIS} starts to discharge STR capacitors after the ESR detection is finished. Internal 500Hz counter calculates the discharge time starting from when STR voltage falls below $V_{DIS1}$to when STR voltage falls below V_{DIS2}. The discharge time data $T_{DISCHARGE}$ is stored to data register REG07 and REG08. For example, if data read from REG07 is 0x12H, data read from REG08 is 0x34H, the $T_{DISCHARGE}$ should be calculated below:

$T_{DISCHARGE}$=0X1234H=$(1*16^3+2*16^2+3*16^1+4*16^0)*$ 2ms=9320ms

And then, the capacitance can be calculated below:

$C_{STR}=I_{DIS}*T_{DISCHARGE}/(V_{DIS1}-V_{DIS2})$



PCB Layout Recommendation

Put C_{IN}, C_{BUS}, C_{STR}, R_{FBR_D} as close as possible to the IC. Decouple C_{STR} to PGND. Decouple C_{VCC} to SGND.

Connect the SGND PIN and the PGND PIN together at a single point.

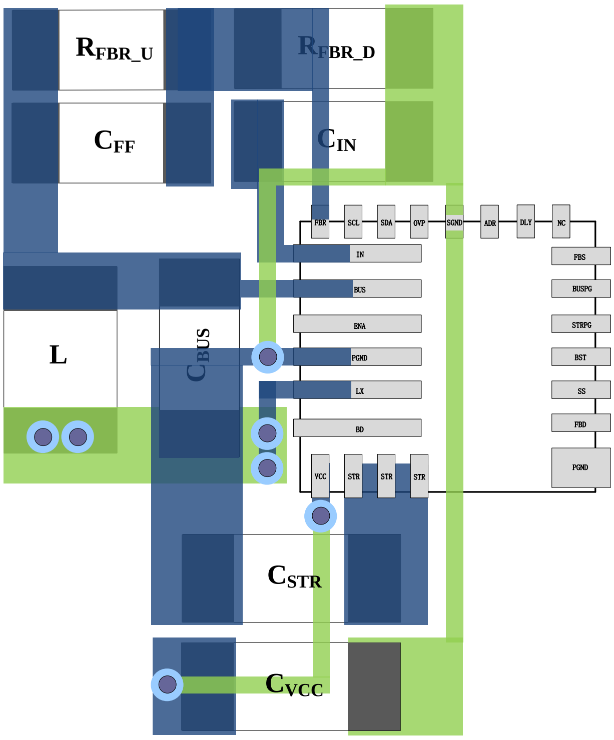
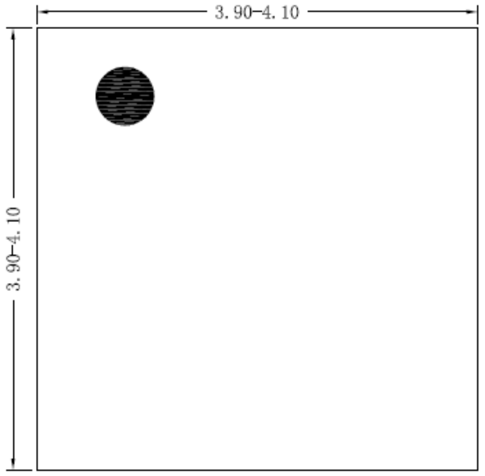
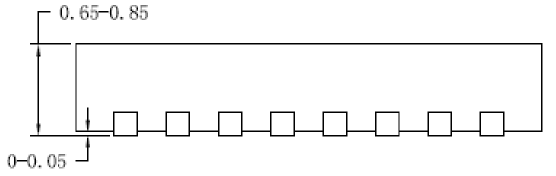


Figure4. PCB Layout Suggestion

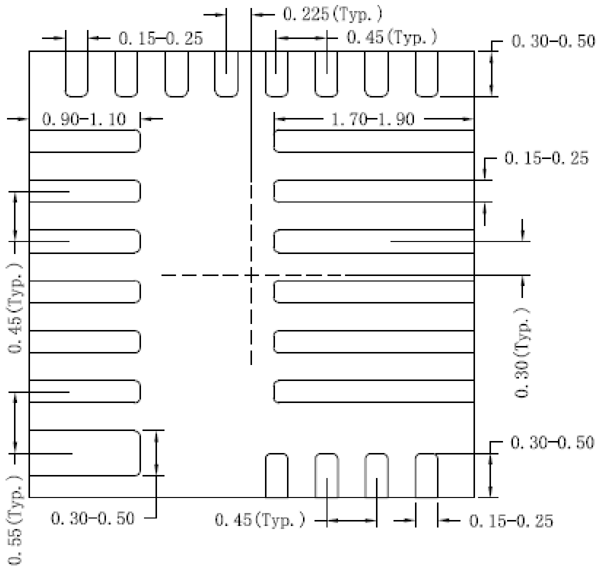
QFN4×4-25 Package Outline Drawing



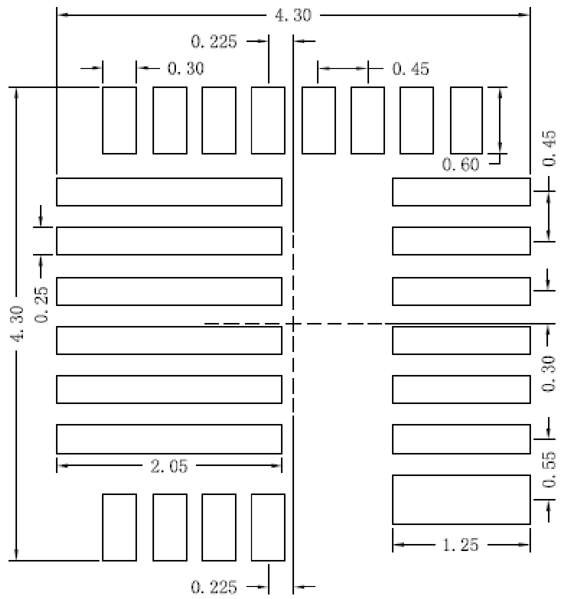
Top View



Side View



Bottom View

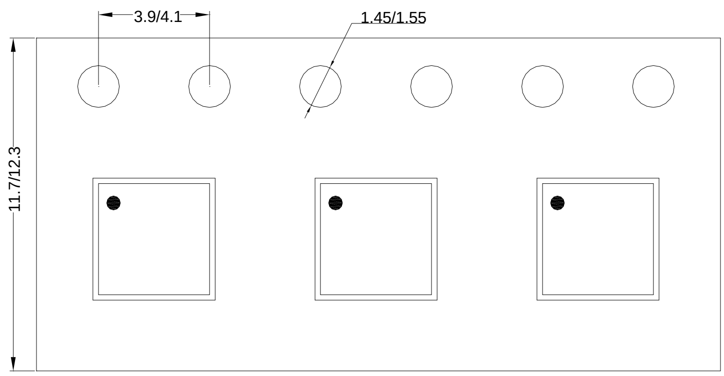


Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr**

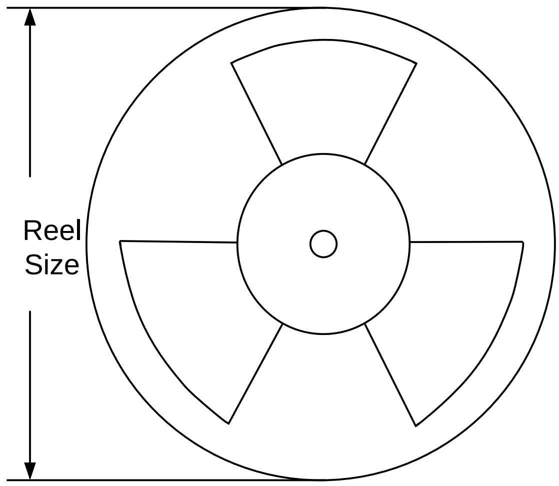
Taping & Reel Specification

1. QFN4×4 taping orientation



Feeding direction

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN4×4	12	8	13"	400	400	5000

3. Others: NA

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