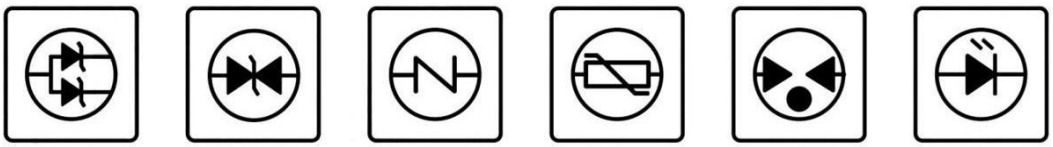
MSKSEMI 美森科
SEMICONDUCTOR



PTVSHC2EN4V5B-MS

Product specification

PTVSHC2EN4V5B-MS

Features

- 1200W Peak pulse power per line (tP = 8/20μs)
- DFN1610-2L package
- Response time is typically < 1 ns
- Protect one I/O or power line
- Low clamping Voltage
- RoHS compliant
- Transient protection for data lines to IEC 61000-4-2(ESD) ±30KV(air), ±30KV(contact); IEC 61000-4-4 (EFT) 40A (5/50ns)

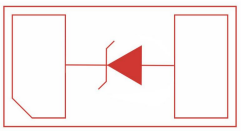
Mechanical Characteristics

- Lead finish:100% matte Sn(Tin)
- Mounting position: Any
- Qualified max reflow temperature:260℃
- Pure tin plating: 7 ~ 17 um
- Pin flatness：≤3mil

Applications

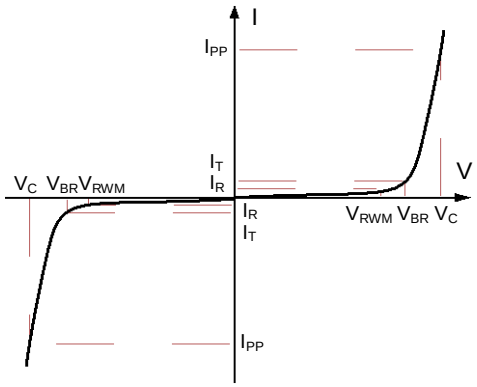
- Cell phone handsets and accessories
- Personal digital assistants (PDA's)
- Notebooks, desktops, and servers
- Portable instrumentation
- Cordless phones
- Digital cameras
- Peripherals
- MP3 players

Reference News

PACKAGE OUTLINE	Circuit Diagram	Marking
 DFN1610-2		D4N

Electronics Parameter

Symbol	Parameter
V_{RWM}	Peak Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
P_{PP}	Peak Pulse Power
C_J	Junction Capacitance



Electrical characteristics per line@25℃(unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Zener Voltage	V_Z	I_{ZT} = 5mA		5.1		V
Reverse Working Voltage(1)	V_{RWM}				4.5	V
Breakdown Voltage(PIN1~PIN2)	V_{BR}	I_t =1mA	4.6		6.1	V
Reverse Leakage Current(PIN1~PIN2)	I_R	V_{RWM} =4.5V			2	μA
Clamping Voltage(PIN1~PIN2)	V_C	I_{PP}=20A t_P = 8/20μs		6.5	8	V
Clamping Voltage(PIN1~PIN2)	V_C	I_{PP}=45A t_P = 8/20μs		7.5	9	V
Clamping Voltage(PIN1~PIN2)	V_C	I_{PP}=90A t_P = 8/20μs		9.5	12	V
Clamping Voltage(PIN1~PIN2)	V_C	I_{PP}=130A t_P = 8/20μs		10	13	V
Junction Capacitance	C_j	V_R=0V f = 1MHz		300	350	pF

Note 1: VRWM is the maximum reverse working voltage, or reverse stand-off voltage. ESD can protect signal line properly within its rated voltage. If the signal line's voltage is over VRWM, ESD will change to other state.

Absolute maximum rating@25℃

Rating	Symbol	Value	Units
Peak Pulse Power (t_P = 8/20μS)	P_{pp}	1200	W
Total Device Dissipation FR-5 Board	P_D	500	mW
Lead Soldering Temperature	T_L	260 (10 sec)	℃
Operating Temperature	T_J	-55 to +150	℃
Storage Temperature	T_{STG}	-55 to +150	℃

Typical Characteristics

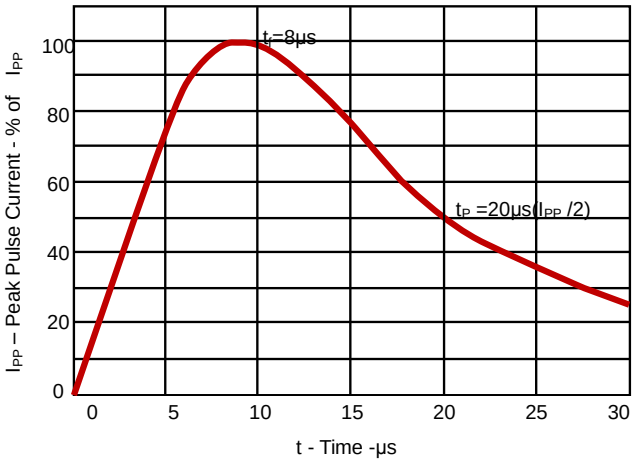


Fig 1.Pulse Waveform

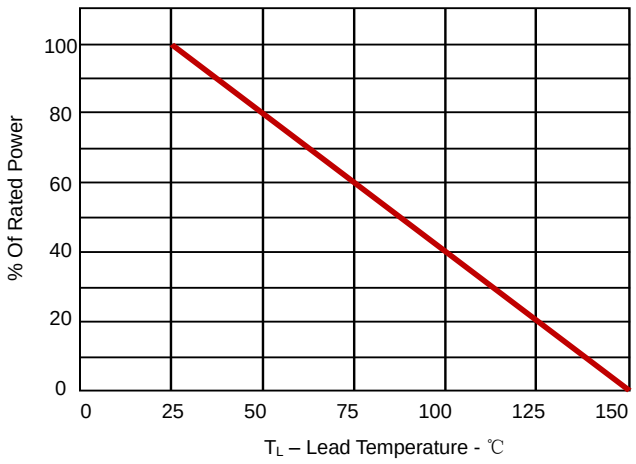


Fig 2.Power Derating Curve

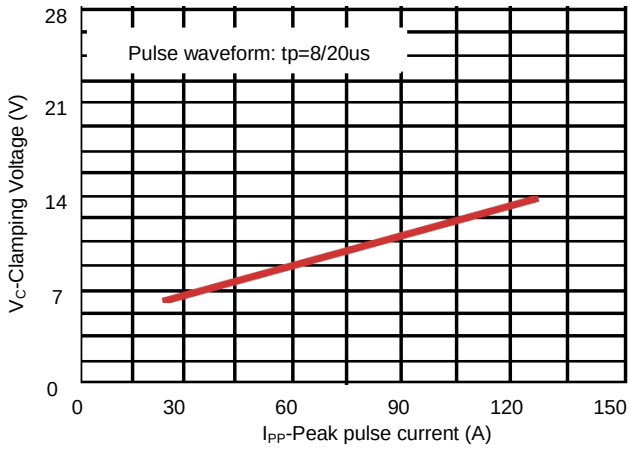


Fig 3. Clamping voltage vs. Peak pulse current

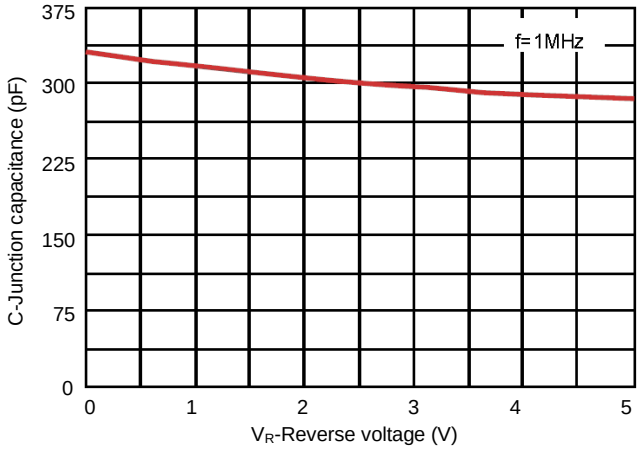


Fig 4. Capacitance vs. Reveres voltage

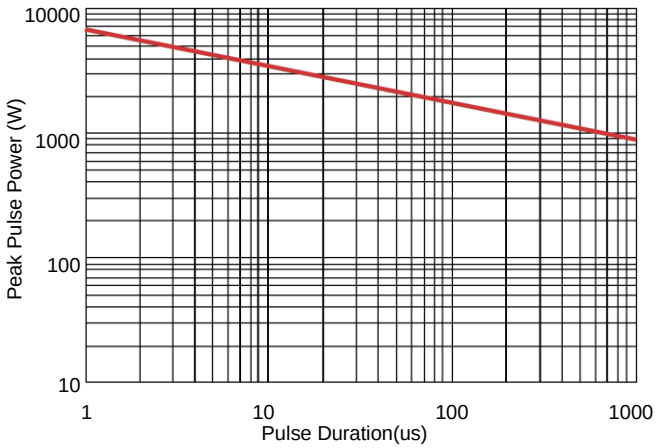
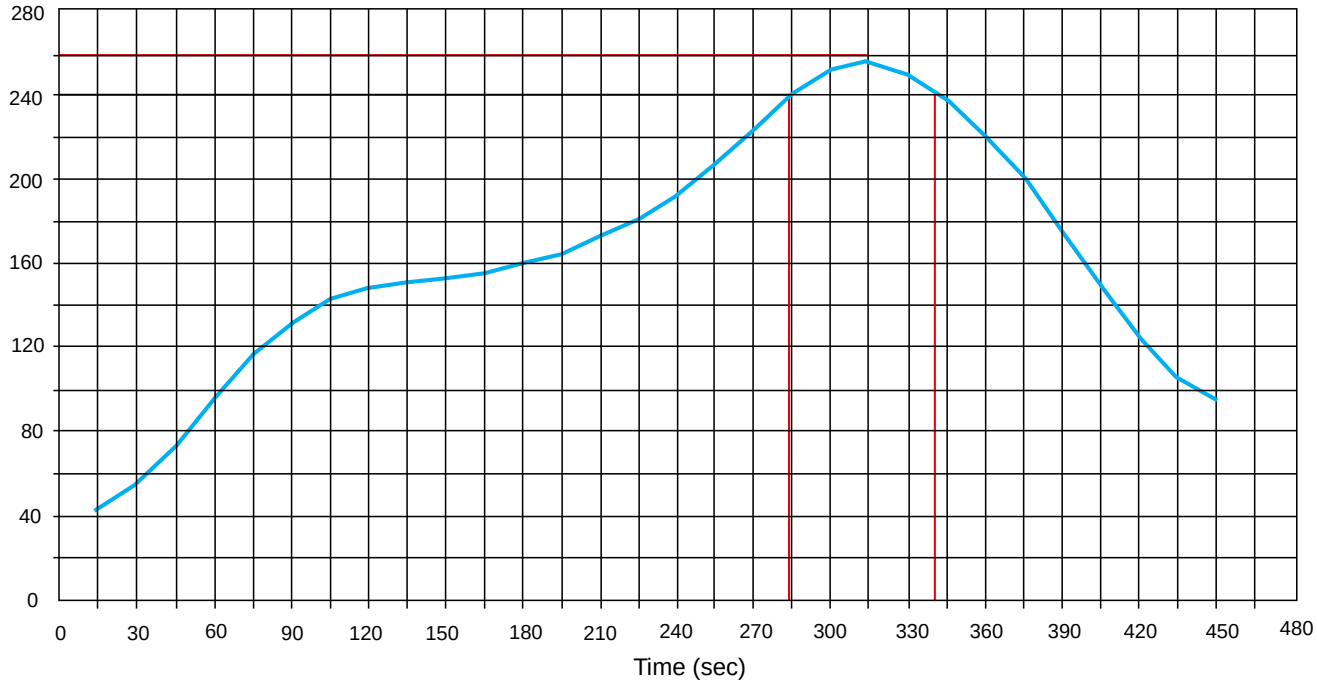


Fig 5. Non Repetitive Peak Pulse Power vs. Pulse time

Solder Reflow Recommendation

Peak Temp=257℃, Ramp Rate=0.802deg. ℃/sec

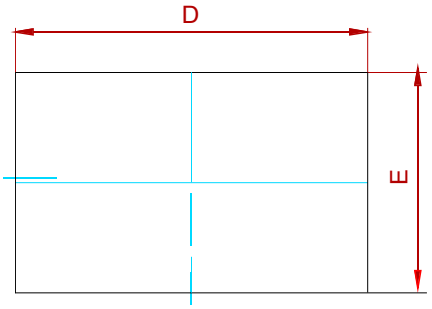


PCB Design

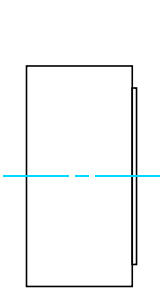
For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

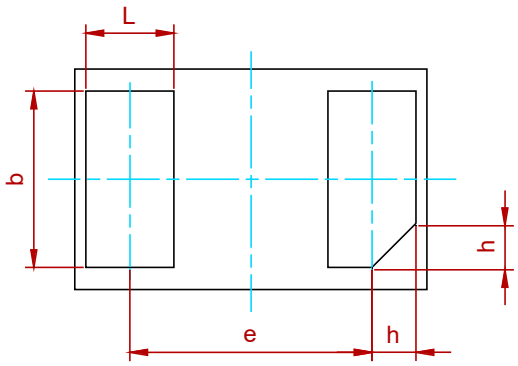
- Do not use stubs, but place the cathode of the TVS diode directly on the signal trace.
- Do not make false economies and save copper for the ground connection.
- Place via holes to ground as close as possible to the anode of the TVS diode.
- Use as many via holes as possible for the ground connection.
- Keep the length of via holes in mind! The longer the more inductance they will have.

PACKAGE MECHANICAL DATA

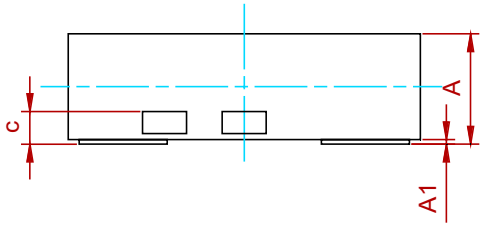


TOP VIEW





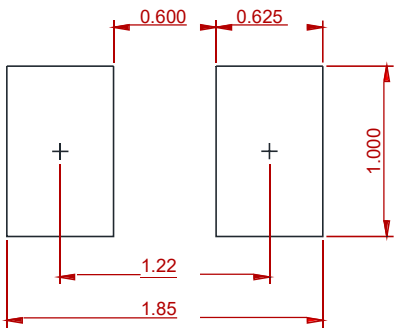
BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
c	0.15 Ref.		
b	0.75	0.80	0.85
L	0.35	0.40	0.45
D	1.55	1.60	1.65
E	0.95	1.00	1.05
e	1.10 BSC		
h	0.20 Ref.		

Recommend PCB Layout (Unit: mm)



Notes:
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

REEL SPECIFICATION

P/N	PKG	QTY
PTVSHC2EN4V5B-MS	DFN1610-2	3000

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