

MSKSEMI 美森科

SEMICONDUCTOR



ESD



TVS



TSS



MOV



GDT



PLED

PTVSHC2EN7VU-MS

Product specification

Features

- 1400W Peak pulse power per line (tP = 8/20μs)
- DFN1610-2L package
- Response time is typically < 1 ns
- Protect one I/O or power line
- Low clamping Voltage
- RoHS compliant
- Transient protection for data lines to IEC 61000-4-2(ESD)±30KV(air), ±30KV(contact); IEC 61000-4-4 (EFT) 40A (5/50ns)


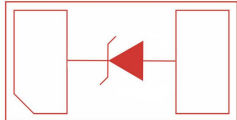

Mechanical Characteristics

- Lead finish:100% matte Sn(Tin)
- Mounting position: Any
- Qualified max reflow temperature:260°C
- Pure tin plating: 7 ~ 17 um
- Pin flatness:≤3mil

Applications

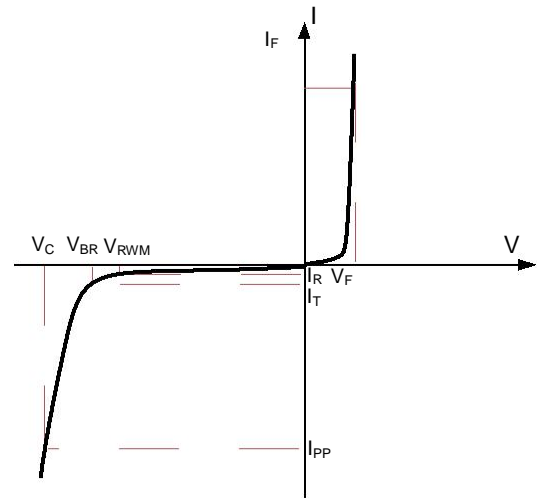
- Cell phone handsets and accessories
- Personal digital assistants (PDA's)
- Notebooks, desktops, and servers
- Portable instrumentation
- Cordless phones
- Digital cameras
- Peripherals
- MP3 players

Reference News

PACKAGE OUTLINE	Circuit Diagram	Marking
 <p data-bbox="301 1529 448 1559">DFN1610-2</p>		

Electronics Parameter

Symbol	Parameter
V_{RWM}	Peak Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
P_{PP}	Peak Pulse Power
C_J	Junction Capacitance
I_F	Forward Current
V_F	Forward Voltage @ I_F



Electrical characteristics per line@25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Peak Reverse Working Voltage	V_{RWM}				7	V
Breakdown Voltage	V_{BR}	$I_T = 1\text{mA}$		8	9.5	V
Reverse Leakage Current	I_R	$V_{RWM} = 7\text{V}$			1	μA
Clamping Voltage	V_C	$I_{PP} = 70\text{A}$ $t_P = 8/20\mu\text{s}$		20	24	V
Junction Capacitance	C_j	$V_R = 0\text{V}$ $f = 1\text{MHz}$	500	550	650	pF

Absolute maximum rating@25°C

Rating	Symbol	Value	Units
Peak Pulse Power ($t_P = 8/20\mu\text{s}$)	P_{pp}	1400	W
Lead Soldering Temperature	T_L	260 (10 sec)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Typical Characteristics

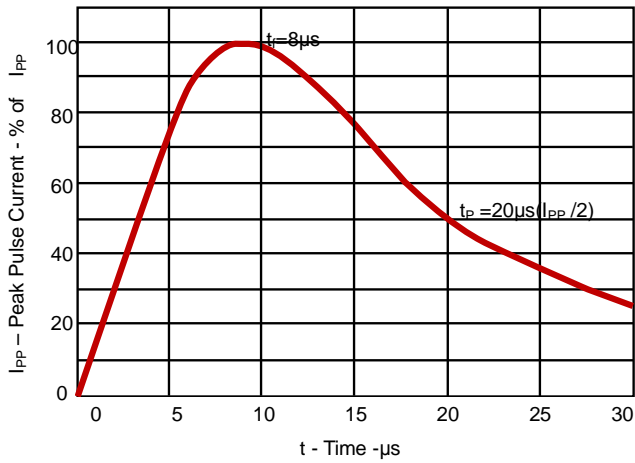


Fig 1. Pulse Waveform

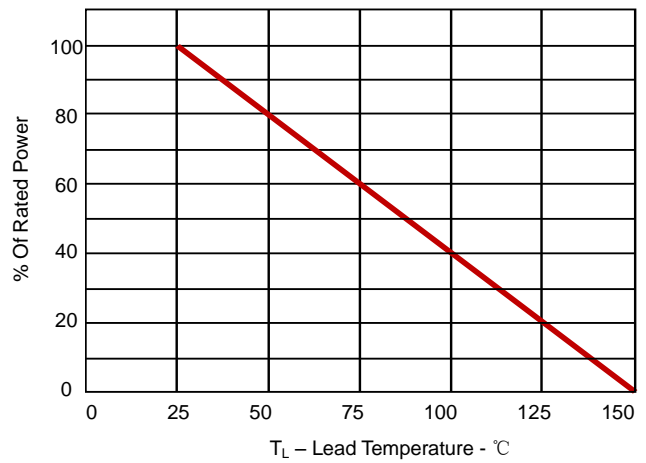


Fig 2. Power Derating Curve

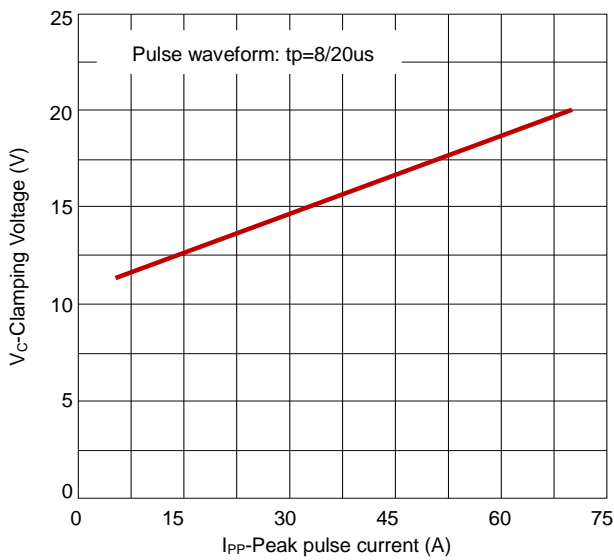


Fig 3. Clamping voltage vs. Peak pulse current

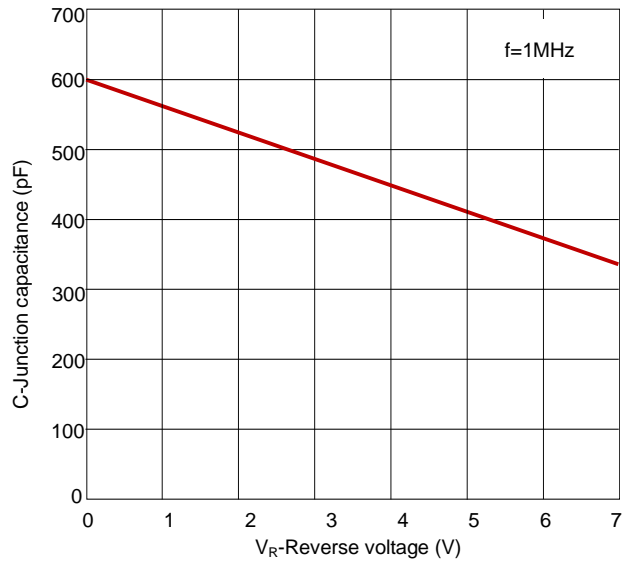


Fig 4. Capacitance vs. Reverse voltage

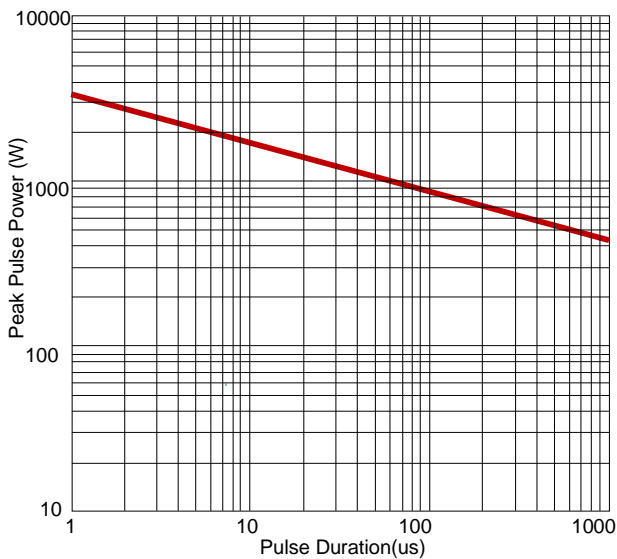
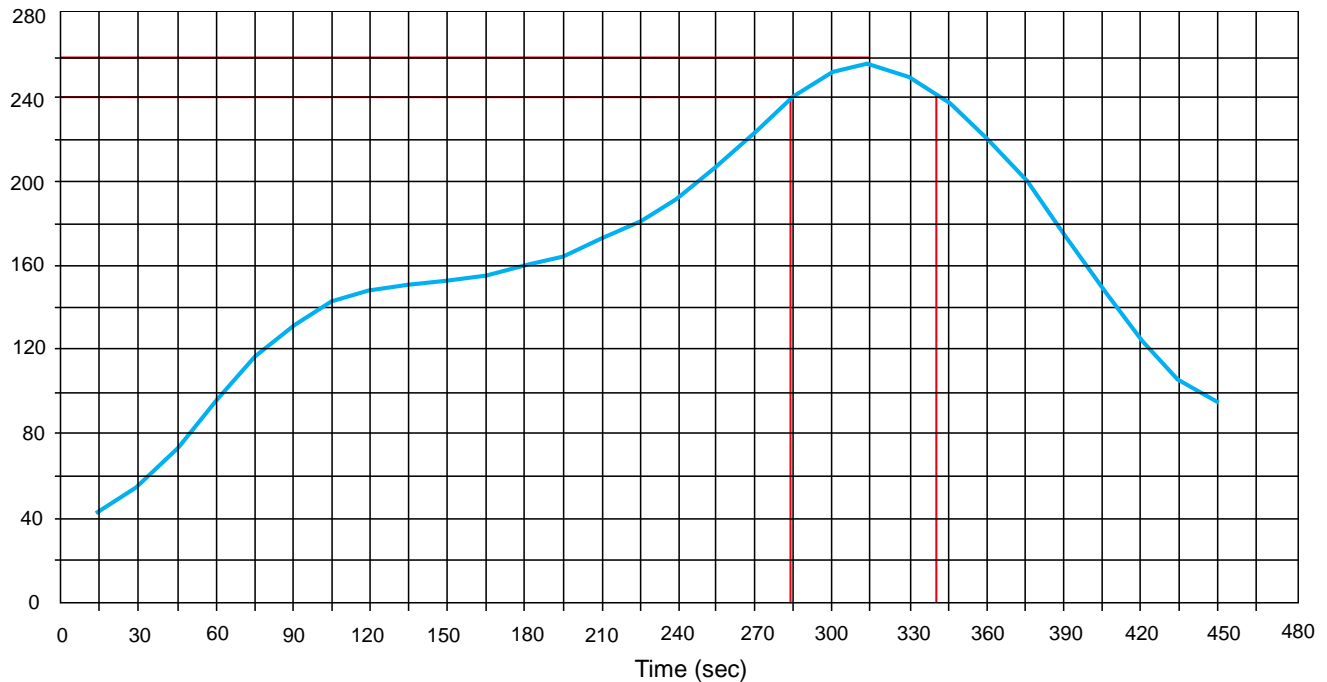


Fig 5. Non Repetitive Peak Pulse Power vs. Pulse time

Solder Reflow Recommendation

Peak Temp=257°C, Ramp Rate=0.802deg. °C/sec

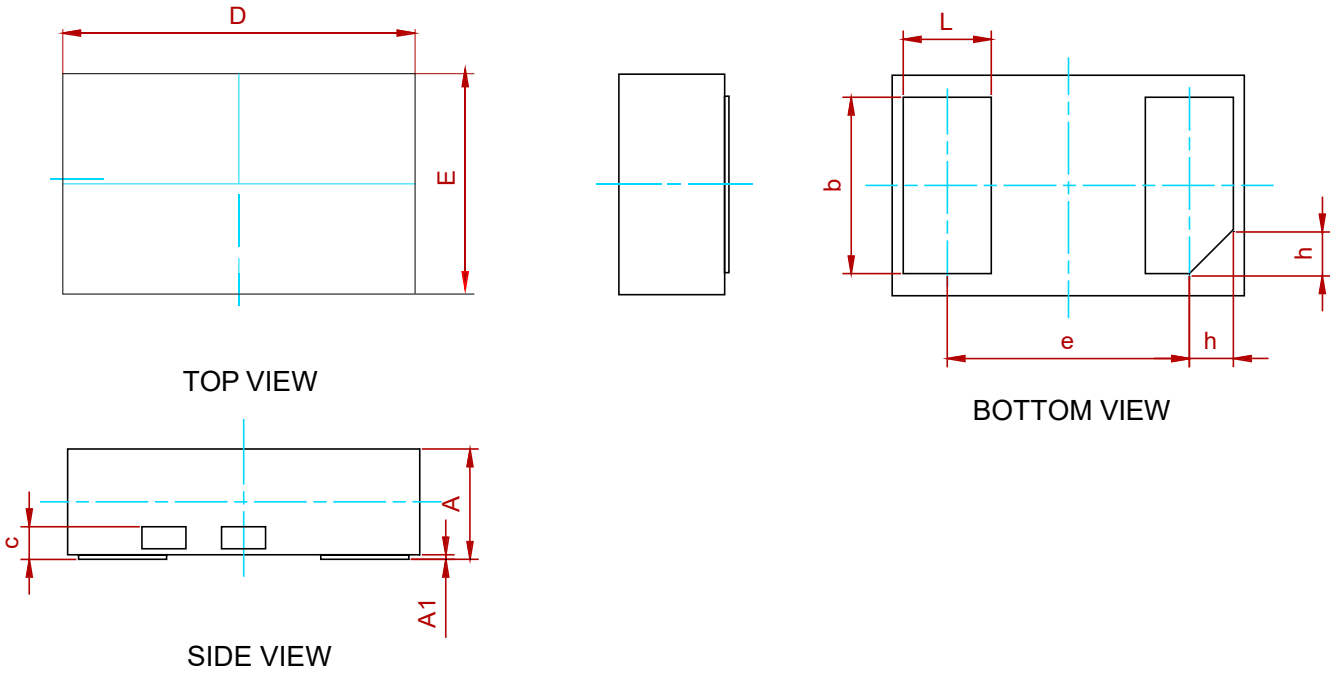


PCB Design

For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

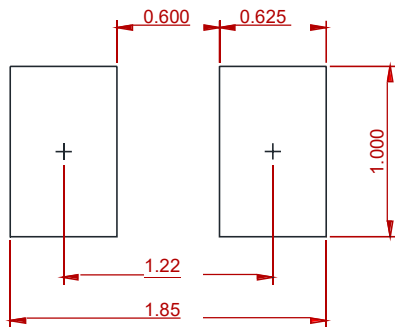
- Do not use stubs, but place the cathode of the TVS diode directly on the signal trace.
- Do not make false economies and save copper for the ground connection.
- Place via holes to ground as close as possible to the anode of the TVS diode.
- Use as many via holes as possible for the ground connection.
- Keep the length of via holes in mind! The longer the more inductance they will have.

PACKAGE MECHANICAL DATA



Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
c	0.15 Ref.		
b	0.75	0.80	0.85
L	0.35	0.40	0.45
D	1.55	1.60	1.65
E	0.95	1.00	1.05
e	1.10 BSC		
h	0.20 Ref.		

Recommend PCB Layout (Unit: mm)



Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

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