XL8574, XL8574A

Remote 8-bit I/O expander for I²C-Bus with interrupt

Rev. 2.1 — 2017

1. DESCRIPTION

This device (XL8574 or XL8574A) provides general-purpose remote I/O expansion via the two-wire bidirectional I²C-bus interface [serial clock line (SCL), serial data line (SDA)].

The devices consist of eight quasi-bidirectional ports, 100kHz I²C-bus interface, three hardware address inputs and interrupt output operating between 2.5V and 6.0V. The quasi-bidirectional port can be independently assigned as an input to monitor interrupt status or keypads, or as an output to activate indicator devices such as LEDs. System master can read from the input port or write to the output port through a single register.

The low current consumption of 2.5μA (typical, static) is great for mobile applications and the latched output ports directly drive LEDs.

The XL8574 and XL8574A are identical, except for the different fixed portion of the slave address. The 3 hardware address pins (A0, A1 and A2) allow eight of each device to be on the same I²C-bus, so there can be up to 16 of these I/O expanders XL8574/8574A together on the same I²C-bus, supporting up to 128 I/Os (for example, 128 LEDs).

The active LOW open-drain interrupt output ($\overline{INT}$) can be connected to the interrupt logic of the MCU and is activated when any input state differs from its corresponding input port register state. It is used to indicate to the MCU that an input state has changed and the device needs to be interrogated without the MCU continuously polling the input register via the I²C-bus.

The internal Power-On Reset (POR) initializes the I/Os as inputs with a weak internal pull-up 100μA current source, the I/Os are HIGH logic levels.

2. FEATURES

- I²C-bus to parallel port expander
- 100kHz I²C-bus clock frequency (Standard-mode I²C-bus)
- Operating power supply voltage 2.5V to 6.0V with non-overvoltage tolerant I/O held to VCC with 100μA current source
- Low standby current (2.5μA typical)
- 8-bit remote I/O pins that default to inputs at power-up
- Latched outputs directly drive LEDs
- Total package sink capability of 80mA
- Open-drain active LOW interrupt output
- Address by 3 hardware address pins for use of up to 8 devices
- -40°C to +85°C operation
- Packages offered: DIP16, SO16W, SSOP20
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100mA
- ESD protection exceeds JESD 22 2000V HBM, 200V MM and 1000V CDM

3. APPLICATIONS

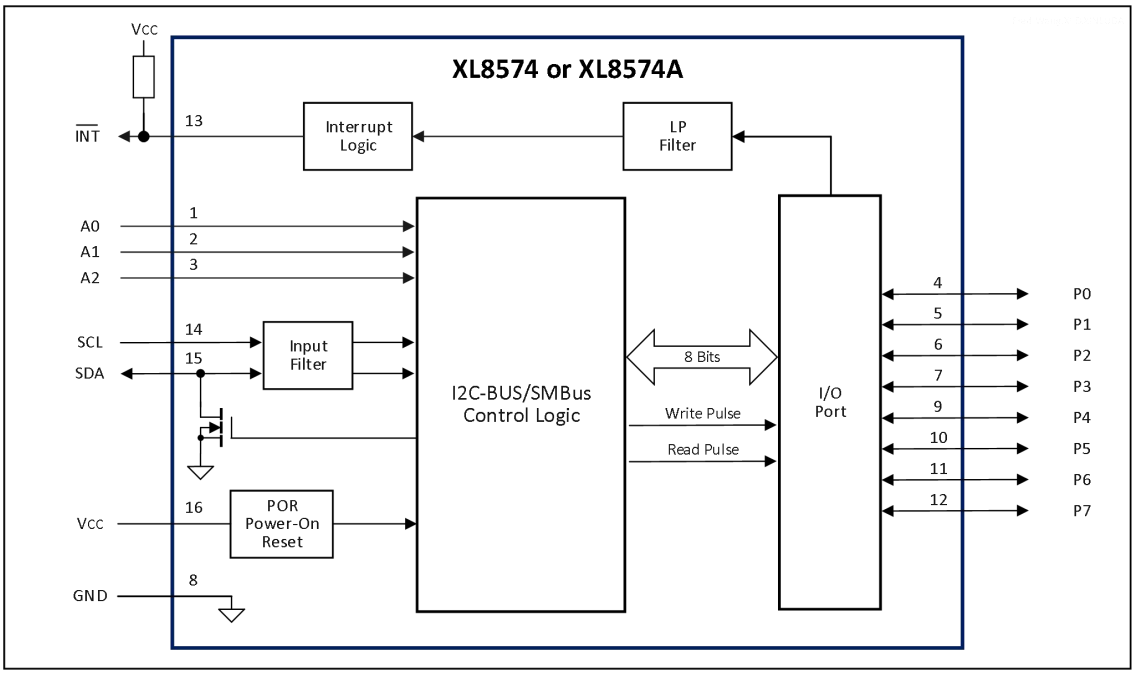
- LED signs and displays
- Servers
- Key pads
- Industrial control
- Medical equipment
- PLC
- Cellular telephones
- Personal electronics
- Mobile devices
- Gaming machines
- Instrumentation and test measurement
- Products with GPIO-Limited processors

4. ORDERING INFORMATION

Table 1. Ordering Information

Part Number	Topside Marking	Package Type	Body size (mm)	Lead pitch (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XD8574P	XD8574P	DIP16(300mil)	19.05 × 6.35	2.54	-40 to +85	MSL3	Tube	1000
XL8574TM	XL8574TM	SOP16(150mil)	10.00 × 3.90	1.27	-40 to +85	MSL3	T&R 13"	2500
XL8574T	XL8574T	SOP16W(300mil)	10.20 × 7.50	1.27	-40 to +85	MSL3	T&R 13"	1000
XL8574TS	XL8574TS	SSOP20(173mil)	6.50 × 4.40	0.65	-40 to +85	MSL3	T&R 13"	2000
XD8574AP	XD8574AP	DIP16(300mil)	19.05 × 6.35	2.54	-40 to +85	MSL3	Tube	1000
XL8574ATM	XL8574ATM	SOP16(150mil)	10.00 × 3.90	1.27	-40 to +85	MSL3	T&R 13"	2500
XL8574AT	XL8574AT	SOP16W(300mil)	10.20 × 7.50	1.27	-40 to +85	MSL3	T&R 13"	1000
XL8574ATS	XL8574ATS	SSOP20(173mil)	6.50 × 4.40	0.65	-40 to +85	MSL3	T&R 13"	2000

5. FUNCTIONAL BLOCK DIAGRAM



REMARK: (1) All I/Os are set to inputs at reset.

(2) Pin numbers shown are for the DIP16, SOP16 and SOP16W packages.

Figure 1. Block Diagram

6. PIN CONFIGURATIONS AND FUNCTIONS

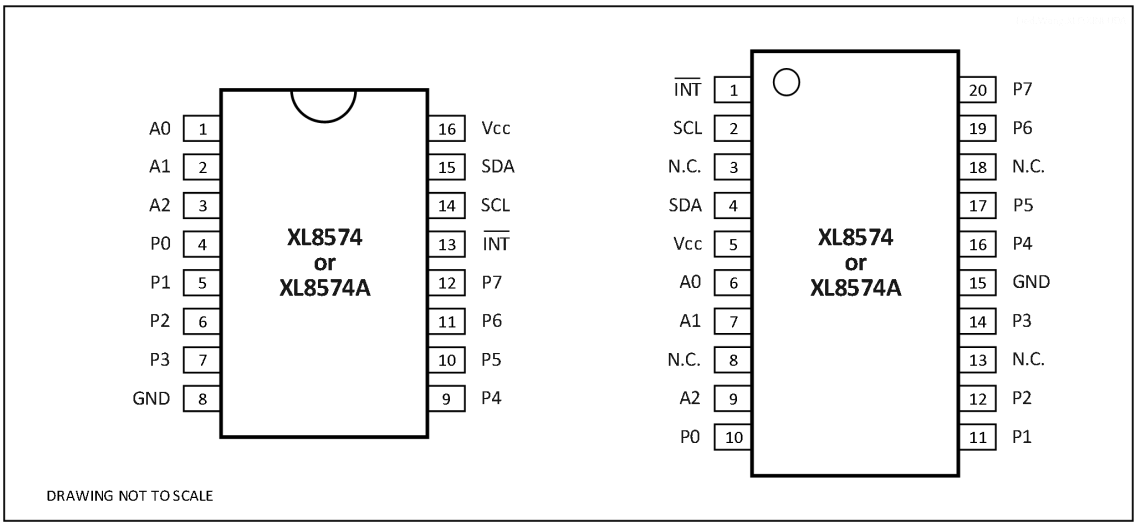


Figure 2. Pin configuration for DIP16/SOP16/SOP16W (TOP VIEW)

Figure 3. Pin configuration for SSOP20 (TOP VIEW)

Table 2. Pin Functions

PIN NAME	PIN NUMBER		PIN TYPE	DESCRIPTION
	DIP16/SOP16/SOP16W	SSOP20		
A0, A1, A2	1, 2, 3	6, 7, 9	I	Address input 0 through 2. Connect directly to V_{CC} or ground. Pull-up resistors are not needed.
P0	4	10	I/O	Port input/output. Push-pull design structure. At power on, P0-P7 are configured as an input.
P1	5	11	I/O	
P2	6	12	I/O	
P3	7	14	I/O	
P4	9	16	I/O	
P5	10	17	I/O	
P6	11	19	I/O	
P7	12	20	I/O	
GND	8	15	–	Supply ground.
$\overline{INT}$	13	1	O	Interrupt output (active LOW). Open-drain design structure. Connect to V_{CC} through a pull-up resistor.
SCL	14	2	I	Serial clock line. Connect to V_{CC} through a pull-up resistor.
SDA	15	4	I/O	Serial data line. Connect to V_{CC} through a pull-up resistor.
V_{CC}	16	5	–	Supply voltage.
N.C.	–	3,8,13,18	–	Not connected.

7. SPECIFICATIONS

7.1. Absolute Maximum Ratings [1]

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	+7	V
V_{IN}	Input pin voltage range [2]		-0.5	Vcc+0.5	V
V_O	Output pin voltage range [2]		-0.5	Vcc+0.5	V
I_{IK}	Input clamp current	V_{IN}<0	–	-20	mA
I_{OK}	Output clamp current	V_O<0	–	-20	mA
I_{IOK}	Input/output clamp current	V_O<0 or V_O>V_{CC}	–	±400	μA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}	–	+50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}	–	-4	mA
I_{CC}	Continuous current through GND		–	-100	mA
	Continuous current through V_{CC}		–	+100	mA
P_{tot}	Total Power Dissipation		–	400	mW
T_{stg}	Storage temperature range		-65	+150	°C
T_{amb}	Ambient temperature range	Operating	-40	+85	°C
MSL	Moisture Sensitivity		–	Level 3	–

[1] Stresses exceeding those listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2. Thermal Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS (PACKAGE)				UNIT
		DIP16	SOP16	SOP16W	SSOP20	
$R_{\theta JA}$	Package thermal resistance, Junction-to -ambient (free air) [3]	48.3	79.7	79.7	112.2	°C/W

[3] Measured with minimum pad spacing on an FR4 PCB board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.

7.3. ESD Ratings

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{ESD}	Electrostatic Discharge	Human Body Mode (HBM), all pins [4]	0	2000	V
		Charged Device Model (MM), all pins [5]	0	200	V
		Charged Device Model (CDM), all pins [6]	0	1000	V

[4] Tested to EIA/JESD22−A114−A.

[5] Tested to EIA/JESD22−A115−A.

[6] Tested to JESD22−C101−A.

7.4. Recommended Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	$V_{CC(MAX)}$ = 5.5V	+2.3	+5.5	V

V_{IH}	High-level input voltage	SCL, SDA	0.7×V_{CC}	V_{CC}	V
		A2–A0, P7–P0	0.7×V_{CC}	V_{CC}	V
V_{IL}	Low-level input voltage	SCL, SDA	-0.5	0.3×V_{CC}	V
		A2–A0, P7–P0	-0.5	0.3×V_{CC}	V
I_{OH}	High-level output current	P7–P0	–	-1	mA
I_{OL}	Low-level output current	P7–P0	–	+25	mA
T_A	Operating free-air temperature		-40	+85	°C

7.5. Electrical Characteristics

V_{CC} = +2.3V to +5.5V; GND = 0 V; T_A = free-air temperature range; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Power Supplies							
I_{CC}	Supply Current, in operating mode	I/O = inputs, V_{IN} = V_{CC} or GND, f_{SCL} = 100 kHz, I_O = 0, No load;	+5.5V	–	40	100	µA
I_{STB}	Standby Current, in standby mode	I/O = inputs, V_{IN} = V_{CC} or GND, f_{SCL} = 0 kHz, I_O = 0, No load;	+5.5V	–	2.5	10	µA
V_{POR}	Power-on reset voltage, V_{CC} rising [7]	V_{IN} = V_{CC} or GND, I_O = 0, No load;	+5.5V	–	1.3	2.4	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage		2.3V to 5.5V	-0.5	–	+0.3×V_{CC}	V
V_{IH}	HIGH-level input voltage		2.3V to 5.5V	0.7×V_{CC}	–	V_{CC}+0.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	2.3V to 5.5V	3	–	–	mA
I_L	leakage current	V_{IN} = V_{CC} or GND	2.3V to 5.5V	-1	–	+1	µA
C_I	input capacitance	V_{IN} = GND	2.3V to 5.5V	–	3	7	pF
I/Os; P0 to P7							
V_{IL}	LOW-level input voltage		2.3V to 5.5V	-0.5	–	+0.3×V_{CC}	V
V_{IH}	HIGH-level input voltage		2.3V to 5.5V	0.7×V_{CC}	–	V_{CC}+0.5	V
I_{OL}	LOW-level output current [8]	V_{OL} = 1.0V	+5.5V	10	25	–	mA
I_{OH}	HIGH-level output current [9]	V_{OH} = GND	+5.5V	30	–	300	µA
I_{LIH}	HIGH-level input leakage current	V_{IN} = V_{CC}	2.3V to 5.5V	–	–	+5	µA
I_{LIL}	LOW-level input leakage current	V_{IN} = GND	2.3V to 5.5V	–	–	-5	µA
C_I	input capacitance		2.3V to 5.5V	–	4	10	pF
C_O	output capacitance		2.3V to 5.5V	–	4	10	pF
Interrupt ($\overline{INT}$)							
I_{OL}	LOW-level output current	V_{OL} = 0.4V	2.3V to 5.5V	1.6	–	–	mA
I_{LIH}	HIGH-level input leakage current	V_{IN} = V_{CC}	2.3V to 5.5V	–	–	+5	µA
I_{LIL}	LOW-level input leakage current	V_{IN} = GND	2.3V to 5.5V	–	–	-5	µA
Address select inputs A0, A1, A2							
V_{IL}	LOW-level input voltage		2.3V to 5.5V	-0.5	–	+0.3×V_{CC}	V
V_{IH}	HIGH-level input voltage		2.3V to 5.5V	0.7×V_{CC}	–	V_{CC}+0.5	V
I_{LIH}	HIGH-level input leakage current	V_{IN} = V_{CC}	2.3V to 5.5V	–	–	+5	µA
I_{LIL}	LOW-level input leakage current	V_{IN} = GND	2.3V to 5.5V	–	–	-5	µA

[7] The power-on reset circuit resets the I^2C-bus logic with V_{CC} < V_{POR} and sets all I/Os to logic high (with current source to V_{CC}).

[8] The current sinked by each I/O must be externally limited to 25 mA, and a device total current must be limited to a maximum current of 80mA.

[9] The current sourced by each I/O must be limited to 1mA.

7.6. Dynamic Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

SYMBOL	PARAMETER	TEST CONDITIONS	Standard-mode			UNIT
			MIN	TYP	MAX	
I²C-bus Interface Timing						
f_{SCL}	I²C-bus SCL Clock frequency		0	–	100	kHz
t_{BUF}	I²C-bus free time between a STOP and START Condition		4.7	–	–	µs
$t_{HD:STA}$	Hold Time (Repeated) START Condition		4.0	–	–	µs
$t_{SU:STA}$	Set-up Time for a Repeated START Condition		4.7	–	–	µs
$t_{SU:STO}$	Set-up Time for STOP Condition		4.0	–	–	µs
$t_{VD:ACK}$	Data Valid Acknowledge Time [10]		0	–	3.4	µs
$t_{HD:DAT}$	Data Hold Time		0	–	–	ns
$t_{VD:DAT}$	Data Valid Time [11]		0	–	3.4	µs
$t_{SU:DAT}$	Data Set-up Time		250	–	–	ns
t_{LOW}	LOW period of the SCL clock		4.7	–	–	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	–	–	µs
t_f	Fall Time of both SDA and SCL signals [12, 13]		–	–	0.3	µs
t_r	Rise Time of both SDA and SCL signals		–	–	1	µs
t_{sp}	Pulse Width of Spikes that must be Suppressed by the Input Filter [17]		–	–	50	ns
C_b	I²C-bus capacitive load [14]		–	–	400	pF
Port timing						
$t_{pv(Q)}$	Output data valid time [18]	$C_L \leq 100pF$	–	–	4	µs
$t_{ps(D)}$	Input data set-up time	$C_L \leq 100pF$	0	–	–	µs
$t_{ph(D)}$	Input data hold time	$C_L \leq 100pF$	4	–	–	µs
Interrupt ($\overline{INT}$) timing						
$t_{iv(INT\_N)}$	Interrupt valid time, on pin $\overline{INT}$	from port to $\overline{INT}$; $C_L \leq 100pF$	–	–	4	µs
$t_{irst(INT\_N)}$	Interrupt reset delay time, on pin $\overline{INT}$	from SCL to $\overline{INT}$; $C_L \leq 100pF$	–	–	4	µs

[10] $t_{VD:ACK}$ = time for Acknowledgment signal from SCL LOW to SDA (out) LOW.

[11] $t_{VD:DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[12] A master device must internally provide a hold time of at least 300ns for the SDA signal (refer to V_{IL} of the SCL signal) in order to bridge the undefined region SCL's falling edge.

[13] The maximum t_f for the SDA and SCL bus lines is specified at 300ns. The maximum fall time for the SDA output stage t_f is specified at 250ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.

[14] C_b = total capacitance of one bus line in pF.

[15] Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

[16] $t_{pv(Q)}$ measured from $0.7 \times V_{CC}$ on SCL to 50 % I/O output.(see Figure 6)

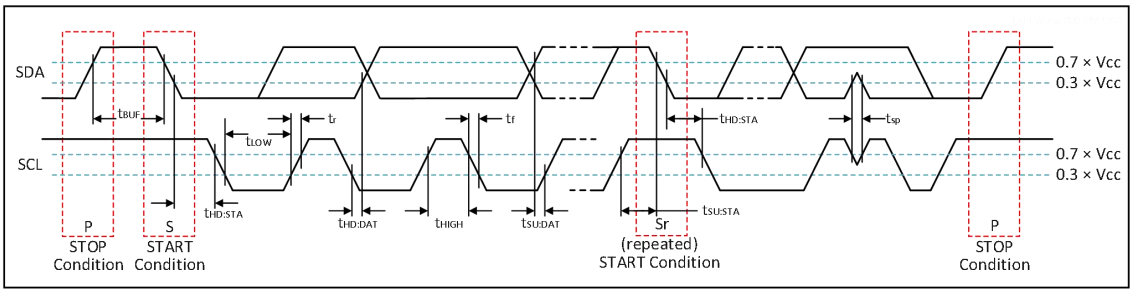


Figure 4. Definition of timing on the I²C-bus

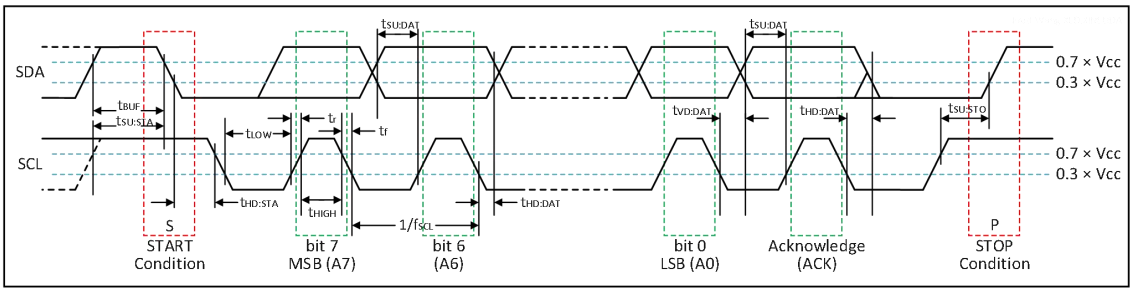


Figure 5. I²C-bus timing diagram

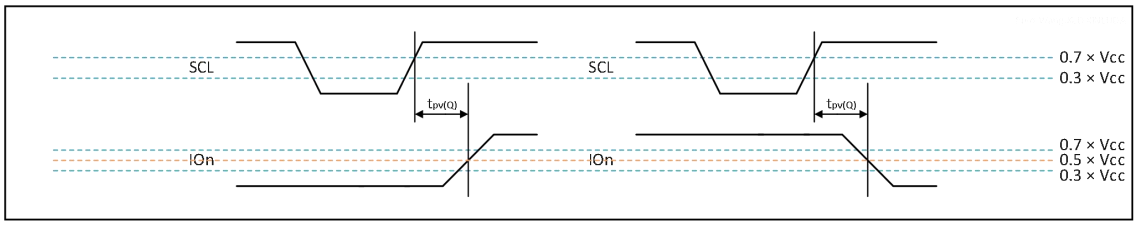
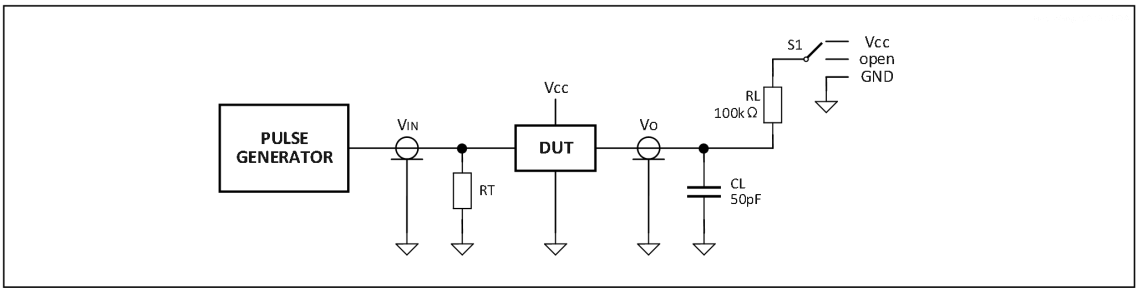


Figure 6. $t_{pv(Q)}$ timing

8. TEST INFORMATION



REMARK: R_L = load resistor.

C_L = load capacitance includes jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance of Zo of the pulse generators.

Figure 7. Test circuitry for switching times

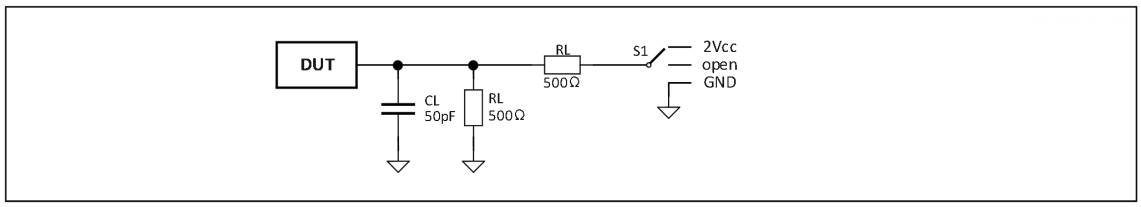


Figure 8. Load circuit

9. CHARACTERISTICS OF THE I²C-BUS INTERFACE

The bidirectional I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

9.1. Bit Transfer

On the I²C-bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as control signals (see Figure 9).

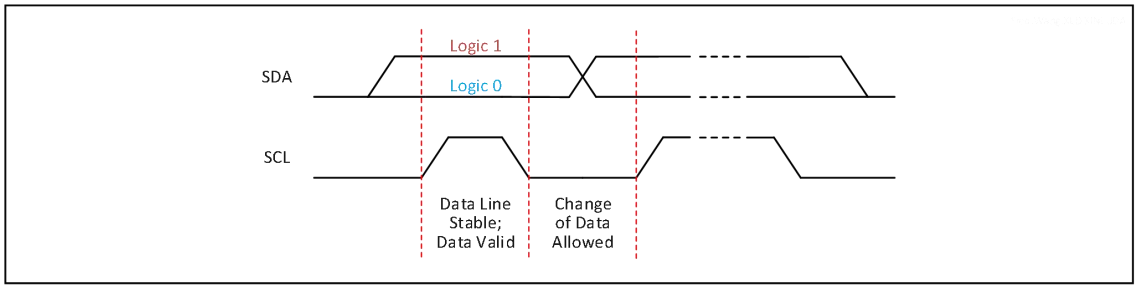


Figure 9. Bit Transfer

9.2. START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. I²C communication with this device is initiated by a master sending a START condition (S). A HIGH-to-LOW transition of the SDA data line input/output while the SCL clock is HIGH is defined as the START condition. A LOW-to-HIGH transition of the SDA data line input/output while the SCL clock is HIGH is defined as the STOP condition (P), is sent by the master (see Figure 10).

After the START condition, the device address byte is sent, MSB first, including the data direction bit (R/$\overline{W}$). This device does not respond to the general call address.

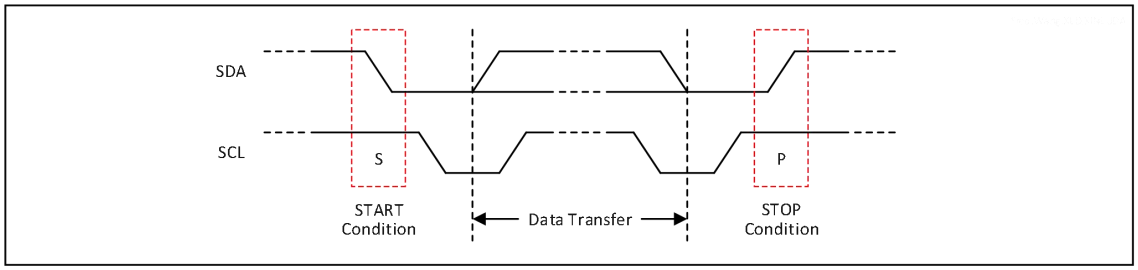


Figure 10. Definition of START and STOP Conditions

9.3. System Configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 11).

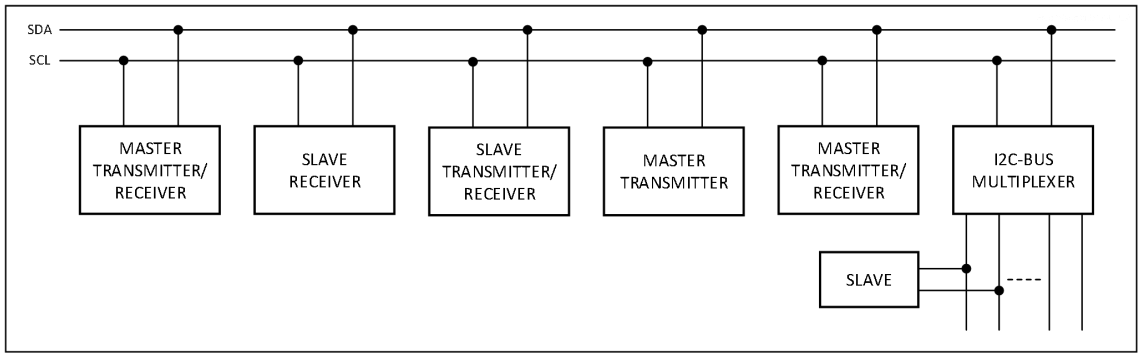


Figure 11. System Configuration

9.4. Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The ACK bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra ACK-related clock pulse.

When a slave receiver which is addressed, it must generate an ACK after the reception of each byte. Similarly, the master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable LOW during the HIGH period of the ACK-related clock pulse (see Figure 12). Set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte that has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must leave the SDA data line HIGH to enable the master to generate a STOP condition.

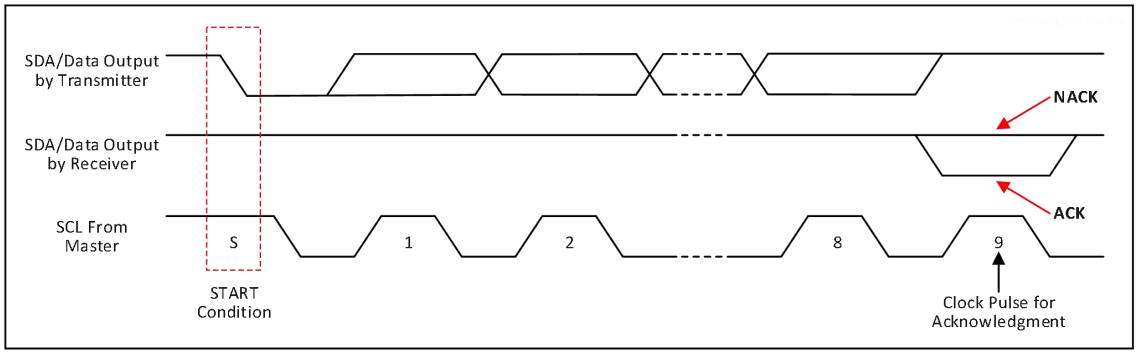


Figure 12. Acknowledgement on the I^2C-bus

10. FUNCTIONAL DESCRIPTION

10.1. Device Address

Table 3 and Table 4 shows the slave address byte of the XL8574.

Table 3. XL8574 device address

BIT	7(MSB)	6	5	4	3	2	1	0(LSB)
SYMBOL	0	1	0	0	A2	A1	A0	R/$\overline{W}$
DESCRIPTION	Fixed bits (A6~A3)				Hardware Selectable bits (A2~A0)			read/write
	I^2C Slave Address 7-BIT (A6~A0)							

Table 4. XL8574 Address Reference

FIXED BITS (A6~A3)				HARDWARE INPUTS (A2~A0)			R/$\overline{W}$	I^2C-BUS SLAVE 8-BIT	I^2C-BUS SLAVE 8-BIT
(MSB)	A5	A4	A3	A2	A1	A0	(LSB)	READ ADDRESS	WRITE ADDRESS
0	1	0	0	0	0	0	1/0	65(DEC), 0x41(HEX)	64(DEC), 0x40(HEX)
0	1	0	0	0	0	1	1/0	67(DEC), 0x43(HEX)	66(DEC), 0x42(HEX)
0	1	0	0	0	1	0	1/0	69(DEC), 0x45(HEX)	68(DEC), 0x44(HEX)
0	1	0	0	0	1	1	1/0	71(DEC), 0x47(HEX)	70(DEC), 0x46(HEX)
0	1	0	0	1	0	0	1/0	73(DEC), 0x49(HEX)	72(DEC), 0x48(HEX)
0	1	0	0	1	0	1	1/0	75(DEC), 0x4B(HEX)	74(DEC), 0x4A(HEX)
0	1	0	0	1	1	0	1/0	77(DEC), 0x4D(HEX)	76(DEC), 0x4C(HEX)
0	1	0	0	1	1	1	1/0	79(DEC), 0x4F(HEX)	78(DEC), 0x4E(HEX)

Table 5 and Table 6 shows the slave address byte of the XL8574A.

Table 5. XL8574A device address

BIT	7(MSB)	6	5	4	3	2	1	0(LSB)
SYMBOL	0	1	1	1	A2	A1	A0	R/$\overline{W}$
DESCRIPTION	Fixed bits (A6~A3)				Hardware Selectable bits (A2~A0)			read/write
	I^2C Slave Address 7-BIT (A6~A0)							

Table 6. XL8574A Address Reference

FIXED BITS (A6~A3)				HARDWARE INPUTS (A2~A0)			R/$\overline{W}$	I^2C-BUS SLAVE 8-BIT	I^2C-BUS SLAVE 8-BIT
(MSB)	A5	A4	A3	A2	A1	A0	(LSB)	READ ADDRESS	WRITE ADDRESS
0	1	1	1	0	0	0	1/0	113(DEC), 0x71(HEX)	112(DEC), 0x70(HEX)
0	1	1	1	0	0	1	1/0	115(DEC), 0x73(HEX)	114(DEC), 0x72(HEX)
0	1	1	1	0	1	0	1/0	117(DEC), 0x75(HEX)	116(DEC), 0x74(HEX)
0	1	1	1	0	1	1	1/0	119(DEC), 0x77(HEX)	118(DEC), 0x76(HEX)
0	1	1	1	1	0	0	1/0	121(DEC), 0x79(HEX)	120(DEC), 0x78(HEX)
0	1	1	1	1	0	1	1/0	123(DEC), 0x7B(HEX)	122(DEC), 0x7A(HEX)
0	1	1	1	1	1	0	1/0	125(DEC), 0x7D(HEX)	124(DEC), 0x7C(HEX)
0	1	1	1	1	1	1	1/0	127(DEC), 0x7F(HEX)	126(DEC), 0x7E(HEX)

The XL8574 and XL8574A are functionally the same, but have a different fixed portion of the slave address.

The device features 3 hardware address pins (A0, A1 and A2) to allow the user to program the device's I^2C slave address by pulling each pin to either V_{CC} or GND directly or through resistors to signify the bit value in the address. This allows up to 8 devices to be on the same bus without address conflicts. The voltage on the pins must not change while the device is powered up in order to prevent possible I^2C glitches as a result of the device address changing during a transmission. All of the pins must be tied either to V_{CC} or GND and cannot be left floating.

The last bit (R/$\overline{W}$) of the slave address defines the operation (read or write) to be performed. A high (logic 1) selects a read operation, while a low (logic 0) selects a write operation.

10.2. Quasi-bidirectional I/O Port

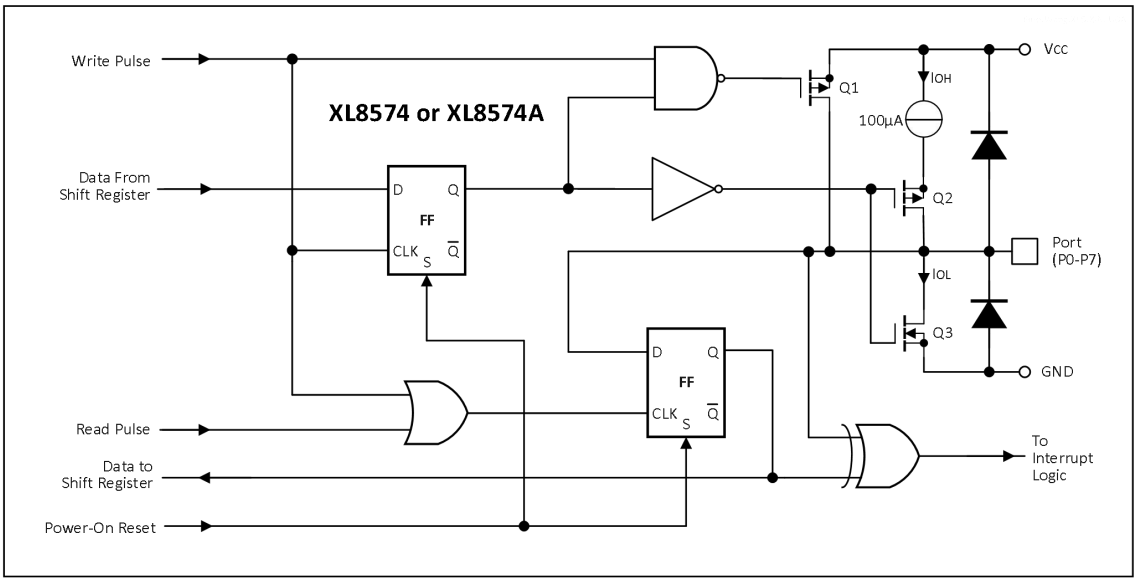


Figure 13. Simplified Schematic Diagram of each Port I/Os (P0 to P7)

A quasi-bidirectional I/O is an input or output port without using a direction control register. Whenever the master reads the register, the value returned to master depends on the actual voltage or status of the pin. At power on reset, all the ports are HIGH with a weak 100µA internal pull-up to V_{CC}, but can be driven LOW by an internal transistor, or an external signal. The I/O ports are entirely independent of each other, but each I/O octal is controlled by the same read or write data byte.

Advantages of the quasi-bidirectional I/O over totem pole I/O include:

- Better for driving LEDs since the P-channel (transistor to V_{CC}) is small, which saves die size and therefore cost. LED drive only requires an internal N-channel transistor to ground, while the LED is connected to V_{CC} through a current-limiting resistor. Totem pole I/O have both N-channel and P-channel transistors, which allow solid HIGH and LOW output levels without a pull-up resistor, it's good for logic levels.

- Simpler architecture — only a single register and the I/O can be both input and output at the same time. Totem pole I/O have a direction register that specifies the port pin direction and it is always in that configuration unless the direction is explicitly changed.
- Does not require a command byte. The simplicity of one register (no need for the pointer register or, technically, the command byte) is an advantage in some embedded systems where every byte counts because of memory or bandwidth limitations.

There is only one register to control four possibilities of the port pin: Input HIGH, input LOW, output HIGH, or output LOW.

- **Input HIGH:** The master needs to write 1 to the register to set the port as an input mode if the device is not in the default power-on condition. The master reads the register to check the input status. If the external source pulls the port pin up to V_{CC} or drives logic 1, then the master will read the logic value of 1.
- **Input LOW:** The master needs to write 1 to the register to set the port to input mode if the device is not in the default power-on condition. The master reads the register to check the input status. If the external source pulls the port pin down to GND or drives logic 0, which sinks the weak 100µA current source, then the master will read the logic value of 0.
- **Output HIGH:** The master writes 1 to the register. There is an additional '*accelerator*' or strong pull-up current when the master sets the port HIGH. The additional strong pull-up is only active during the HIGH time of the acknowledge clock cycle. This accelerator current helps the port's 100µA current source make a faster rising edge into a heavily loaded output, but only at the start of the acknowledge clock cycle to avoid bus contention if an external signal is pulling the port LOW to GND or driving the port with logic 0 at the same time. After the half clock cycle there is only the 100µA current source to hold the port HIGH.
- **Output LOW:** The master writes 0 to the register. There is a strong current sink transistor that holds the port pin LOW. A large current may flow into the port, which could potentially damage the part if the master writes a 0 to the register and an external source is pulling the port HIGH at the same time.

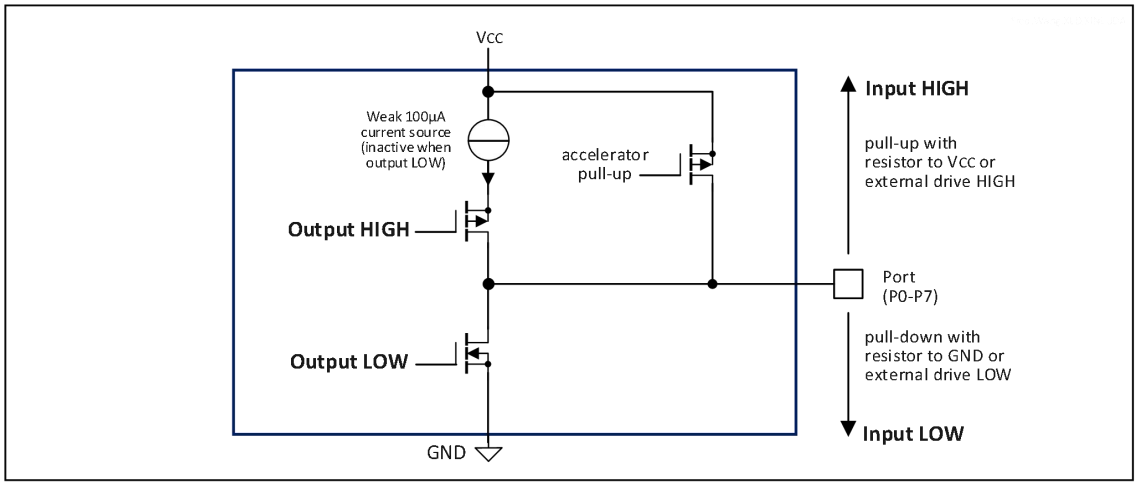


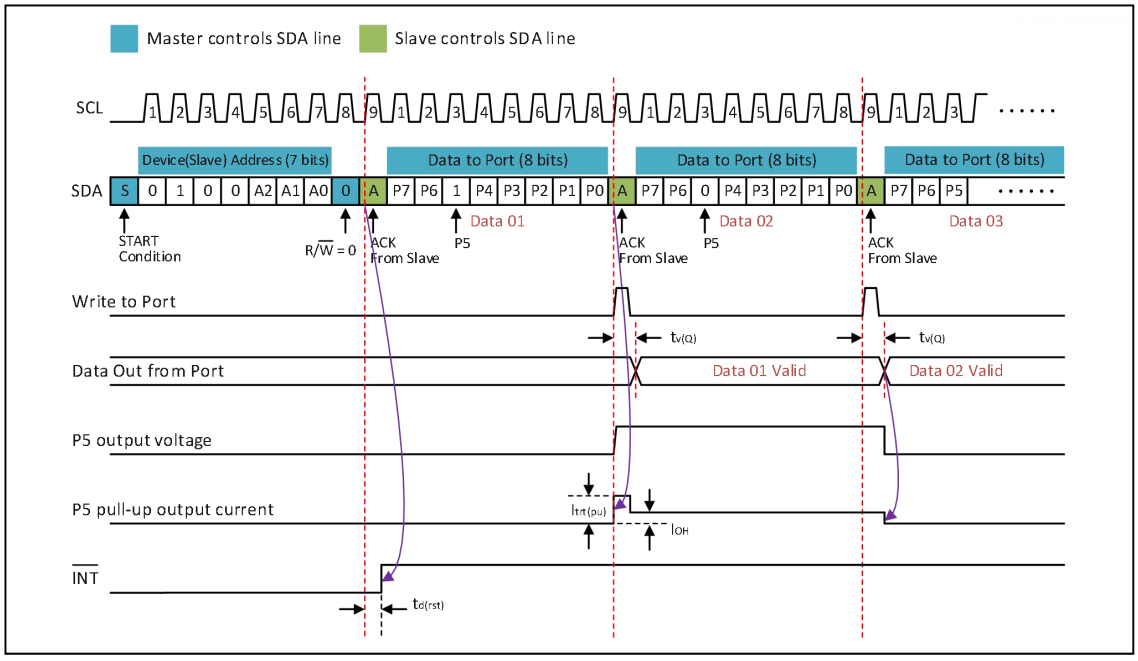
Figure 14. Simple quasi-bidirectional Port I/Os (P0 to P7)

10.3. Device Functional Modes

10.3.1. Writing to the port (Output mode)

The master (MCU) sends the START condition and slave address setting the last bit of the address byte to low (logic 0) for the write mode. The XL8574/8574A acknowledges and the master then sends the data byte for P7 to P0 to the port register. As the clock line goes HIGH, the 8-bit data is presented on the port lines after it has been acknowledged by the XL8574/8574A. If a LOW is written, the strong pull-down turns on and stays on. If a HIGH is written, the strong pull-up turns on for ½ of the clock cycle, then the line is held HIGH by the weak current source. The master can then send a STOP or ReSTART condition or continue sending data. The number of data bytes that can be sent successively is not limited and the previous data is overwritten every time a data byte has been sent and acknowledged.

Ensure a HIGH (logic 1) is written for any port that is being used as an input to ensure the strong external pull-down is turned off.



REMARK: (1) The device is XL8574 for this example.

Figure 15. Writing to the port (Output mode)

Simple code for Writing (Output Mode):

<S> <slave address + write> <**ACK**> <data out> <**ACK**> <data out> <**ACK**> ··· <data out> <**ACK**> <P>

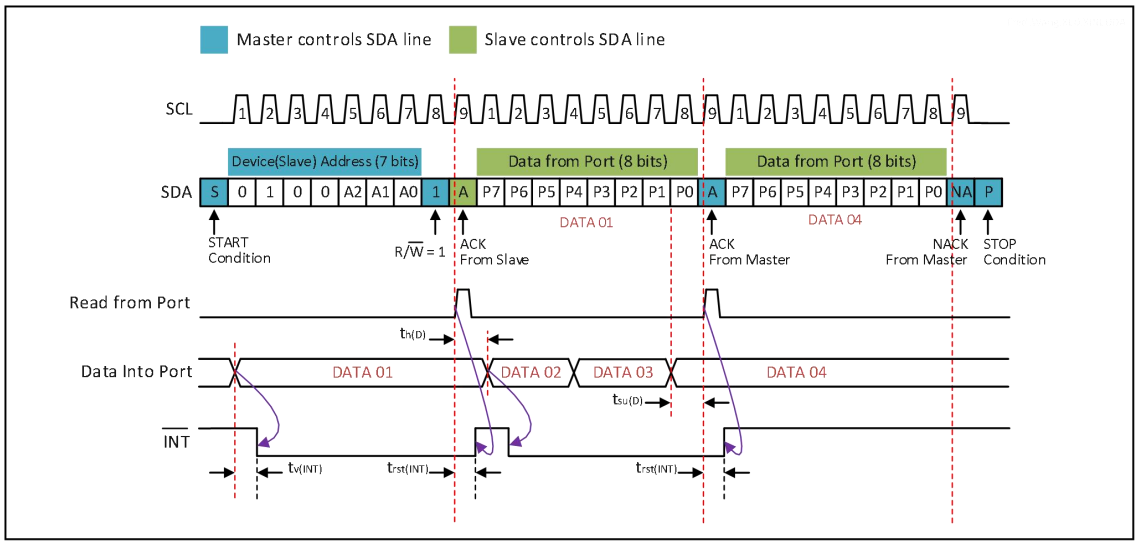
Remark: Bold type = generated by slave device.

10.3.2. Reading from a port (Input mode)

The port must have been previously written to HIGH (logic 1), which is the condition after power-on reset. To enter the Read mode the master (MCU) addresses the slave device and sets the last bit of the address byte to logic 1 (address byte read). The slave will acknowledge and then send the data byte to the master. The master will NACK and then send the STOP condition or ACK and read the input register again.

The read of any pin being used as an output will indicate HIGH or LOW depending on the actual state of the pin.

If the data on the input port changes faster than the master can read, this data may be lost. The DATA 02 and DATA 03 are lost because these data did not meet the setup time and hold time (see Figure 16).



REMARK: (1) The device is XL8574 for this example.

(2) A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge(ACK) phase is valid (output mode). Input data is lost.

Figure 16. Reading from a port (Input mode)

Simple code for Reading (Input Mode):

<S> <slave address + read> <**ACK**> <**data in**> <ACK> ⋯ <**data in**> <ACK> <**data in**> <NACK> <P>

Remark: Bold type = generated by slave device.

10.4. Power-on Reset (POR)

When power (from 0V) is applied to V_{CC}, an internal Power-On Reset(POR) holds the device (XL8574 or XL8574A) in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the device registers and I^2C/SMBus state machine will initialize to their default states. The power-on reset typically completes the reset and enables the part by the time the power supply is above V_{POR}. Thereafter, V_{CC} must be lowered below 0.2V to reset the device. For a power-reset cycle, V_{CC} must be lowered below 0.2V and then restored to the operating voltage.

10.5. Interrupt Output ($\overline{INT}$)

The device (XL8574 or XL8574A) provides an open-drain output ($\overline{INT}$) which can be fed to a corresponding input of the MCU (see Figure 17). As soon as a port input is changed, the $\overline{INT}$ will be active (output LOW) and notify the MCU.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to V_{CC}.

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time ($t_{iv(INT)}$) the signal $\overline{INT}$ is valid. The interrupt will reset to HIGH when data on the port is changed to the original setting or data is read or written by the master. In the Write mode, the interrupt may be reset (HIGH) on the rising edge of the acknowledge(ACK) bit of the address byte and also on the rising edge of the write to port pulse.

The interrupt will always be reset (HIGH) on the falling edge of the write to port pulse (see Figure 15). The interrupt is reset (HIGH) in the Read mode on the rising edge of the read from port pulse (see Figure 16).

During the interrupt reset, any I/O change close to the read or write pulse may not generate an interrupt, or the interrupt will have a very short pulse. After the interrupt is reset, any change in I/Os will be detected and transmitted as an $\overline{INT}$.

At power-on reset all ports are in Input mode and the initial state of the ports is HIGH, therefore, for any port pin that is pulled LOW or driven LOW by external source, the interrupt output will be active (LOW).

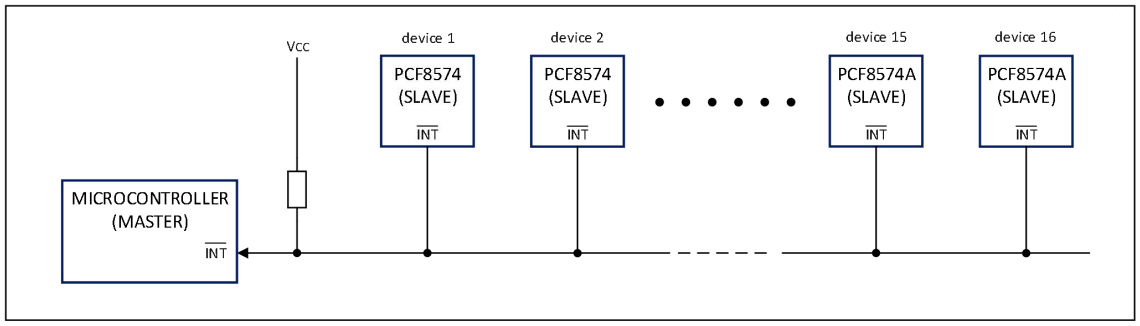


Figure 17. Application of multiple PCF8574/8574As with interrupt

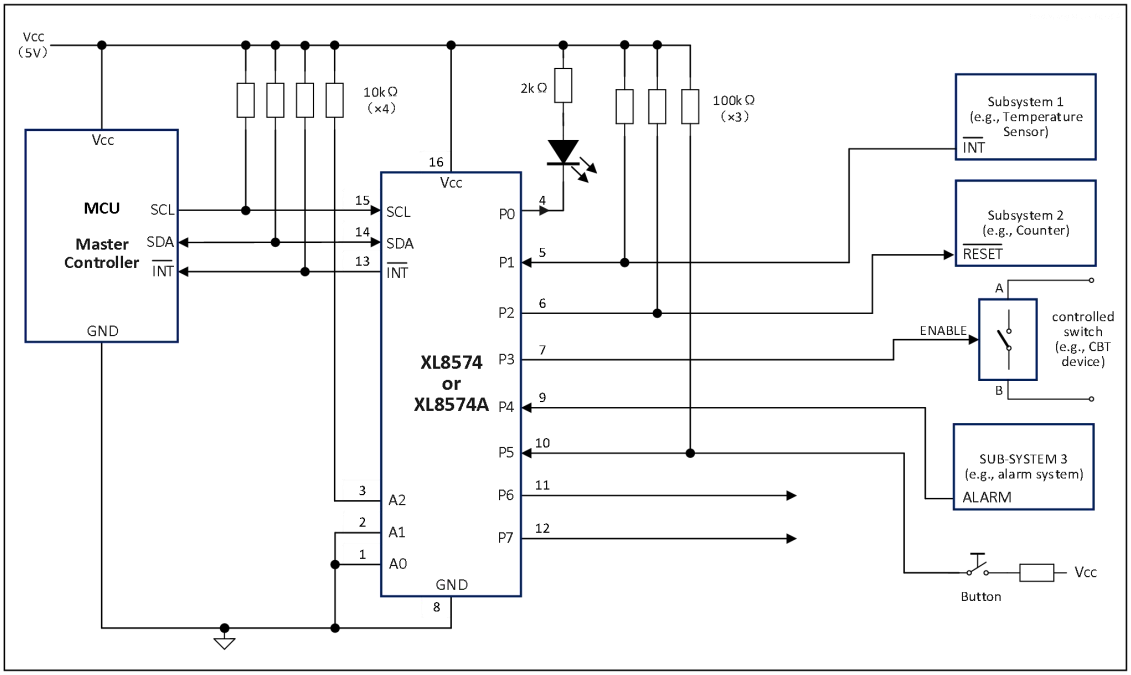
11. APPLICATION INFORMATION

11.1. Bidirectional I/O Expander Application

Figure 18 shows an application in which the device (XL8574 or XL8574A) can be used. In this bidirectional 8-bit I/O expander application, P1, and P4-P5 are configured as inputs, and P0, P2-P3 and P6-P7 are configured as outputs. When used in this configuration, during a write, the input I/Os must be written as HIGH (logic 1) so the external devices fully control the input ports.

The desired HIGH or LOW logic levels may be written to the ports used as outputs. If 10μA internal output HIGH is not enough current source, the port needs external pull-up resistor. During a read, the logic levels of the external devices driving the input ports and the previous written logic level to the output ports will be read.

The GPIO also has an interrupt line ($\overline{INT}$) that can be connected to the interrupt logic of the MCU. By sending an interrupt signal on this line, the remote I/O informs the MCU that there has been a change of data on its ports without having to communicate via the I^2C-bus.



REMARK: (1) XL8574 device address is configured as 0100 100Xb for this example.

XL8574A device address is configured as 0111 100Xb for this example.

(2) P1 and P4-P5 are configured as inputs.

(3) P0, P2-P3, and P6-P7 are configured as outputs.

(4) P6 and P7 are not used and must be configured as outputs.

(5) Pin numbers shown are for DIP16/SOP16/SOP16W packages.

Figure 18. Bidirectional I/O Expander Application

11.2. High Current-drive Load Application

The GPIO has a minimum guaranteed sinking current of 10mA per bit at 5V. In applications requiring additional drive, two port pins may be connected together to sink up to 20mA current. Both bits must then always be turned on or off together.

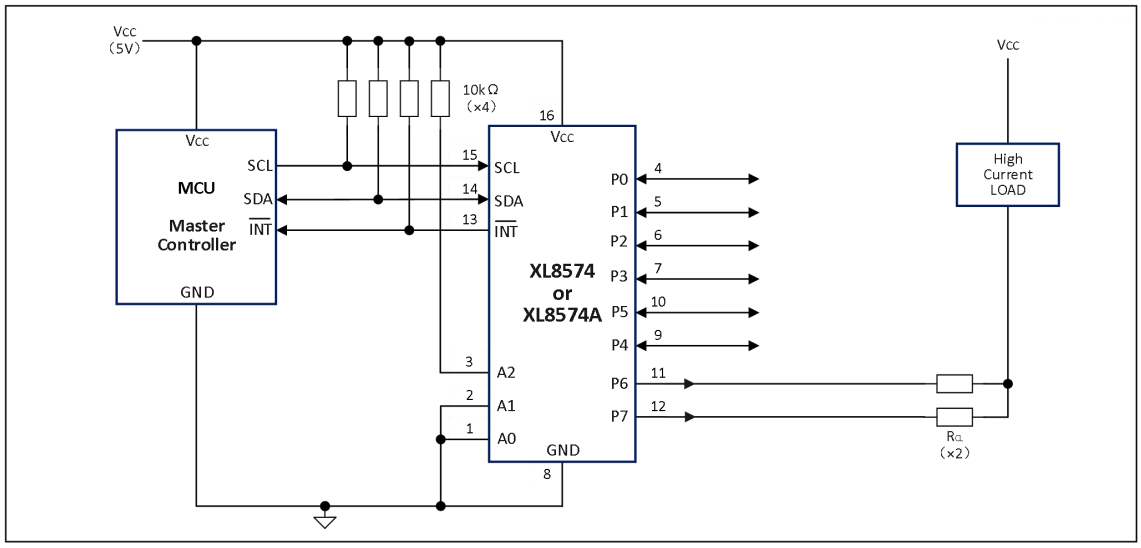


Figure 19. High Current-drive Load Application

Up to five pins can be connected together to drive 80mA, which is the device recommended total current limit. Each pin needs its own current-limiting resistor as shown in Figure 19 to prevent damage to the device should all ports not be turned on at the same time.

11.3. Minimizing I_{CC} when the I/Os are used to control LEDs

When the device I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in Figure 18. Because the LED acts as a diode, with threshold voltage V_T, and when a I/O is configured as an input the LED will be off, but the I/O V_{IN} is a V_T drop below V_{CC}. For a I/O configured as an input, the supply current (I_{CC}) increases as V_{IN} becomes lower than V_{CC}.

Designs for battery-powered applications, it is essential that the voltage of I/O pins controlling LEDs off is greater than or equal to V_{CC} when the I/O are configured as input to minimize current consumption. Figure 20 shows a high-value resistor in parallel with the LED. Figure 21 shows V_{CC} less than the LED supply voltage by at least V_T. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevents additional supply current consumption when the I/O is configured as an input and the LED is off.

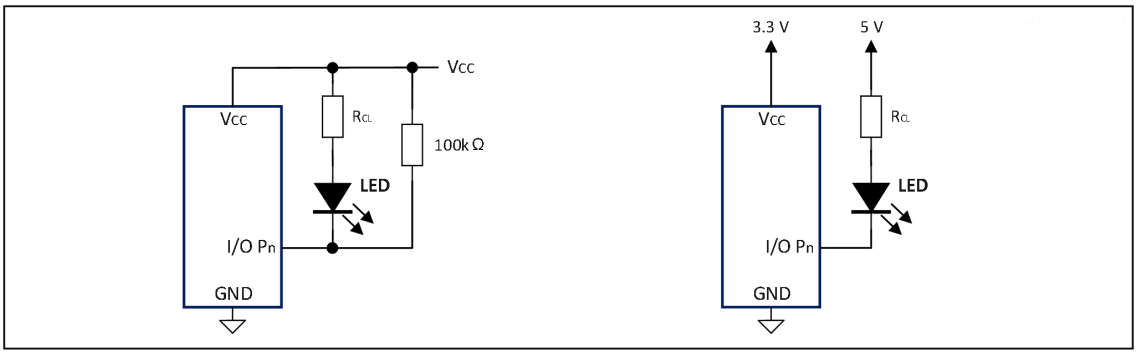


Figure 20. High-Value Resistor in Parallel With the LED

Figure 21. Device Supplied by a Lower Voltage

12. ESD AND HANDLING INFORMATION

This IC can be damaged by Electrostatic Discharge (ESD). It recommends that all ICs be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision ICs may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

These devices have limited built-in ESD protection. All input and output pins are protected against ESD under normal handling. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

13. ABBREVIATIONS

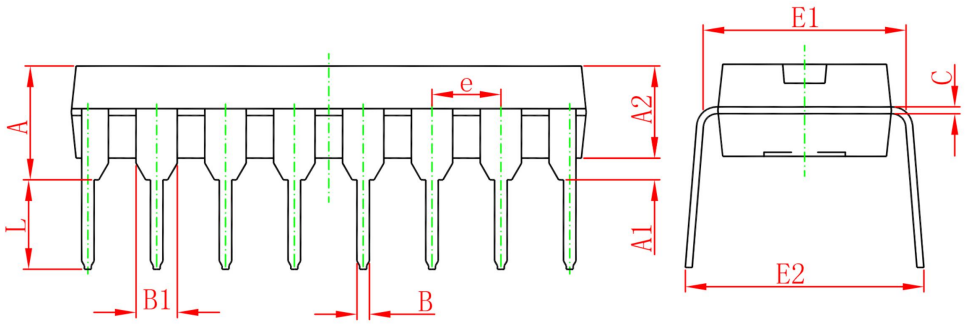
Table 15. Abbreviations

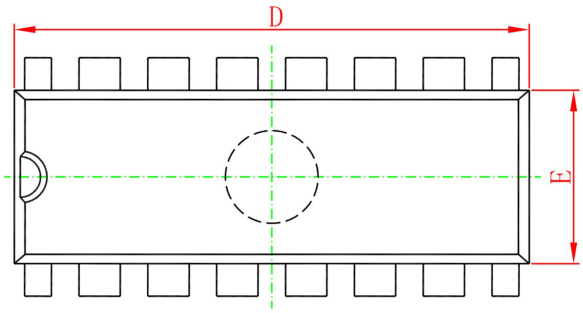
ACRONYM	DESCRIPTION
ACPI	Advanced Configuration and Power Interface
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DEC	Decimal
DUT	Device Under Test
ESD	Electrostatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
HBM	Human Body Model
HEX	Hexadecimal
IC	Integrated Circuit
I/O	Input/Output
I^2C-bus	Inter-Integrated Circuit bus
LED	Light Emitting Diode
LSB	Least Significant Bit
MCU	Microcontroller Unit
MM	Machine Model
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
SMBus	System Management Bus

14. PACKAGE INFORMATION

14.1. DIP16(300mil) Package outline dimensions

DIP16(300mil): plastic dual in-line package; 16 leads 300mil. body width 6.35mm/250mil.

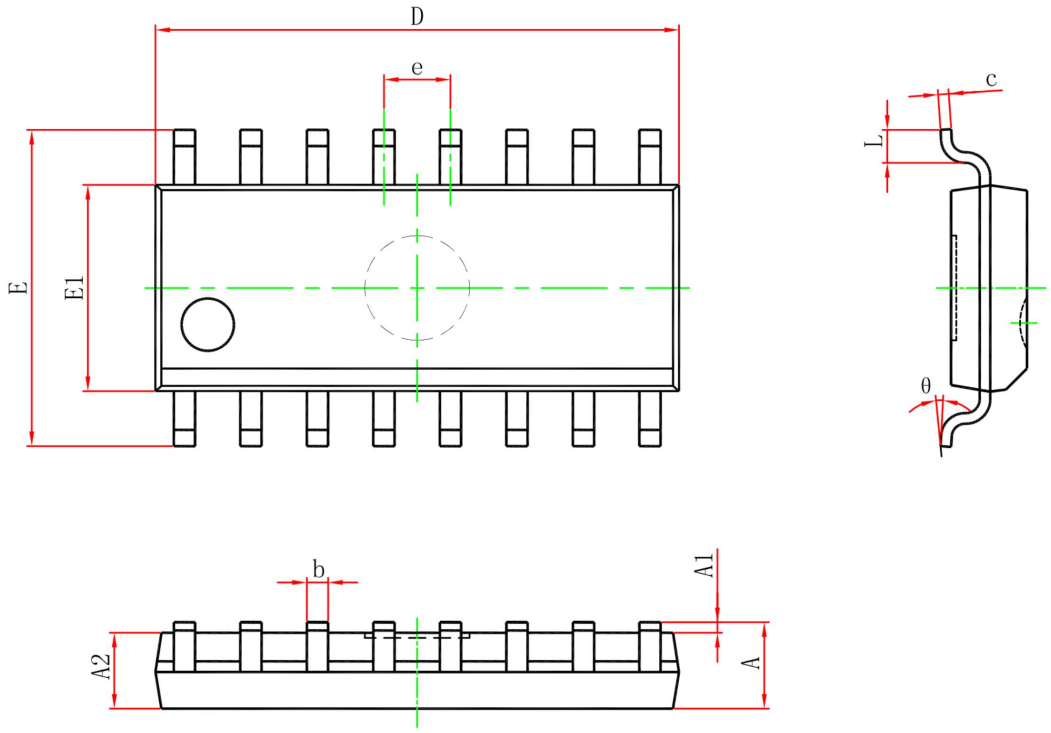




SYMBOL	Dimensions In Millimeters			Dimensions In Inches		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.710	—	4.310	0.146	—	0.170
A1	0.510	—	—	0.020	—	—
A2	3.200	3.300	3.400	0.126	0.130	0.134
B	0.440	—	0.530	0.017	—	0.021
C	0.250	—	0.300	0.010	—	0.012
D	18.950	19.050	19.150	0.746	0.750	0.754
e	2.540 (BSC)			0.100 (BSC)		
E	6.250	6.350	6.450	0.246	0.250	0.254
E1	7.320	—	7.920	0.288	—	0.312
E2	8.300	—	9.300	0.327	—	0.366
L	3.000	—	3.600	0.118	—	0.142
θ	0°	—	8°	0°	—	8°

14.2. SOP16(150mil) Package outline dimensions

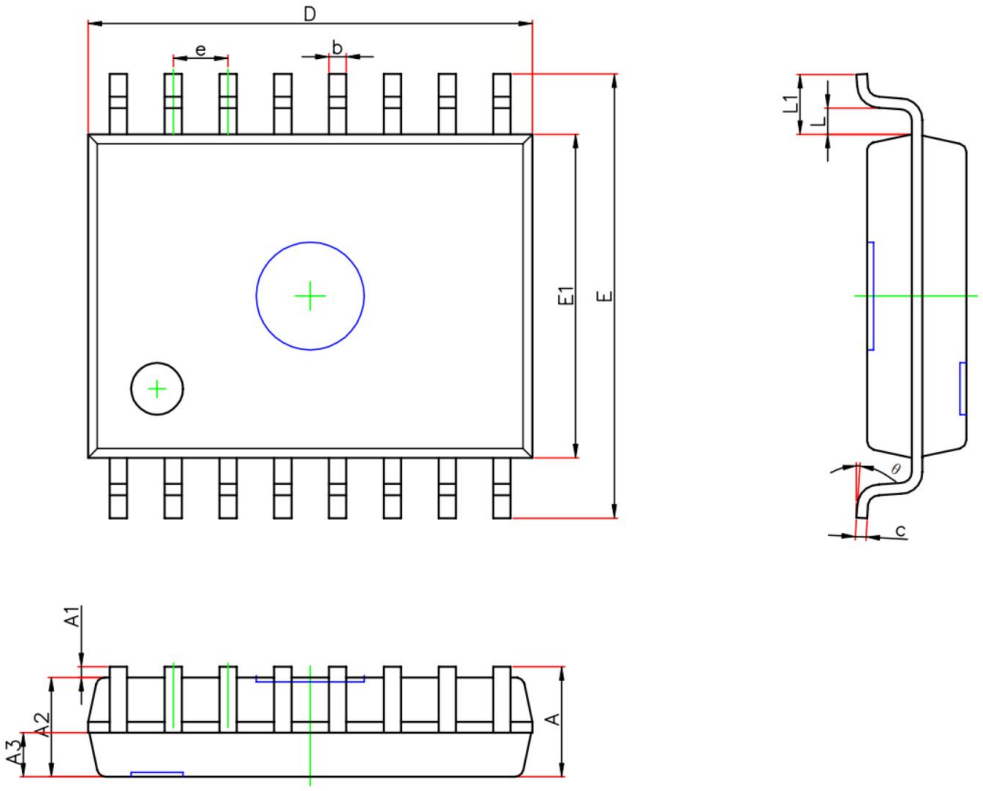
SOP16(150mil): plastic small outline package; 16 leads; body width 3.90mm/150mil.



SYMBOL	Dimensions In Millimeters			Dimensions In Inches		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.450	—	1.850	0.057	—	0.073
A1	0.050	—	0.250	0.002	—	0.010
A2	1.400	—	1.600	0.055	—	0.063
b	0.356	—	0.456	0.014	—	0.018
c	0.203	—	0.233	0.008	—	0.009
D	9.800	10.000	10.200	0.386	0.394	0.402
e	1.270 (BSC)			0.050 (BSC)		
E	5.840	—	6.240	0.230	—	0.246
E1	3.800	3.900	4.000	0.150	0.154	0.157
L	0.400	—	0.700	0.016	—	0.028
θ	0°	—	8°	0°	—	8°

14.3. SOP16W(300mil) Package outline dimensions

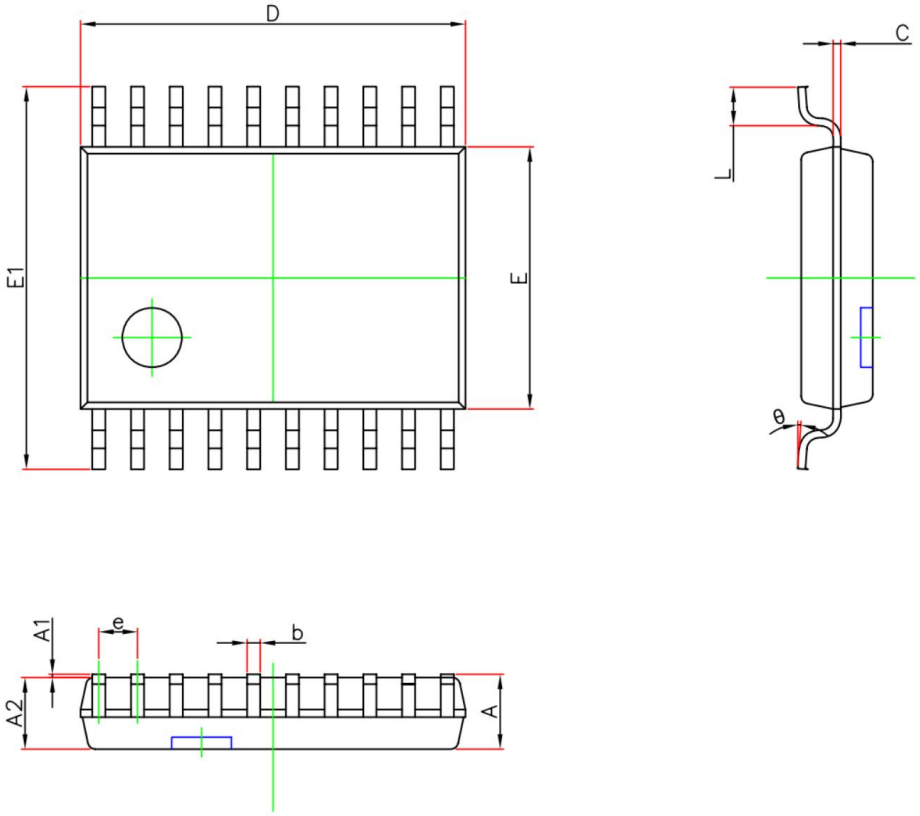
SOP16W(300mil): plastic small outline package; 16 leads; Wide body, body width 7.50mm/300mil.



SYMBOL	Dimensions In Millimeters			Dimensions In Inches		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	—	—	2.650	—	—	0.104
A1	0.100	0.200	0.300	0.004	0.008	0.012
A2	2.200	2.300	2.4000	0.087	0.091	0.094
b	0.390	—	0.470	0.015	—	0.019
c	0.250	—	0.300	0.010	—	0.012
D	10.100	10.200	10.300	0.398	0.402	0.406
e	1.270 (BSC)			0.050 (BSC)		
E	10.260	10.410	10.600	0.404	0.410	0.417
E1	7.400	7.500	7.600	0.291	0.295	0.299
L	0.550	—	0.850	0.022	—	0.033
L1	1.400 (REF)			0.060 (REF)		
θ	0°	—	8°	0°	—	8°

14.4. SSOP20(173mil) Package outline dimensions

SSOP20(173mil): plastic shrink small outline package; 20 leads; body width 4.40mm/173mil.



SYMBOL	Dimensions In Millimeters			Dimensions In Inches		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	—	—	1.450	—	—	0.057
A1	0.050	—	0.200	0.002	—	0.008
A2	1.150	—	1.250	0.045	—	0.049
b	0.200	—	0.310	0.008	—	0.012
c	0.090	—	0.200	0.004	—	0.008
D	6.300	6.500	6.700	0.248	0.256	0.264
E	4.300	4.400	4.500	0.169	0.173	0.177
E1	6.200	6.400	6.600	0.244	0.252	0.260
e	0.650 (BSC)			0.026 (BSC)		
L	0.450	—	0.750	0.018	—	0.030
θ	0°	—	8°	0°	—	8°