MSKSEMI 美森科



ESD





TSS



MOV



GDT



PIFF

PTVSHC2EN12VU-MS

Product specification





Features

- 1600W Peak pulse power per line (t_P = 8/20µs)
- DFN1610-2 package
- Response time is typically < 1 ns
- Protect one I/O or power line
- Low clamping Voltage
- RoHS compliant
- Transient protection for data lines to
 IEC 61000-4-2(ESD) ±30KV(air), ±30KV(contact);
 IEC 61000-4-4 (EFT) 40A (5/50ns)

Mechanical Characteristics

- Lead finish:100% matte Sn(Tin)
- Mounting position: Any
- Qualified max reflow temperature:260 °C
- Pure tin plating: 7 ~ 17 um
- Pin flatness:≤3mil
- Device meets MSL3 requirements

Applications

- Cell phone handsets and accessories
- Personal digital assistants (PDA's)
- Notebooks, desktops, and servers
- Portable instrumentation
- Cordless phones
- Digital cameras
- Peripherals
- MP3 players

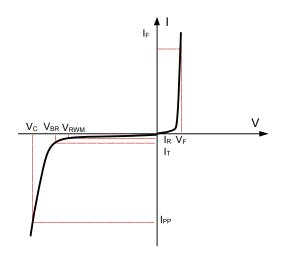
Reference News

PACKAGE OUTLINE	Circuit Diagram	Marking
		H12N
DFN1610-2L		



Electronics Parameter

Symbol	Parameter
VRWM	Peak Reverse Working Voltage
lR	Reverse Leakage Current @ V _{RWM}
V _{BR}	Breakdown Voltage @ I⊤
lτ	Test Current
 PP	Maximum Reverse Peak Pulse Current
Vc	Clamping Voltage @ IPP
P _{PP}	Peak Pulse Power
Cı	Junction Capacitance
lF	Forward Current
VF	Forward Voltage @ I _F



Electrical characteristics per line@25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Peak Reverse Working Voltage	V RWM				12	V
Breakdown Voltage	V _{BR}	k = 1mA	13.5	15.0		V
Reverse Leakage Current	l R	V _{RWM} = 12V			1	μΑ
Clamping Voltage	Vc	I _{PP} =65A t _P = 8/20μs		30.0	35.0	V
Junction Capacitance	Cj	V _R =0V f = 1MHz	300	355	400	pF

Absolute maximum rating@25℃

Rating	Symbol	Value	Units
Peak Pulse Power (t⊳ = 8/20µS)	P _{pp}	1600	W
Lead Soldering Temperature	TL	260 (10 sec)	$^{\circ}$
Operating Temperature	TJ	-55 to +125	$^{\circ}$
Storage Temperature	Тѕтс	-55 to +150	${\mathbb C}$



TypicalCharacteristics

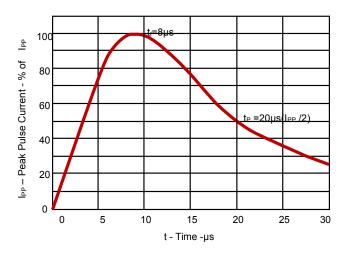


Fig 1.Pulse Waveform

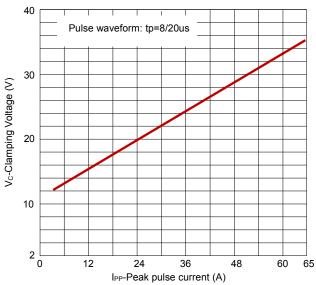
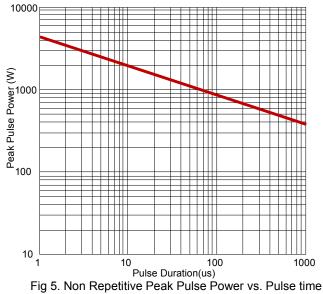


Fig 3. Clamping voltage vs. Peak pulse current



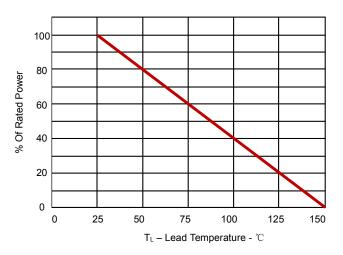


Fig 2.Power Derating Curve

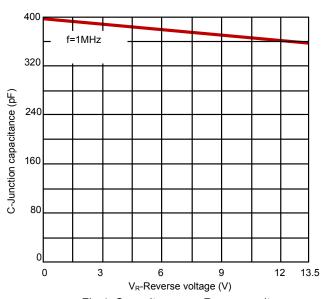
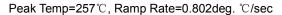
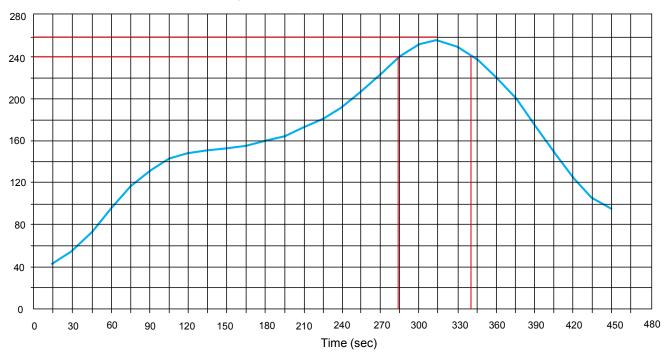


Fig 4. Capacitance vs. Reveres voltage



SolderReflowRecommendation





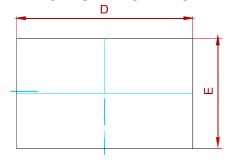
PCBDesign

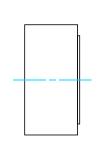
For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

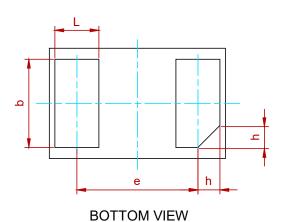
- Do not use stubs, but place the cathode of the TVS diode directly on the signal trace.
- Do not make false economies and save copper for the ground connection.
- Place via holes to ground as close as possible to the anode of the TVS diode.
- Use as many via holes as possible for the ground connection.
- Keep the length of via holes in mind! The longer the more inductance they will have.



PACKAGE MECHANICAL DATA







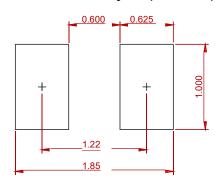
TOP VIEW



SIDE VIEW

O. mah al	D	Dimensions in Millimeters			
Symbol	Min.	Тур.	Max.		
А	0.45	0.50	0.55		
A1	0.00	0.02	0.05		
С		0.15 Ref.			
b	0.75	0.80	0.85		
L	0.35	0.40	0.45		
D	1.55	1.60	1.65		
E	0.95	1.00	1.05		
е		1.10 BSC			
h		0.20 Ref.			

Recommend PCB Layout (Unit: mm)



Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

REEL SPECIFICATION

P/N	PKG	QTY
PTVSHC2EN12VU-MS	DFN1610-2	3000



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