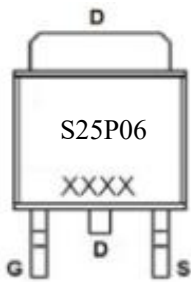
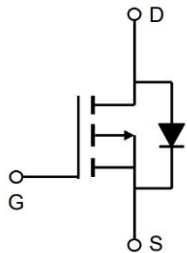


Features	<i>Bvdss</i>	<i>Rdson</i>	<i>ID</i>
	-60V	39mΩ	-25A
➤ Split Gate Trench MOSFET technology ➤ Excellent package for heat dissipation ➤ High density cell design for low $R_{DS(ON)}$			
Application ➤ DC-DC Converters ➤ Synchronous-rectification applications ➤ Power management functions			
RoHS			
Package    Marking and pin assignment TO-252-3L top view Schematic diagram			

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
25P06	S25P06	TO-252-3L	2500

Absolute Maximum Ratings ($T_J=25^{\circ}\text{C}$ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C=25^{\circ}\text{C}$	I_D	-25	A
	$T_C=100^{\circ}\text{C}$	I_D	-16	A
Pulsed Drain Current		I_{DM}^1	-100	A
Single Pulse Avalanche Energy		E_{AS}^2	48	mJ
Power Dissipation	$T_C = 25^{\circ}\text{C}$	P_D	40	W
Operating junction and storage temperature		T_J, T_{STG}	150, -55~150	$^{\circ}\text{C}$
Maximum Temperature for Soldering		T_L	260	$^{\circ}\text{C}$



Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	3.12	$^{\circ}\text{C/W}$

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS25P06	TO-252-3L	1	2	3	Tape Reel

Electrical Characteristics ($T_j=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-60	-	-	V
Gate-body Leakage current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60V, V_{GS} = 0V$	-	-	1	μA
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.3	-1.8	-2.3	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -10A$	-	39	50	m Ω
		$V_{GS} = -4.5V, I_D = -5A$	-	50	72	
Input Capacitance	C_{ISS}	$V_{DS} = -30V, V_{GS} = 0V,$ $f = 1MHz$	-	667	-	pF
Output Capacitance	C_{OSS}		-	114	-	
Reverse Transfer Capacitance	C_{RSS}		-	5.2	-	
Gate Resistance	R_g	$V_{GS} = 0V, V_{DS}$ Open	-	5.0	-	Ω
Total Gate Charge	Q_g	$V_{GS} = -10V, V_{DS} = -30V, I_D = -10A$	-	11.6	-	nC
Gate-Source Charge	Q_{gs}		-	2.4	-	
Gate-Drain Charge	Q_{gd}		-	1.5	-	
Turn-On Delay Time	$T_{d(on)}$	$V_{GS} = -10V, V_{DS} = -30V,$ $R_G = 3\Omega, I_D = -10A$	-	10	-	ns
Rise Time	T_R		-	6	-	
Turn-Off Delay Time	$T_{d(off)}$		-	40	-	
Fall Time	T_F		-	13	-	
Diode Forward Current	I_S	$T_C = 25^{\circ}\text{C}$	-	-	-25	A
Diode Pulse Current	I_{SM}		-	-	-100	A
Diode Forward Voltage	V_{SD}	$I_S = -10A, V_{GS} = 0V$	-	-	-1.2	V
Reverse Recovery time	T_{rr}	$I_S = -10A, V_{DD} = -30V$	-	28	-	ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s$	-	40	-	nC

Note :

1.Repetitive rating; pulse width limited by maximum junction temperature

2. $V_{DD}=30V$, $L=0.3mH$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

General Description:

Fig1:Typ. output characteristics

$I_D=f(V_{DS})$, $T_J=25^\circ C$; parameter: V_{GS}

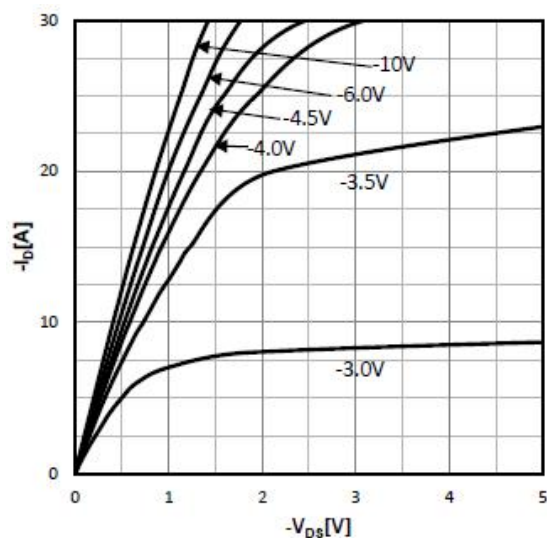


Fig2:Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$, $T_J=25^\circ C$; parameter: V_{GS}

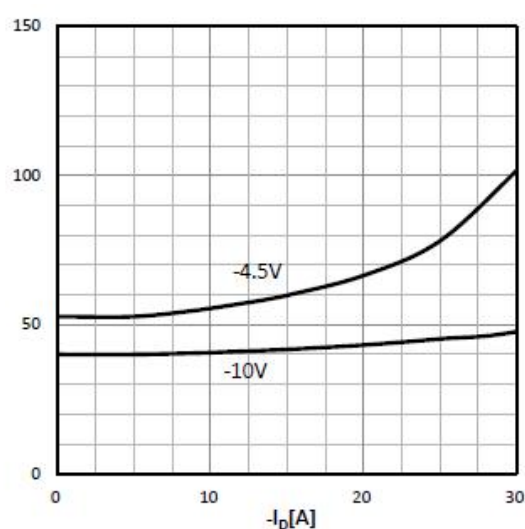


Fig3:Typ. transfer characteristics

$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)}max$;

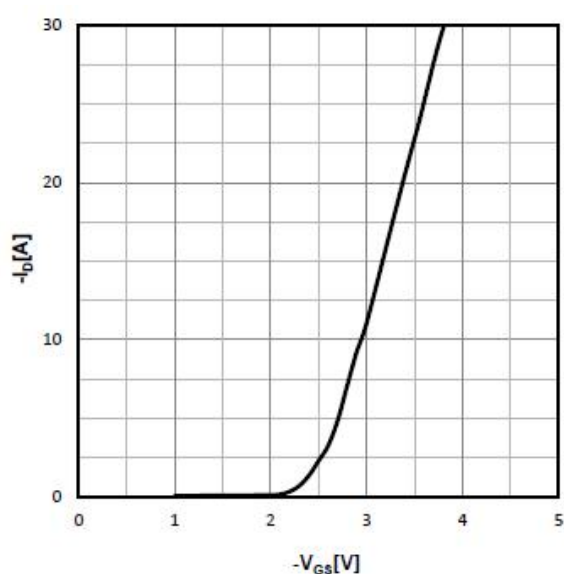


Fig4:Typ. drain-source on resistance

$R_{DS(on)}=f(T_J)$, $I_D=-10A$, $V_{GS}=-10V$;

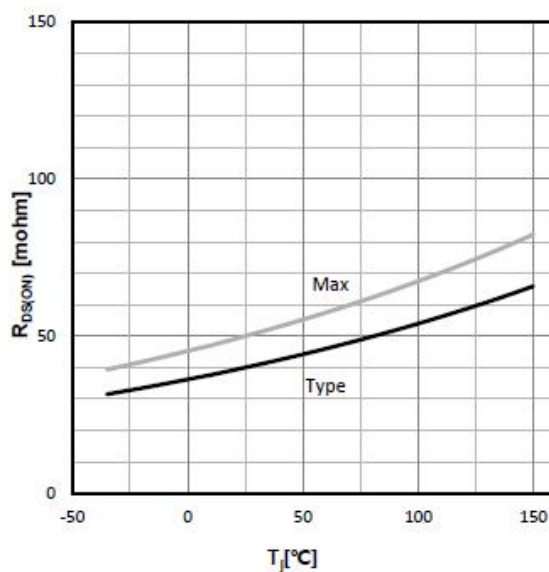


Fig5:Typ. gate threshold voltage

$V_{GS}=f(T_J)$, $V_{GS}=V_{DS}$, $I_D=-250 \mu A$;

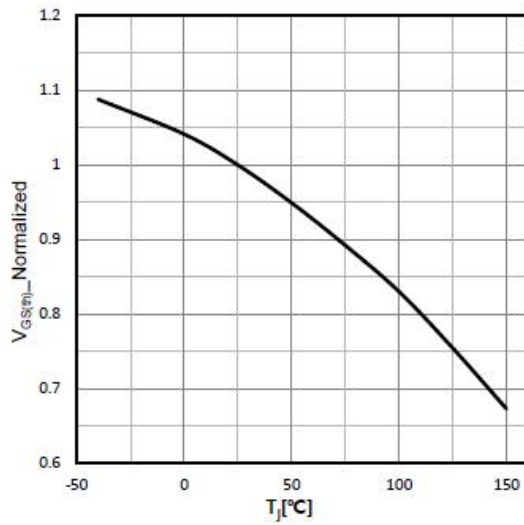


Fig6:Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_J)$; $I_D=-250 \mu A$;

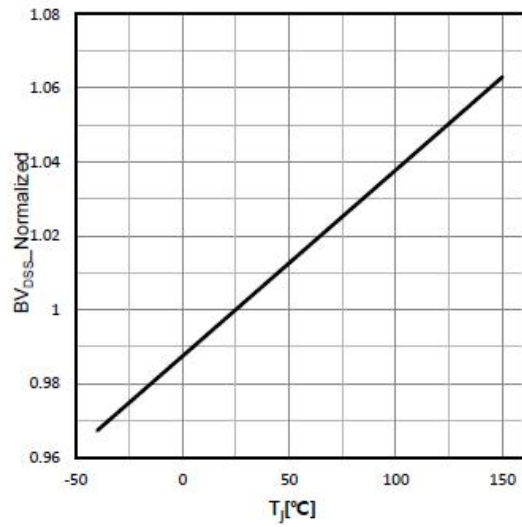


Fig7:Typ. gate charge

$V_{GS}=f(Q_g)$, $I_D=-10A$, $T_J=25^\circ C$; parameter: V_{DS}

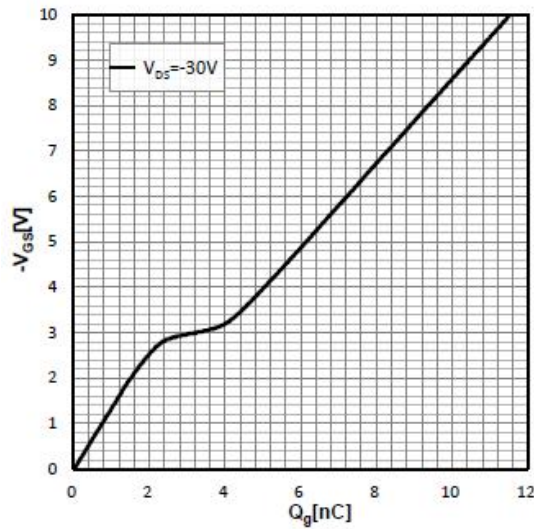


Fig8:Typ. Capacitances

$C=f(V_{DS})$; $V_{GS}=0V$; $f=1.0 MHz$;

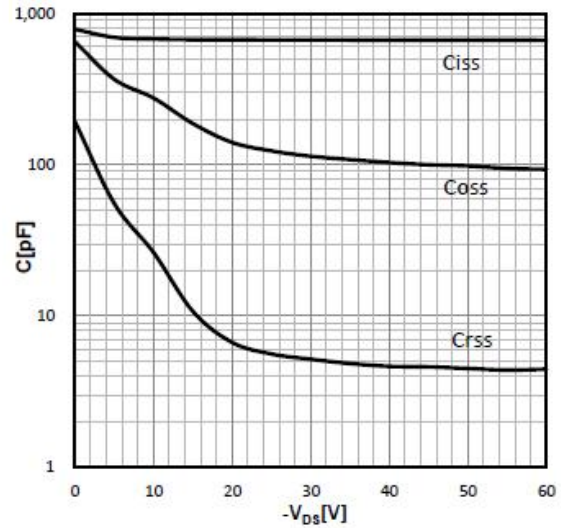


Fig9:Power Dissipation

$P_{tot}=f(T_c)$

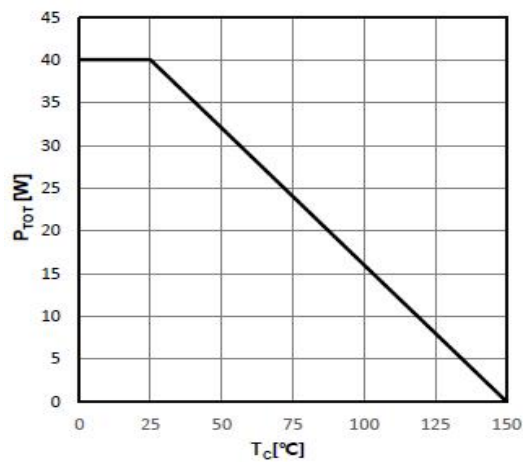


Fig10:Drain current

$I_D=f(T_c)$

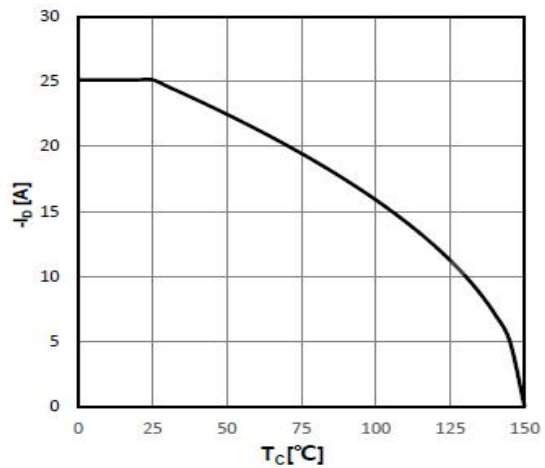


Fig11:Safe operating area

$I_D=f(V_{DS})$; $T_C=25^\circ\text{C}$; $D=0$; parameter: t_p

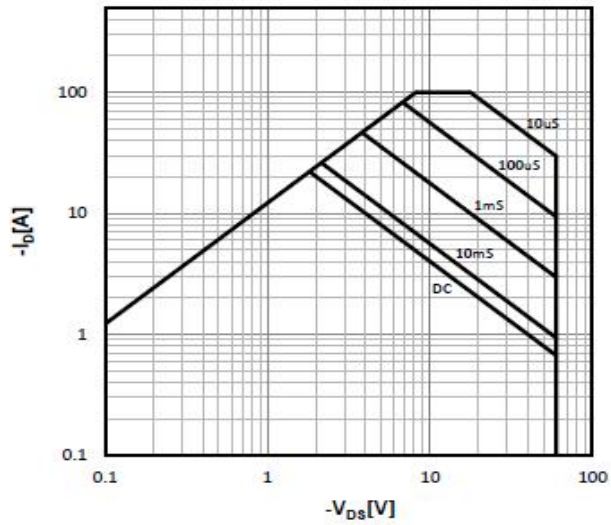


Fig12:Typ. forward characteristics

$I_F=f(V_{SD})$

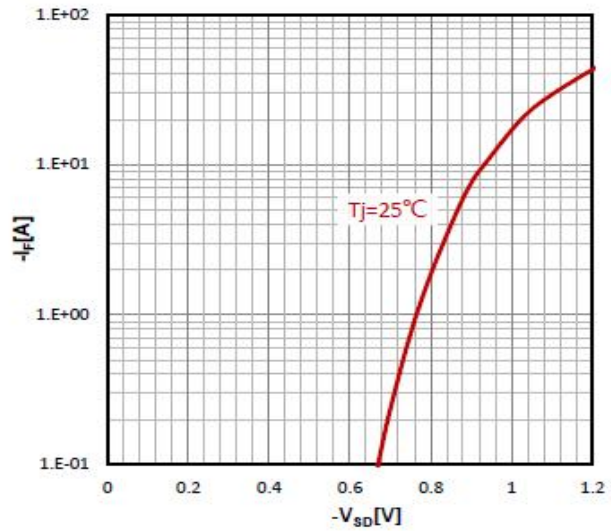
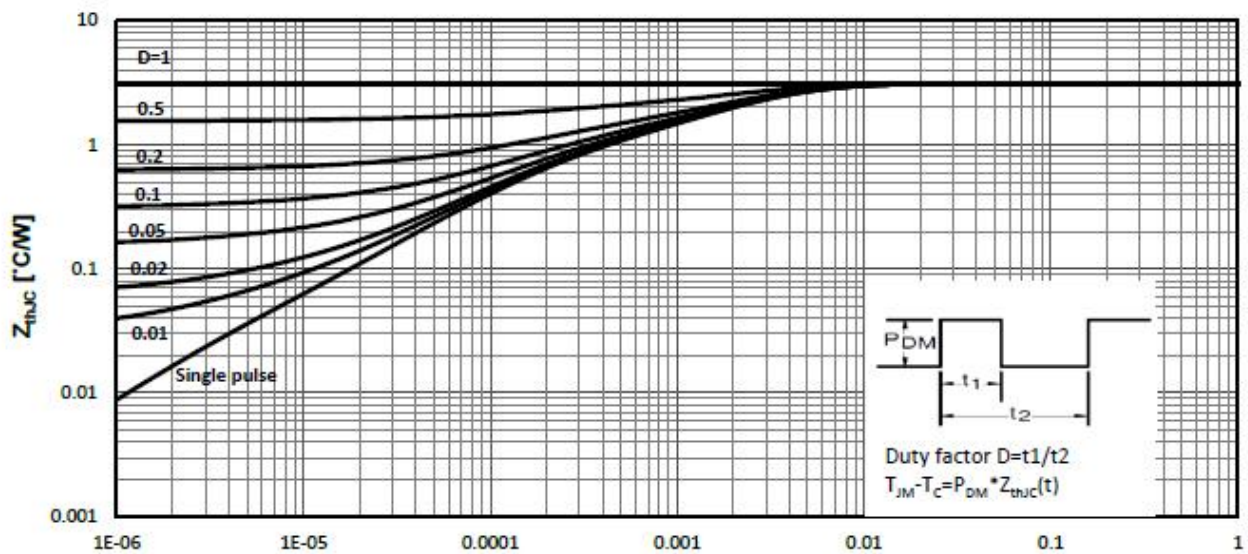


Figure 13: Max. Transient Thermal Impedance

$Z_{thJC}=f(t_p)$; parameter: D



Test Circuit and Waveform

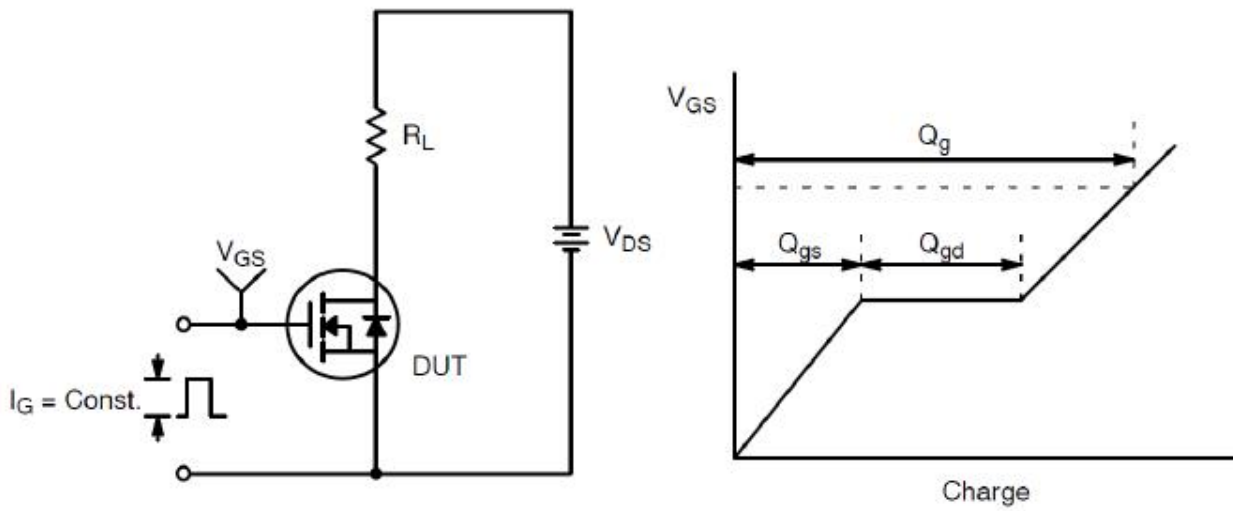


Fig-1: Gate Charge Test Circuit & Waveform

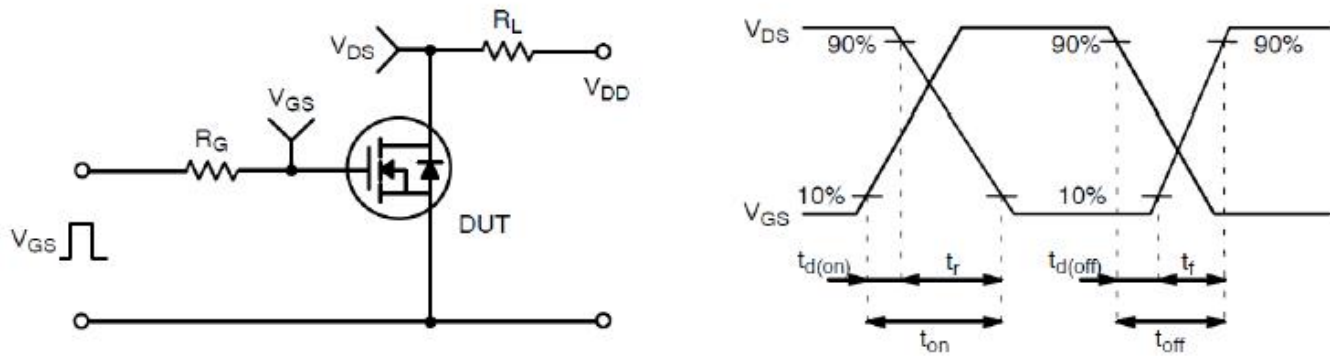


Fig-2: Resistive Switching Test Circuit & Waveforms

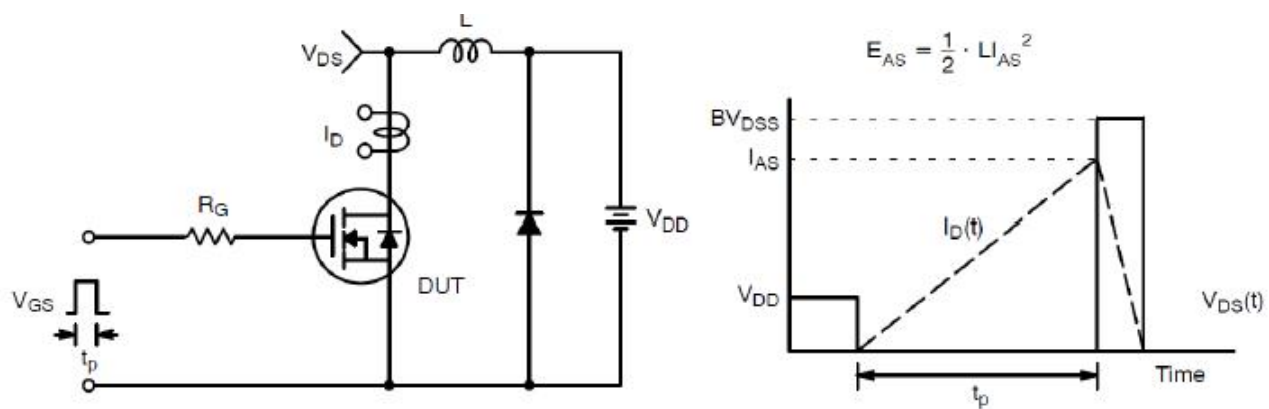
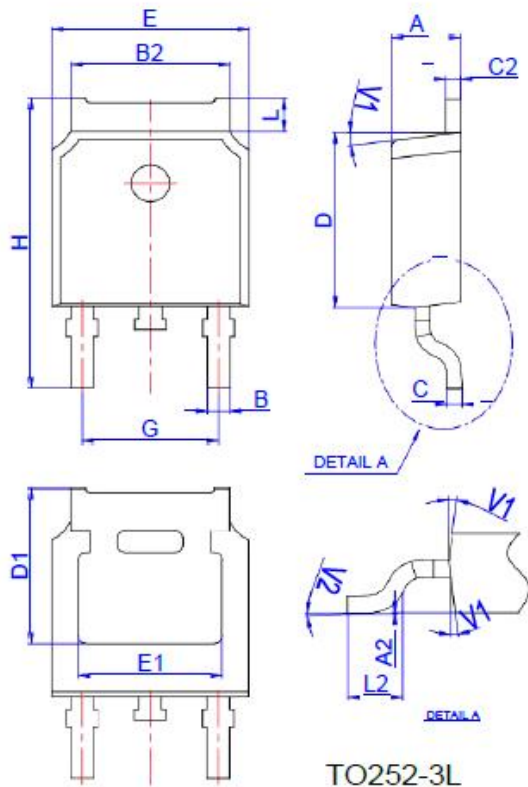
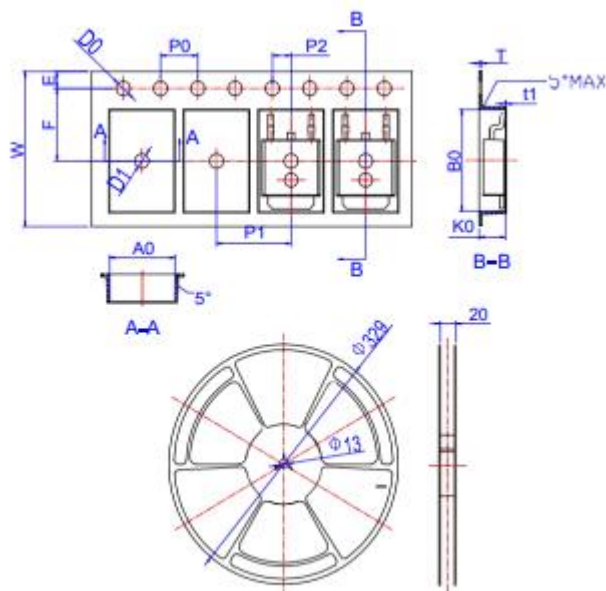


Fig-3: Unclamped Inductive Switching Test Circuit & Waveforms

Package Dimensions TO252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

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