

Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Bvdss

-60V

Rdson

12mΩ

ID

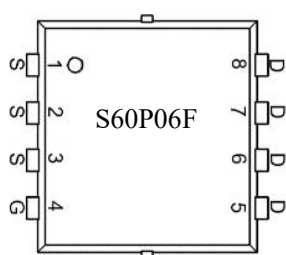
-60A

Application

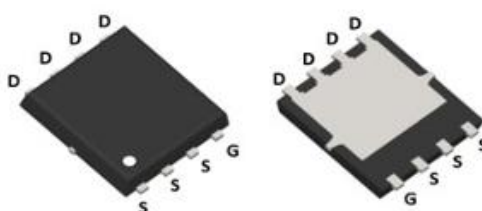
- Battery switching application
- Hard switched and high frequency circuits
- Power management

RoHS

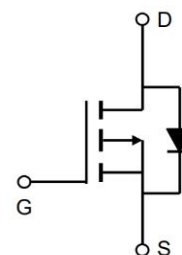
Package



Marking and pin assignment



PDFN5*6-8L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
60P06	S60P06F	PDFN5*6-8L	5000

Absolute Maximum Ratings ($T_J=25^{\circ}\text{C}$ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C=25^{\circ}\text{ C}$	I_D	-60	A
	$T_C=100^{\circ}\text{ C}$	I_D	-38	A
Pulsed Drain Current		I_{DM}^1	-240	A
Single Pulse Avalanche Energy		E_{AS}^2	337	mJ
Power Dissipation	$T_C = 25^{\circ}\text{C}$	P_D	114	W
Operating junction and storage temperature		T_J, T_{STG}	150, -55 ~ 150	$^{\circ}\text{C}$
Maximum Temperature for Soldering		T_L	260	$^{\circ}\text{C}$



Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	1.1	$^{\circ}\text{C}/\text{W}$
Thermal resistance, junction – ambient	$R_{\theta JA}^*$	60	$^{\circ}\text{C}/\text{W}$

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS60P06F	PDFN5*6-8L	4	5,6,7,8	1,2,3	Tape Reel

Electrical Characteristics (Tj=25 $^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$	-60	-	-	V
Gate-body Leakage current	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1.3	-1.8	-2.3	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{V}, I_D = -20\text{A}$	-	12	16	m Ω
		$V_{GS} = -4.5\text{V}, I_D = -10\text{A}$	-	16	20	
Input Capacitance	C_{ISS}	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$	-	2630	-	pF
Output Capacitance	C_{OSS}		-	484	-	
Reverse Transfer Capacitance	C_{RSS}		-	9.4	-	
Gate Resistance	R_g	$V_{GS} = 0\text{V}, V_{DS}$ Open	-	12.5	-	Ω
Total Gate Charge	Q_g	$V_{GS} = -10\text{V}, V_{DS} = -30\text{V}, I_D = -10\text{A}$	-	38	-	nC
Gate-Source Charge	Q_{gs}		-	6.9	-	
Gate-Drain Charge	Q_{gd}		-	4.98	-	
Turn-On Delay Time	$T_{d(on)}$	$V_{GS} = -10\text{V}, V_{DS} = -30\text{V},$ $R_G = 3\Omega, I_D = -10\text{A}$ $R_L = 3\Omega$	-	20	-	ns
Rise Time	T_R		-	25	-	
Turn-Off Delay Time	$T_{d(off)}$		-	60	-	
Fall Time	T_F		-	30	-	
Diode Forward Current	I_S	$T_C = 25^{\circ}\text{C}$	-	-	-60	A
Diode Forward Voltage	V_{SD}	$I_S = -5.0\text{A}, V_{GS} = 0\text{V}$	-	-	-1.2	V
Reverse Recovery time	T_{rr}	$I_S = -10\text{A}, V_{DD} = -30\text{V}$ $dI/dt = 100\text{A}/\mu\text{s}$	-	50	-	ns
Reverse Recovery Charge	Q_{rr}		-	80	-	nC

Note :

- 1.Repetitive rating; pulse width limited by maximum junction temperature
2. $V_{DD}=30V$, $L=0.3mH$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

Typical Performance Characteristics

Fig1:Typ. output characteristics

$$I_D=f(V_{DS})$$

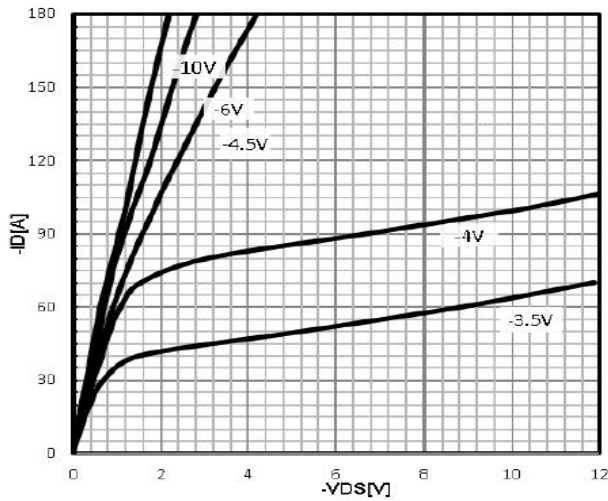


Fig2:Typ. drain-source on resistance

$$R_{DS(on)}=f(I_D)$$

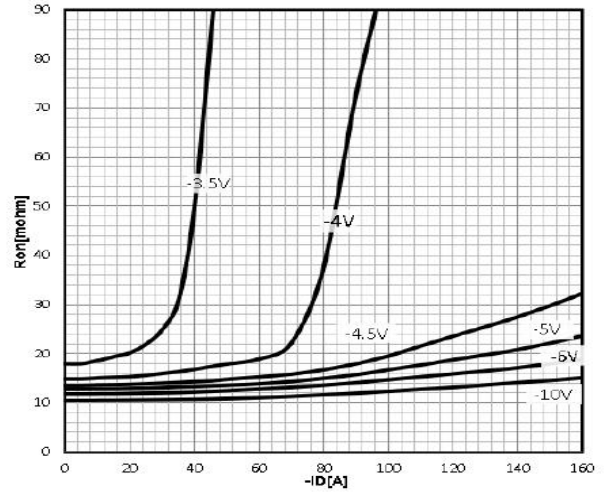


Fig3:Typ. transfer characteristics

$$-I_D=f(-V_{GS})$$

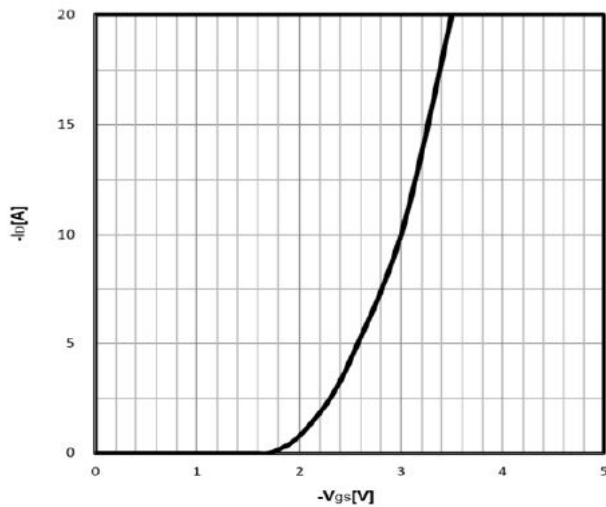


Fig4:Drain-source on-state resistance

$$R_{DS(on)}=f(T_J)|_{I_D=-20A; V_{GS}=-10V}$$

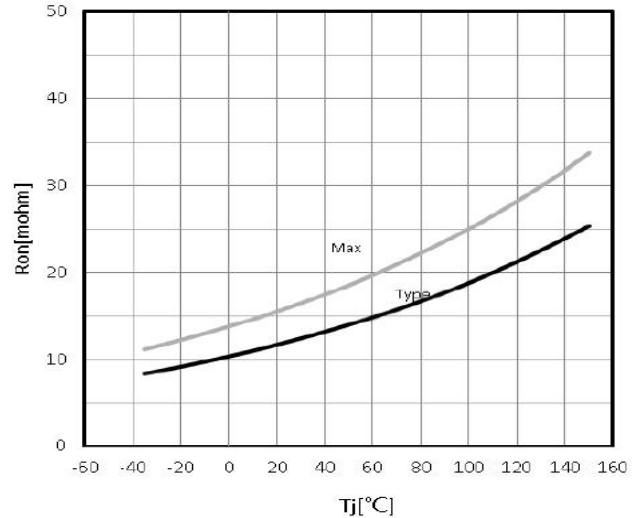


Fig5:Gate Threshold Voltage

$$-V_{TH}=f(T_J); I_D=-250\mu A$$

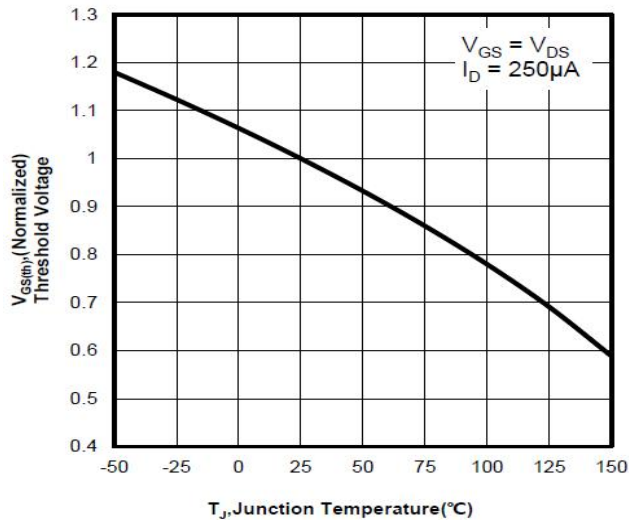


Fig6:Drain-source breakdown voltage

$$-V_{BR(DSS)}=f(T_J); I_D=-250\mu A$$

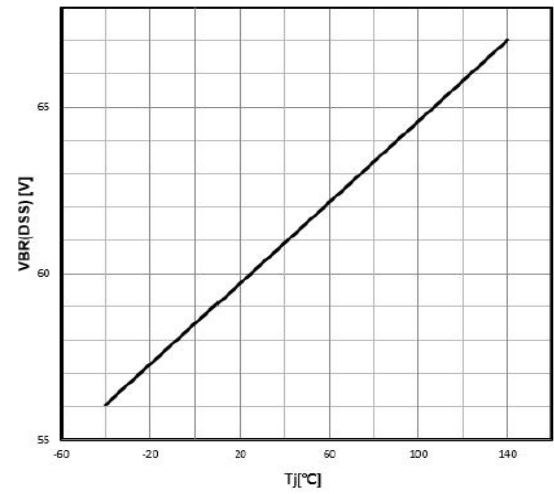


Fig7:Typ. gate charge

$$V_{GS}=f(Q_{gate}); I_D=-10A$$

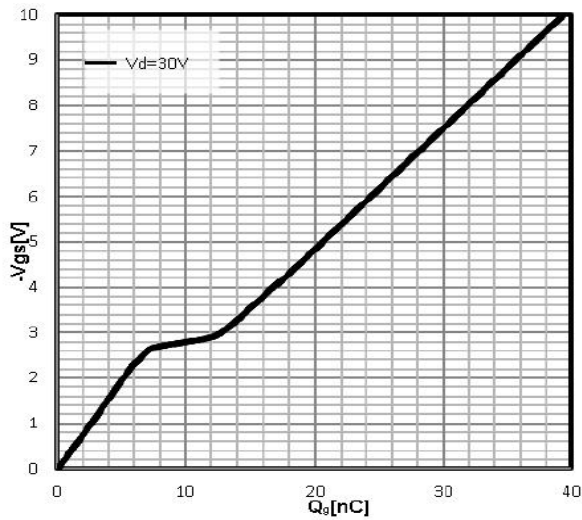


Fig8:Typ. Capacitances

$$C=f(-V_{DS}); V_{GS}=0V; f=1MHz$$

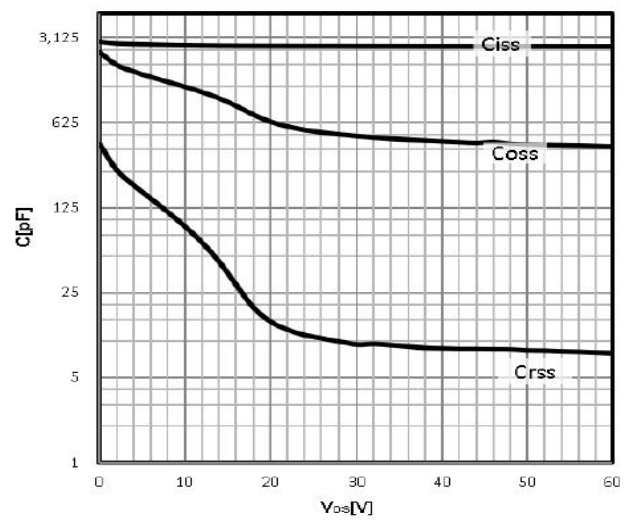


Fig9:Power Dissipation

$$P_{tot}=f(T_C)$$

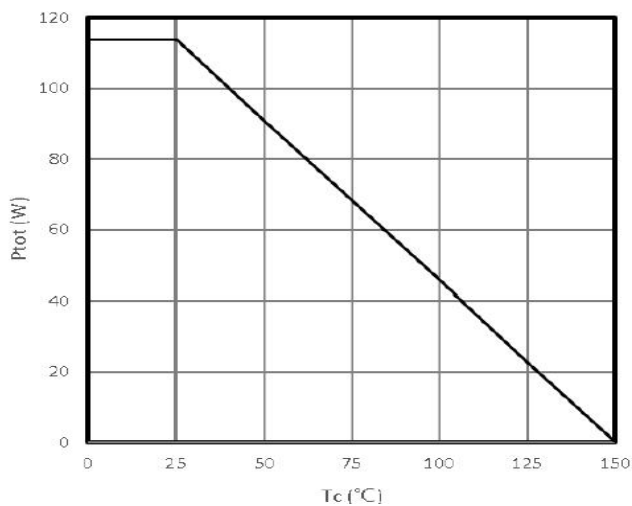


Fig10:Maximum Drain Current

$$-I_D=f(T_C)$$

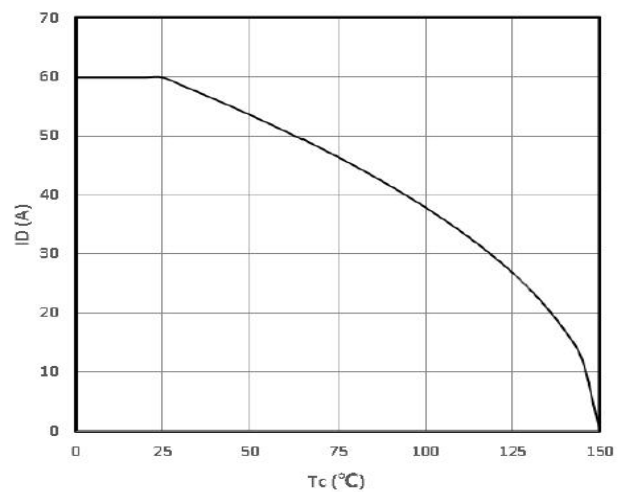


Fig11:Safe operating area

$$-I_D = f(-V_{DS})$$

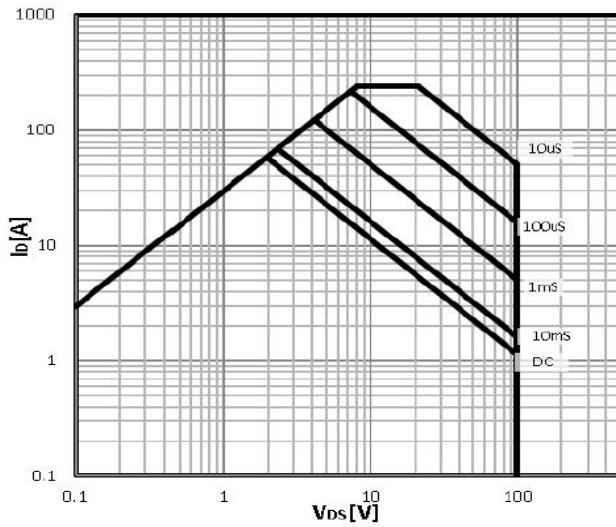


Fig12:Body Diode Forward Voltage Variation

$$-I_F = f(-V_{DS})$$

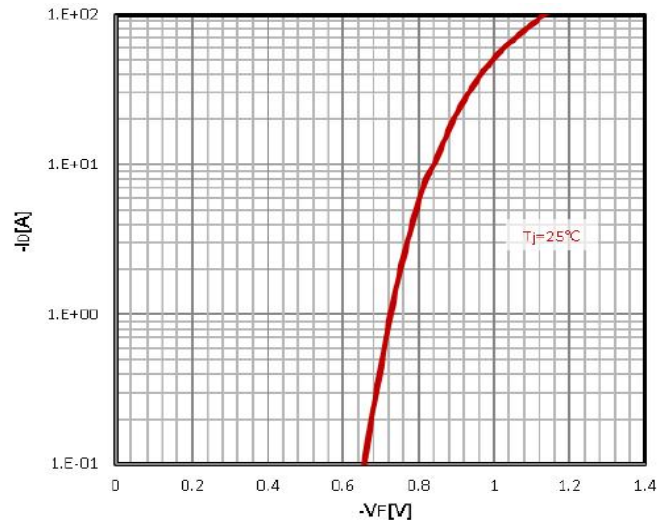
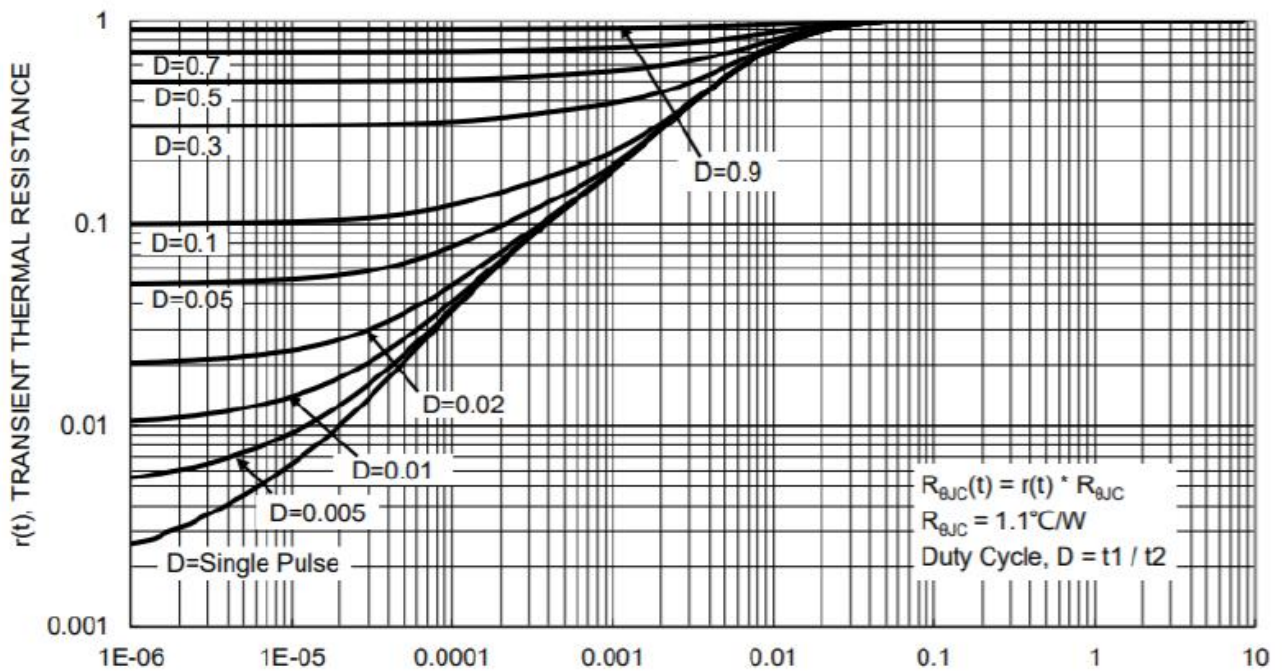


Fig12:Body Diode Forward Voltage Variation



Test Circuit and Waveform

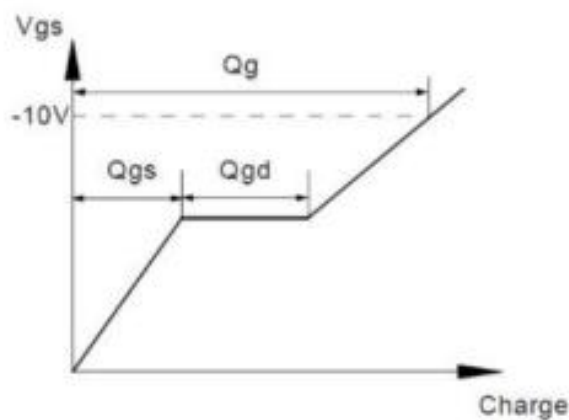
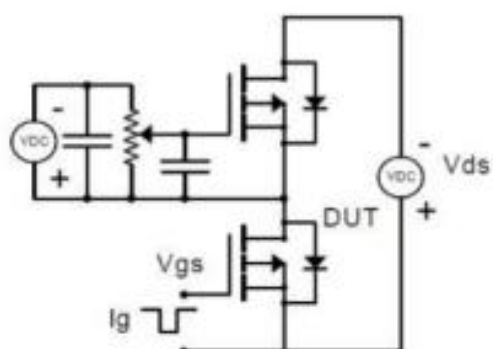


Figure.1: Gate Charge Test Circuit & Waveform

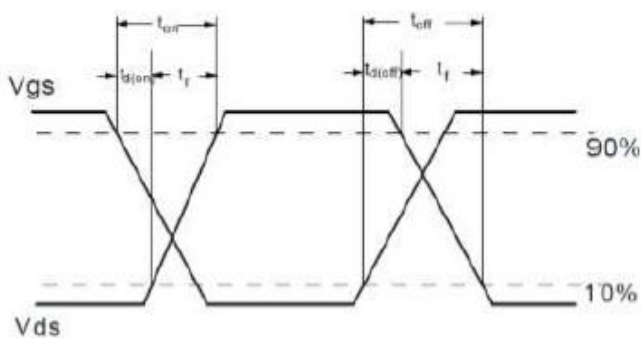
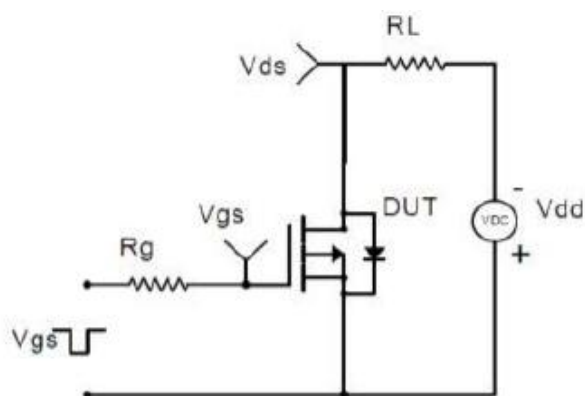


Figure.2: Resistive Switching Test Circuit & Wave forms

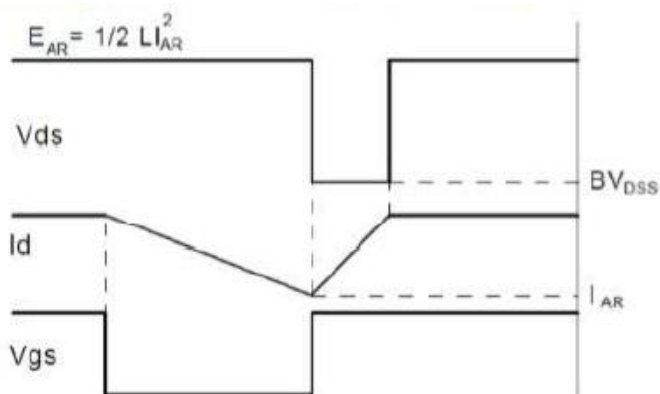
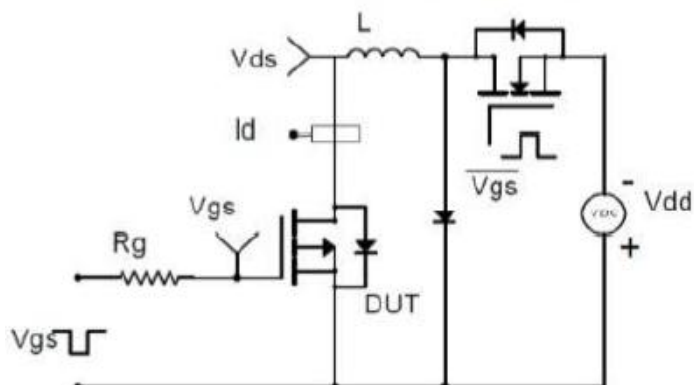


Figure.3: Unclamped inductive Switching (UIS) Test Circuit & Wave forms

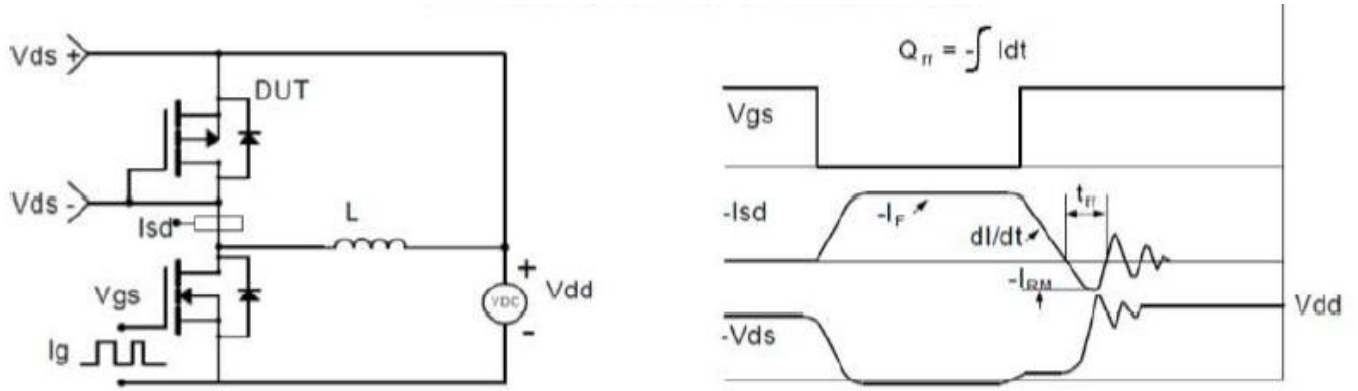
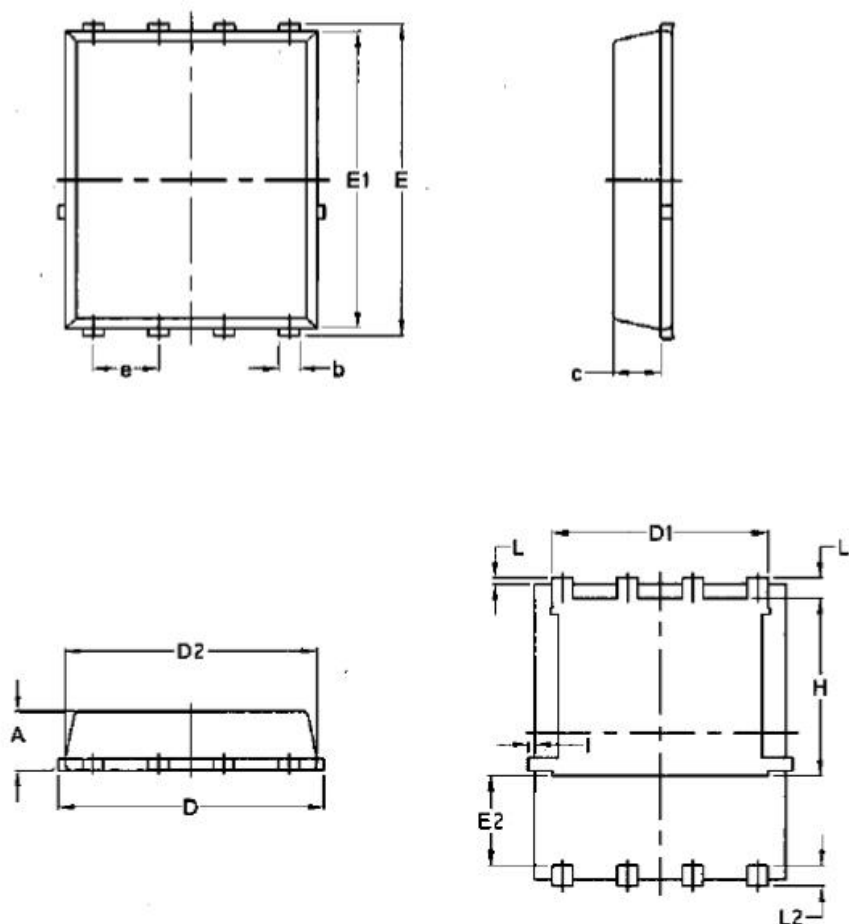


Figure.4: Diode Recovery Test Circuit & Wave form

Package Dimensions PDFN5*6-8L


Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070



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