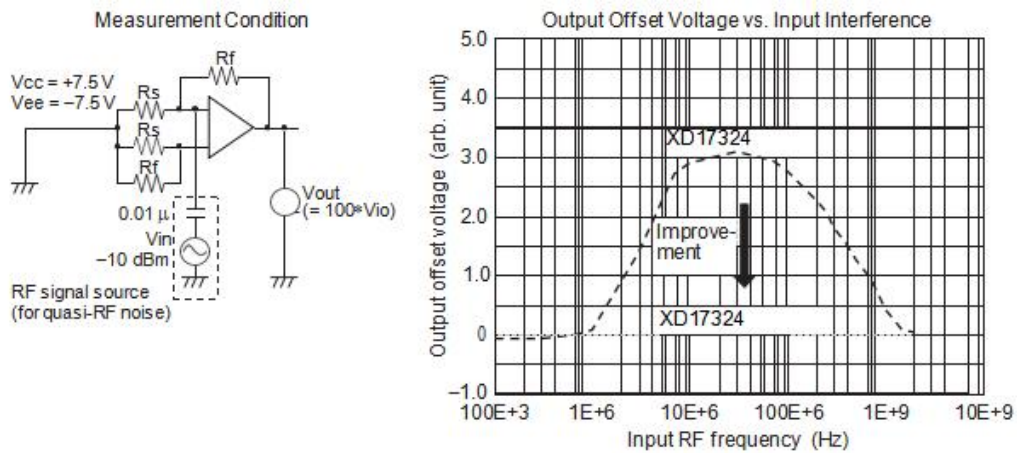


1. DESCRIPTION

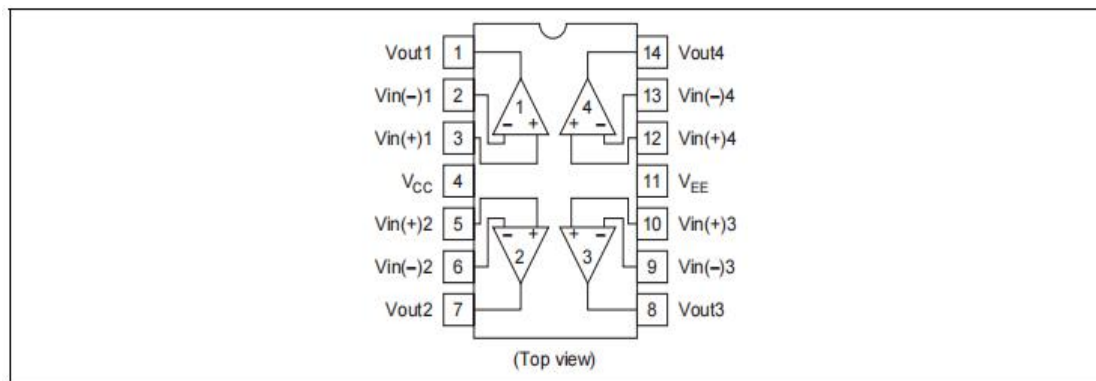
XD17324 are quad operational amplifier that provide high gain and internal phase compensation, with single power supply. They can be widely used to control equipments.

2. FEATURES

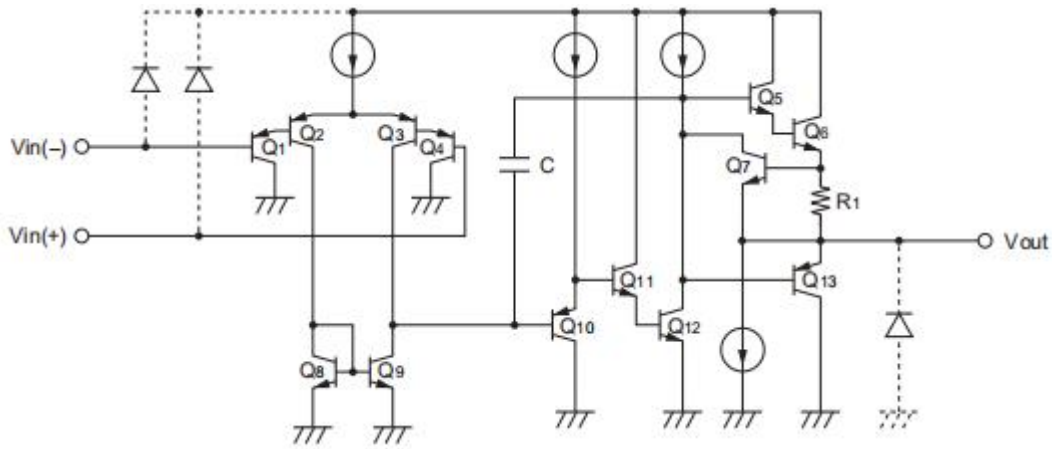
- Wide range of supply voltage, and single power supply used
- Internal phase compensation
- Wide range of common mode voltage, and possible to operate with an input about 0 V
- Low electro-magnetic susceptibility level



3. PIN ARRANGEMENT



4. CIRCUIT SCHEMATIC



Note: If Input/Output terminals voltage over the absolute maximum ratings, there is possibility of mis-operation, characteristics deterioration and destruction, because of the current's flowing to parasitic diode in IC.

The Input/Output terminals are recommended to be protected with the clamp circuit which using the diode with low forward voltage (like schottky barrier diode) when there is a possibility for the Input/Output terminals voltage exceeds the absolute maximum ratings.

5. ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Power supply voltage	VCC	32	V
Output sink current	Iosink	50	mA
Common mode input voltage	VCM	-0.3 to +VCC	V
Differential input voltage	Vin(diff)	±VCC	V
Output voltage	Vout	-0.3 to +VCC	V
Allowable power dissipation	DIP	PT	625 *2
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-55 to +125	°C

Notes: XD17324, This is the allowable values up to Ta = 50°C. Derate by 8.3 mW/°C.

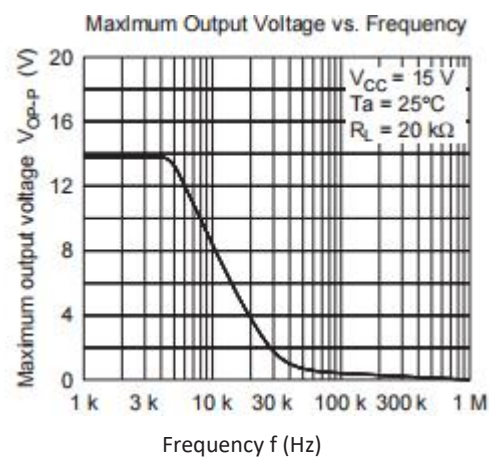
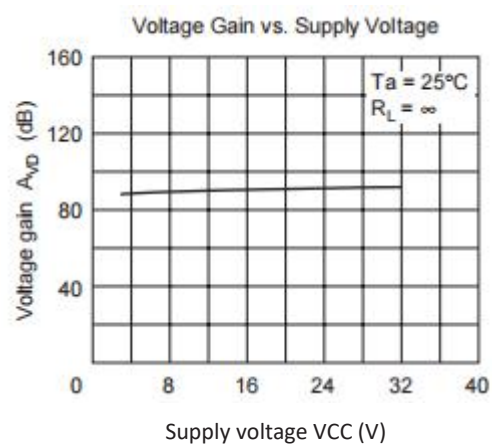
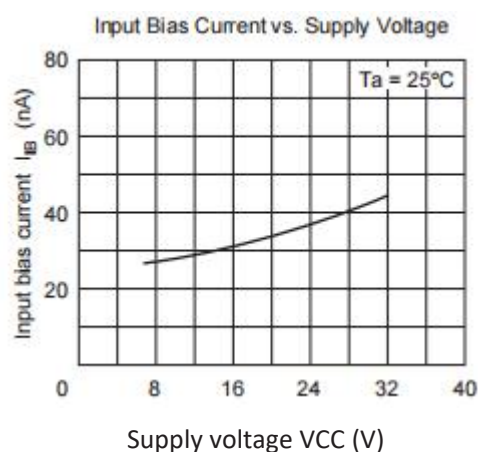
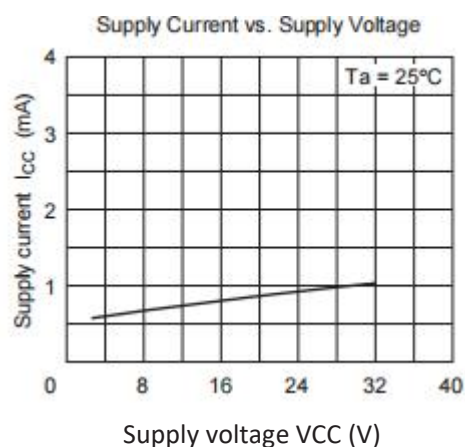
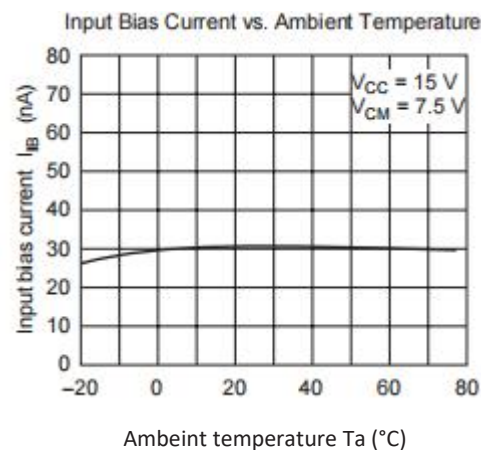
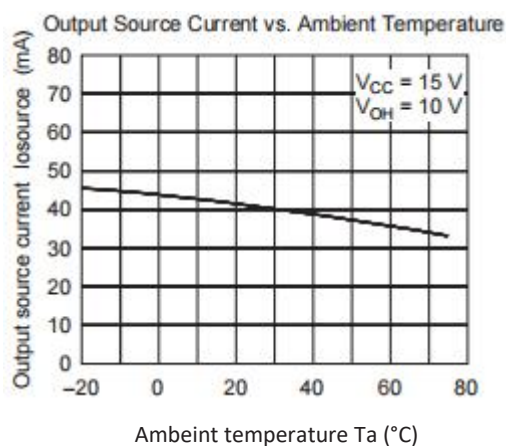
6. ELECTRICAL CHARACTERISTICS

($V_{CC} = +15\text{ V}$, $T_a = 25^\circ\text{C}$)

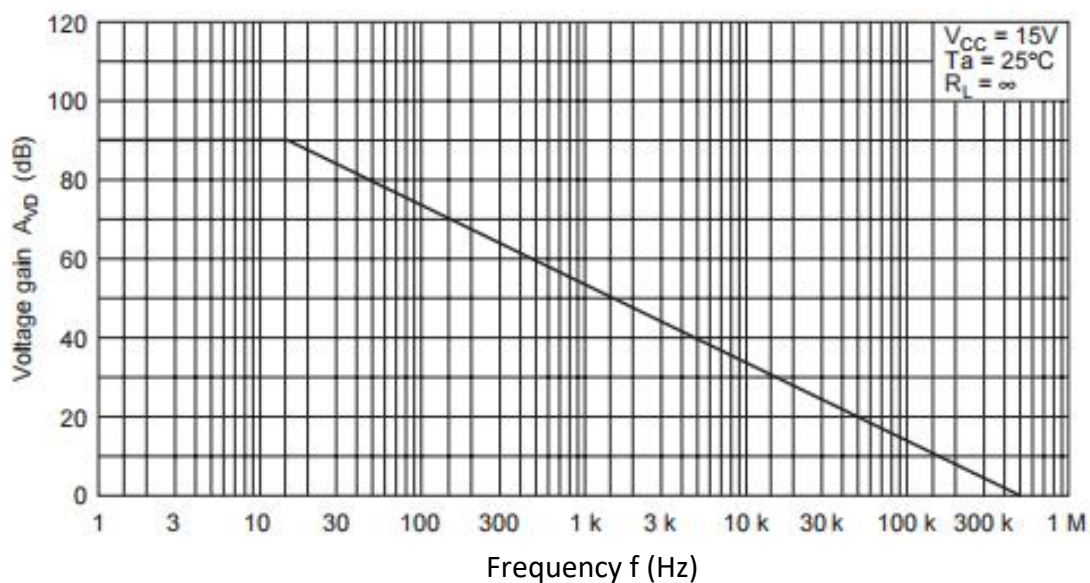
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input offset voltage	VIO		2	7	mV	$V_{CM} = 7.5\text{ V}$, $R_S = 50\ \Omega$, $R_f = 50\text{ k}\Omega$
Input offset current	IIO		5	50	nA	$V_{CM} = 7.5\text{ V}$, $I_{IO} = I_{II(-)} - I_{II(+)} $
Input bias current	IIB		30	500	nA	$V_{CM} = 7.5\text{ V}$
Power source rejection ratio	PSRR		93		dB	$f = 100\text{ Hz}$, $R_S = 1\text{ k}\Omega$, $R_j = 100\text{ k}\Omega$
Voltage gain	AVD	75	90		dB	$R_S = 1\text{ k}\Omega$, $R_f = 100\text{ k}\Omega$, $R_L = \infty$
Common mode rejection ratio	CMR		80		dB	$R_S = 50\ \Omega$, $R_f = 5\text{ k}\Omega$
Common mode input voltage range	VCM	-0.3		13.5	V	$R_S = 1\text{ k}\Omega$, $R_f = 100\text{ k}\Omega$, $f = 100\text{ Hz}$
Maximum output voltage	VOP-P		13.6		V	$f = 100\text{ Hz}$, $R_S = 1\text{ k}\Omega$, $R_f = 100\text{ k}\Omega$, $R_L = 20\text{ k}\Omega$
Output source current	Iosource	20	40		mA	$V_{IN+} = 1\text{ V}$, $V_{IN-} = 0\text{ V}$, $V_{OH} = 10\text{ V}$
Output sink current	Iosink	10	20		mA	$V_{IN} = 0\text{ V}$, $V_{IN} = 1\text{ V}$, $V_{OL} = 2.5\text{ V}$
Supply current	ICC		0.8	2	mA	$V_{IN} = \text{GND}$, $R_L = \infty$
Slew rate	SR		0.19		V/ μs	$f = 1.5\text{ kHz}$, $V_{CM} = 7.5\text{ V}$, $R_L = \infty$
Channel separation *1	CS		(120)		dB	$f = 1\text{ kHz}$
Output sink current	Iosink	15	50		μA	$V_{IN+} = 0\text{ V}$, $V_{IN-} = 1\text{ V}$, $V_{OL} = 200\text{ mV}$
		3	9		mA	$V_{IN+} = 0\text{ V}$, $V_{IN-} = 1\text{ V}$, $V_{OL} = 1\text{ V}$
Output voltage	VOH1	13.2	13.6		V	$I_{OH} = -1\text{ mA}$
	VOH2	12.0	13.3		V	$I_{OH} = -10\text{ mA}$
Output voltage	VOL1		0.8	1.0	V	$I_{OL} = 1\text{ mA}$
	VOL2		1.1	1.8	V	$I_{OL} = 10\text{ mA}$

Note: 1. Design spec.

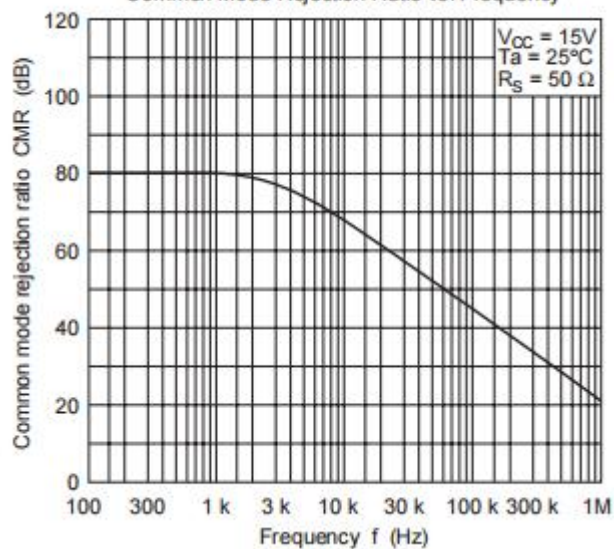
7. CHARACTERISTIC CURVES



Voltage Gain vs. Frequency



Common Mode Rejection Ratio vs. Frequency

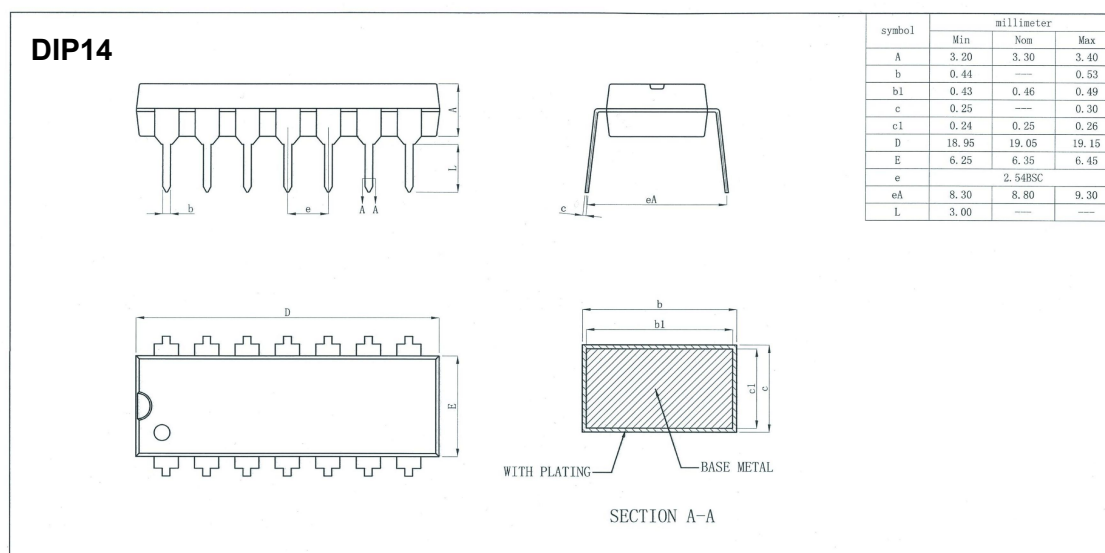


8. ORDERING INFORMATION

Ordering Information

part Number	Device Marking	Package type	Body size (mm)	Temperature (°C)	MSL	Transport	Package Quantit
XD17324	XD17324	DIP14	19.05*6.35	-40 to +85	MSL3	Tube 25	1000

9. DIMENSIONAL DRAWINGS



[if you need help contact us. Xinluda reserves the right to change the above information without prior notice]