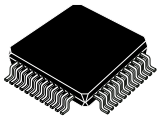
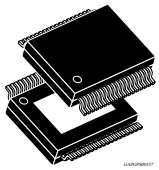
# L9305

Datasheet

## Automotive 4-channel valve driver



TQFP48 exposed pad down (7x7x1 mm)



PowerSSO36 exposed pad down

| Product status link |
|---|
| L9305 |

| Product summary | |
|---|---|
| **Order code** | **L9305EP** |
| **Package** | PowerSSO36 |
| **Packing** | Tube |
| **Order code** | **L9305EP-TR** |
| **Package** | PowerSSO36 |
| **Packing** | Tape and reel |
| **Order code** | **L9305QFP** |
| **Package** | TQFP48 |
| **Packing** | Tray |
| **Order code** | **L9305QFP-TR** |
| **Package** | TQFP48 |
| **Packing** | Tape and reel |

## Features

- AEC-Q100 qualified
- 4-channel independent LSD/HSD current controlled drivers
  - Integrated current sense path
  - Current accuracy (in normal range)
    - ± 5 mA in 0 to 0.5 A range
    - ± 1% in 0.5 A to 1.5 A range
  - Current accuracy (in extended range)
    - ± 15 mA in 0 to 0.3 A range
    - ± 5% in 0.3 A to 0.5 A range
    - ± 4% in 0.5 A to 2 A range
  - Max driver $R_{DSON}$ 375 mΩ @ 175 °C
  - 13-bit current set-point resolution
  - Variable and fixed frequency current control
  - Programmable dither function
  - Selectable driver slew rate control
- Safety features
  - High side fail safe ENABLE switch pre-driver with VDS monitoring
  - Redundant safe enable path
  - Advanced diagnosis and monitoring using BIST
  - Temperature sensor and monitoring
  - Redundant current sensing for all channels
  - Calibration & configuration memory including CRC
  - Secure serial communications using address feedback, 5-bit CRC, frame counter & long/short frame detection
  - Register verification
- 32-bit SPI communications with 5-bit CRC message verification
- Package options: PWSSO36, TQFP48
- Full ISO26262 compliant, ASIL-D systems ready

## Description

The L9305 is a configurable, monolithic solenoid driver IC designed for the control of linear solenoids for automatic transmission, electronic stability control, and active suspension applications. The four channels can be configured as either low side or high side drivers in any combination. The device includes the power transistor, recirculation transistor and current sensing for both the power and recirculation transistor. This architecture guarantees redundancy of the current measurement for each channel.

The regulated current is programmable in the range of 0-1.5 A (normal range), with a resolution of 0.25 mA, or 0-2 A (extended range), with a resolution of 0.33 mA. The user can superimpose configurable dither modulation over the set point current.

A 32-bit CRC protected SPI interface is used for configuration and control of all channels and provides status feedback of all diagnostic functions. An active low reset input, RESN, is used to disable all channels and resets internal registers to their default values. A safe enable path is provided through the EN_DR pin and the integrated Fail Safe Pre-driver. An isolated redundant safety switch-off path ensures that critical internal faults disable the fail safe pre-driver. An active high enable pin, EN_DR, is used to enable or disable the operation of all channels. When the EN_DR pin is low, all channels are disabled. A fault output pin is provided and can be used to generate an external interrupt to the microcontroller whenever a fault is detected. The user can map specific faults to the FAULTn pin based on their specific system requirements.

# 1 Block diagram

Figure 1. **Block diagram**

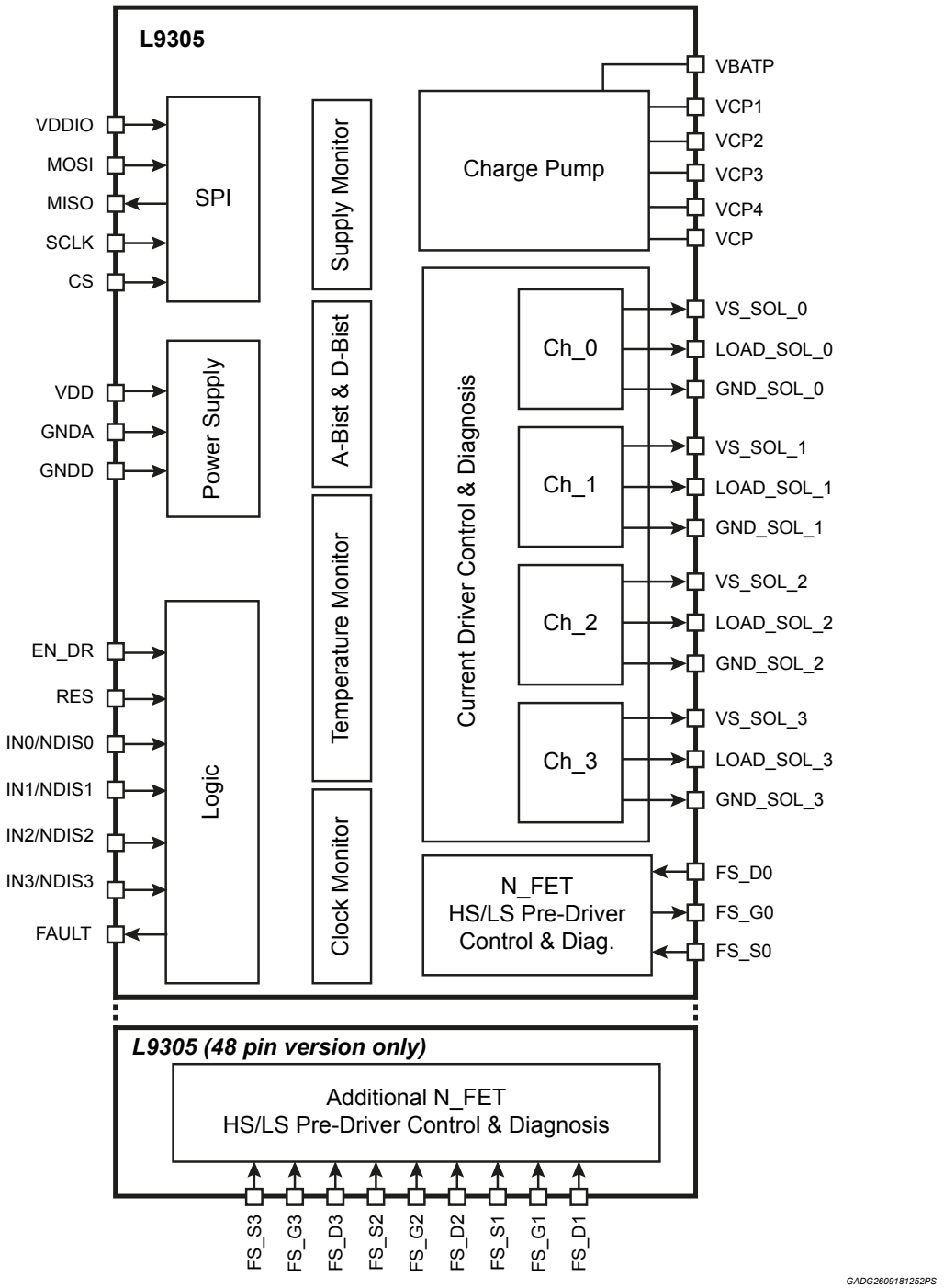


Figure 2. **PWSSO36 application schematic**

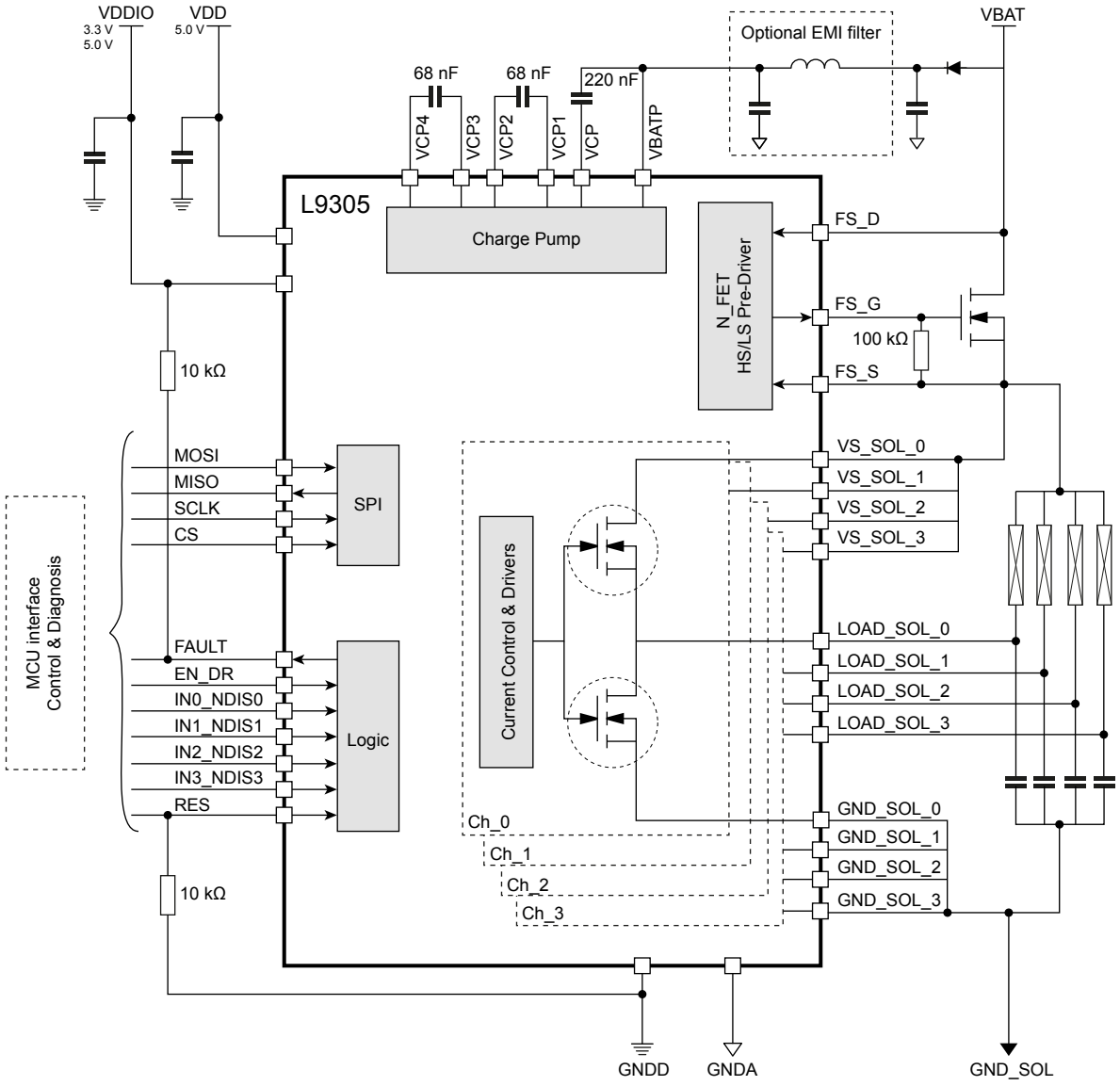
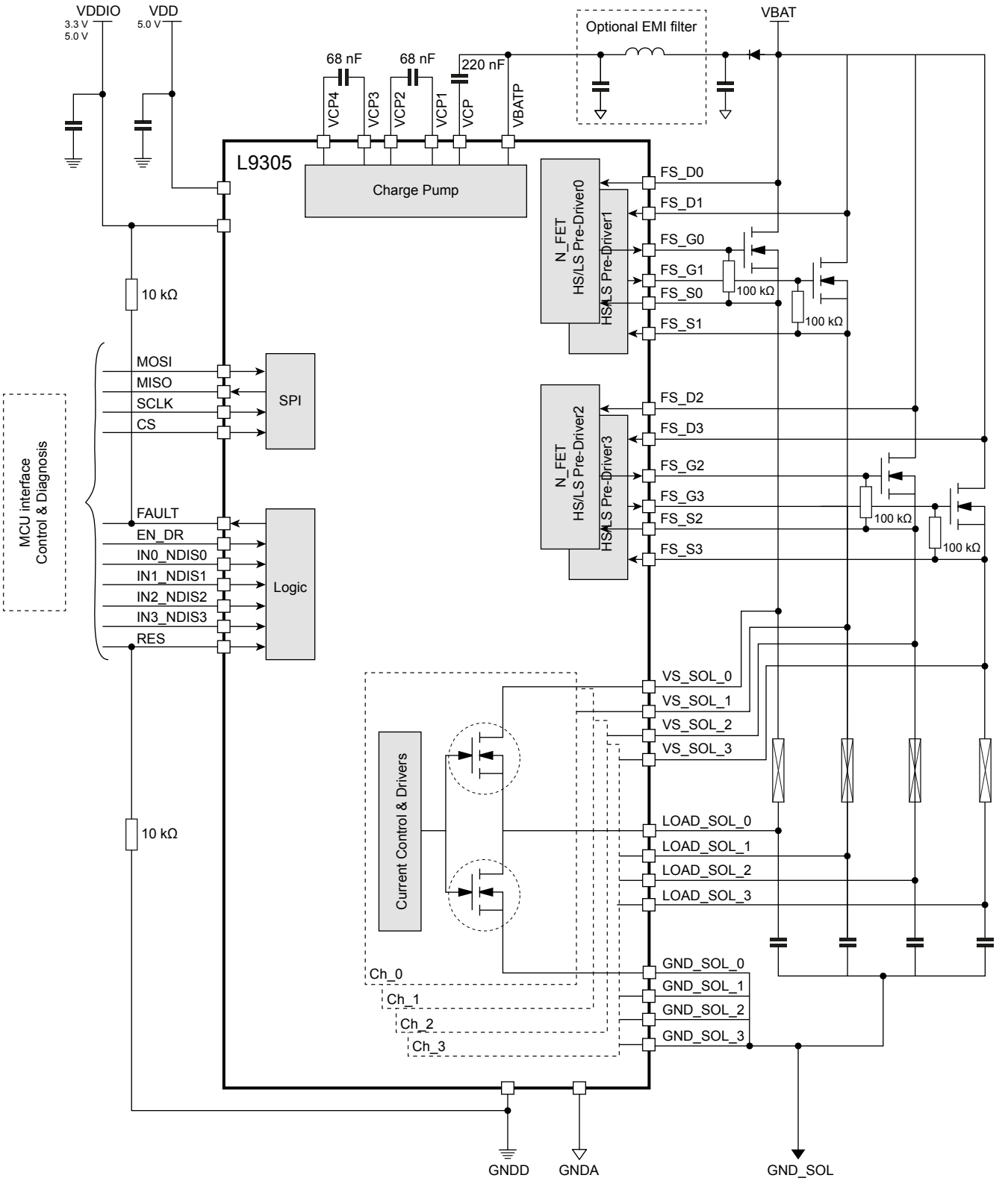


Figure 3. **TQFP48 application schematic**



# 2 Pins description

Figure 4. **PowerSSO-36 pinout diagram**

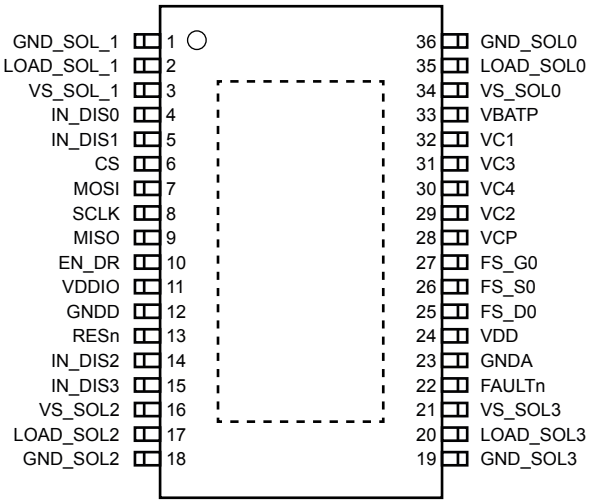



Figure 5. **TQFP48 pinout diagram**

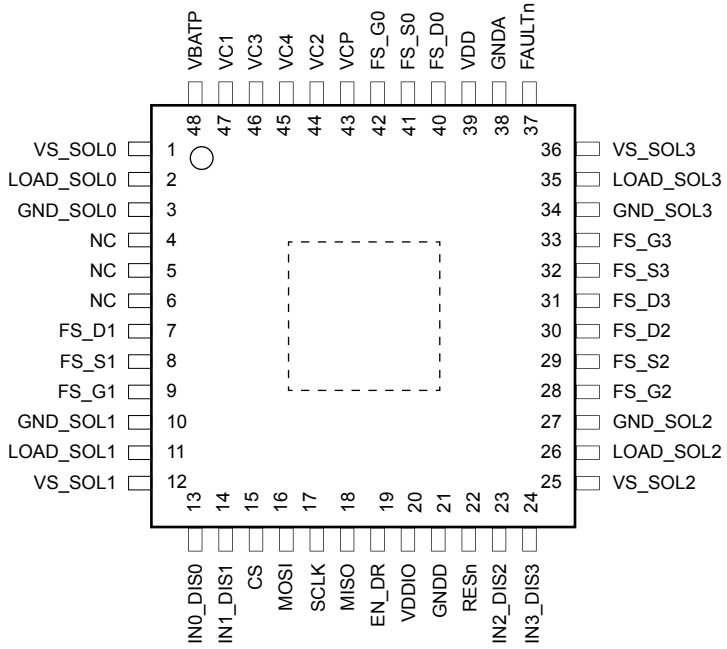


**Table 1. PowerSSO-36 and TQFP48 pins list**

| Pin number PowerSSO-36 | Pin number TQFP48 | Symbol | Function |
|---|---|---|---|
| 1 | 10 | GND_SOL1 | Channel 1 Ground: Ground connection for channel 1 power stage. |
| 2 | 11 | LOAD_SOL1 | Channel 1 Output |
| 3 | 12 | VS_SOL1 | Channel 1 Supply Voltage: Connect to Switched Battery Voltage with reverse protection diode |
| 4 | 13 | IN_DIS0 | Parallel Input Channel 0: Input for direct control from external MCU when in SW Mode; Disable channel command when in SW mode |
| 5 | 14 | IN_DIS1 | Parallel Input Channel 1: Input for direct control from external MCU when in SW Mode; Disable channel command when in SW mode |
| 6 | 15 | CS | SPI Chip Select Input: SPI communication protocol Chip Select from MCU to the device. Digital logic level: 5.0V or 3.3V |
| 7 | 16 | MOSI | SPI Data Input: SPI communication protocol input from MCU to the device. Digital logic level: 5.0V or 3.3V |
| 8 | 17 | SCLK | SPI Clock Input: SPI communication protocol clock from MCU to the device. Digital logic level: 5.0V or 3.3V |
| 9 | 18 | MISO | SPI Data Output: SPI communication protocol output to MCU from the device. Digital logic level: 5.0V or 3.3V |
| 10 | 19 | EN_DR | Enable Driver: |
| 11 | 20 | VDDIO | IO Supply: To be connected to 5.0V or 3.3V |
| 12 | 21 | GNDD | Digital Ground: Ground for digital circuits |
| 13 | 22 | RESn | Reset: when HIGH, device out of reset, when LOW, device in reset state |
| 14 | 23 | IN_DIS2 | Parallel Input Channel 2: Input for direct control from external MCU when in SW Mode; Disable channel command when in SW mode |
| 15 | 24 | IN_DIS3 | Parallel Input Channel 3: Input for direct control from external MCU when in SW Mode; Disable channel command when in SW mode |
| 16 | 25 | VS_SOL2 | Channel 2 Supply Voltage: Connect to Switched Battery Voltage with reverse protection diode |
| 17 | 26 | LOAD_SOL2 | Channel 2 Output |
| 18 | 27 | GND_SOL2 | Channel 2 Ground: Ground connection for channel 2 power stage. |
| 19 | 34 | GND_SOL3 | Channel 3 Ground: Ground connection for channel 3 power stage. |
| 20 | 35 | LOAD_SOL3 | Channel 3 Output |
| 21 | 36 | VS_SOL3 | Channel 3 Supply Voltage: Connect to Switched Battery Voltage with reverse protection diode |
| 22 | 37 | FAULTn | Fault: when LOW, Fault present, when HIGH, no fault present |
| 23 | 38 | GNDA | Analog Ground: Ground for analog circuits |
| 24 | 39 | VDD | Supply Voltage: Supply for circuits. Connect to 5.0V supply voltage |
| 25 | 40 | FS_D0 | Fail Safe Drain: to be connected to external FET Drain used as FS. VDS monitor |
| 26 | 41 | FS_S0 | Fail Safe Source: to be connected to external FET Source used as FS. VDS monitor |
| 27 | 42 | FS_G0 | Fail Safe Gate: Gate command for external FET Drain used as FS |
| 28 | 43 | VCP | Charge Pump Voltage: Connected to Protected Battery Voltage through External Capacitor |
| 29 | 44 | VC2 | Charge Pump: External Capacitor connection |
| 30 | 45 | VC4 | Charge Pump: External Capacitor connection |
| 31 | 46 | VC3 | Charge Pump: External Capacitor connection |

| Pin number PowerSSO-36 | Pin number TQFP48 | Symbol | Function |
|---|---|---|---|
| 32 | 47 | VC1 | Charge Pump: External Capacitor connection |
| 33 | 48 | VBATP | Supply Voltage: Connected to Protected Battery Voltage (reverse protection diode and filter against EMC) |
| 34 | 1 | VS_SOL0 | Channel 0 Supply Voltage: Connect to Switched Battery Voltage with reverse protection diode |
| 35 | 2 | LOAD_SOL0 | Channel 0 Output |
| 36 | 3 | GND_SOL0 | Channel 0 Ground: Ground connection for channel 0 power stage. |
| – | – | – | Available on TQFP-48 version only |
| – | 9 | FS_G_1 | Fail Safe Gate: Gate command for external FET Drain used as FS |
| – | 8 | FS_S_1 | Fail Safe Source: to be connected to external FET Source used as FS. VDS monitor |
| – | 7 | FS_D_1 | Fail Safe Drain: to be connected to external FET Drain used as FS. VDS monitor |
| – | 6 | NC | Not Used: To be connected to GND. |
| – | 5 | NC | Not Used: To be connected to GND. |
| – | 4 | NC | Not Used: To be connected to GND. |
| – | 28 | FS_G2 | Fail Safe Gate: Gate command for external FET Drain used as FS |
| – | 29 | FS_S2 | Fail Safe Source: to be connected to external FET Source used as FS. VDS monitor |
| – | 30 | FS_D2 | Fail Safe Drain: to be connected to external FET Drain used as FS. VDS monitor |
| – | 31 | FS_D3 | Fail Safe Drain: to be connected to external FET Drain used as FS. VDS monitor |
| – | 32 | FS_S3 | Fail Safe Source: to be connected to external FET Source used as FS. VDS monitor |
| – | 33 | FS_G_3 | Fail Safe Gate: Gate command for external FET Drain used as FS |

# 3 Product Characteristics

## 3.1 Absolute maximum ratings

This part may be irreparably damaged if taken outside the values specified in the next table. Operation above the absolute maximum ratings may also cause a decrease in reliability. The operating junction temperature range is from -40 °C to +175 °C. The maximum junction temperature must not be exceeded. All voltages are with respect to analog ground pin GNDA.

**Table 2. Absolute maximum ratings**

| Pin name | Type | Test condition | Min | Typ | Max | Unit | Pin type |
|---|---|---|---|---|---|---|---|
| VBATP | Global | | -0.3 | – | 40 | V | S |
| VCP | Local | Note: VCP-VBATP<13V, VBATP-VCP<0.3V | -0.3 | – | 50 | V | S |
| VC1, VC3 | Local | Note: VCx-VBATP<0.3V | -0.3 | – | 40 | V | O |
| VC2, VC4 | Local | Note: VCx-VBATP<13V VBATP-VCx<0.3V | -0.3 | – | 50 | V | O |
| VS_SOLx | Global | | -0.3 | – | 40(1) | V | S |
| LOAD_SOLx | Global | | -0.3 | – | 40(1) | V | O |
| GND_SOLx | Local | | -0.3 | – | 0.3 | V | I |
| VDD | Local | | -0.3 | – | 19 | V | S |
| VDDIO | Local | | -0.3 | – | 19 | V | S |
| GNDD | Local | | -0.3 | – | 0.3 | V | S |
| FS_D0 | Global | | -0.3 | – | 40 | V | I |
| FS_G0 | Local | Internally shorted to FS_S0 (off phase) Note: FS_G0-FS_S0<13V | -2(2) | – | 50 | V | O |
| FS_S0 | Global | Note: FS_S0-FS_G0<0.3V | -2 | – | 50 | V | O |
| CS, SCLK, MOSI, EN_DR, RESn, INx_DISx | Local | | -0.3 | – | 19 | V | I |
| MISO, FAULTn | Local | | -0.3 | – | 19 | V | O |

1. *35V AMR over life-time, 40V for ISO-pulse transients (as defined in ISO7637-2 standard).*
2. *biased condition, -0.3V for unbiased conditions/sleep mode.*

## 3.2 Latchup trials

Latch-up tests performed according to JEDEC 78 class 2 Level A

## 3.3 ESD performance

**Table 3. ESD Performance**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| ESD HBM | HBM Global pins | ESD according to Human Body Model (HBM), Q100-002 for all pins; (100pF/1,5kΩ) | -4 | – | 4 | kV | Global |
| ESD HBM | HBM all pins | ESD according to Human Body Model (HBM), Q100-002 for all pins; (100pF/1,5kΩ) | -2 | – | 2 | kV | ALL |
| ESD CDM Corner | CDM corner pins | ESD according to Charged Device Model (CDM), Q100-011 Corner pins | -750 | – | 750 | V | Corner |
| ESD CDM | CDM all pins | ESD according to Charged Device Model (CDM), Q100-011 All pins | -500 | – | 500 | V | ALL |

## 3.4 Temperature range

**Table 4. Device operating temperature**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| $T_{amb}$ | Operating ambient temperature | | -40 | – | 135 | °C | ALL |
| $T_j$ | Junction temperature | | -40 | – | 175 | °C | ALL |
| $T_{stg}$ | Storage temperature | – | -50 | – | 175 | °C | ALL |
| $T_{pas}$ | Maximum non/operating temperature during passive lifetime | – | -55 | – | 150(1) | °C | ALL |
| $R_{Th\ j\text{-}a}$ | Thermal Resistance junction to ambient | Package: PWSSO36<br>2s2p (4L) board(2)<br>Natural convection | – | 22 | – | °C/W | ALL |
| $R_{Th\ j\text{-}c}$ | Thermal Resistance junction to case | | – | 1 | – | | |
| $R_{Th\ j\text{-}b}$ | Thermal Resistance junction to board | | – | 7 | – | | |
| $R_{Th\ j\text{-}a}$ | Thermal Resistance junction to ambient | Package: TQFP48 (E-pad: 5x5 mm)<br>2s2p (4L) board(2)<br>Natural convection | – | 27 | – | °C/W | ALL |
| $R_{Th\ j\text{-}c}$ | Thermal Resistance junction to case | | – | 2 | – | | |
| $R_{Th\ j\text{-}b}$ | Thermal Resistance junction to board | | – | 9 | – | | |

1. *175°C are allowed for limited time. Eventual Mission profiles with passive lifetime temperature >150°C have to be evaluated by ST to confirm that product qualification is able to cover the required conditions.*
2. *JESD51-7*

All parameters are guaranteed, and tested, in the temperature range from $T_j$ -40 to 150 °C (unless otherwise specified); the device is still operative and functional at higher temperatures (up to $T_j$ 175 °C). Device functionality at high temperature up to $T_j$ = 175 °C is guaranteed by bench validation, electrical parameters are guaranteed by correlation with ATE tests at reduced temperature and adjusted limits (if needed).

# 4 Input / Output

## 4.1 Reset (RESn)

The RESn pin is the reset input for the device. If the RESn pin is low, the device is held in an internal reset state, all outputs channels are disabled, the failsafe pre-drivers are disabled, the FAULTn pin is held low and all registers are reset to their default values. An internal pull down current source will hold the RESn pin low in case the pin is open. RESn pin status is echoed in each SPI frame.

## 4.2 Enable (EN_DR)

The EN_DR pin is used to enable / disable the output stages. When EN_DR pin is low, all channels are disabled, all fail safe pre-drivers are disabled and the FAULTn pin is pulled low if EN_DR is not masked. The EN_DR pin can be connected to a general purpose output pin of the microcontroller or to an alternative safety circuit.

When EN_DR pin is set high, all channels are enabled based on their configuration settings and the fail safe pre-drivers can be controlled through the Fail Safe Configuration Register.

## 4.3 Channel inputs (INx/NDISx)

The INx/NDISx pins serve two purposes depending on the selected load control method. If the load is controlled using the internal closed loop current control circuit (referred to as Hardware Mode), INx/NDISx serves as an enable/disable signal for each channel. When in this mode, if INx/NDISx is high, output control is disabled and when low output control is enabled.

The second operating mode is referred to as Software Mode. When the device is programmed for Software Mode, the INx/NDISx pin serves as the PWM input signal to directly control the output drivers. When INx/NDISx is high, the driving transistor is enabled and the active recirculation transistor is disabled. When INx/NDISx is low, the driving transistor is disabled and the active recirculation transistor is enabled. The driving transistor and active recirculation transistor are dependent on the programmed output configuration, high side or low side. High and low side configurations are explained in Section 6: Current control drivers.

## 4.4 Fault (FAULTn)

The device sets the FAULTn pin low upon detecting internal and external faults and while the device is in reset. The FAULTn pin is open drain and requires an external pull-up resistor connected between VDDIO and the FAULTn pin. A summary of all faults linked to the state of FAULTn are shown in Table 5 and Table 6. Only faults with specified masking register bits can be masked or unmasked by the user. Faults denoted as “None” are automatically linked to FAULTn output status. In addition to the items below, RESn is not masked and is linked to the FAULTn pin by default.

**Table 5. Global and external supply fault pin error masking**

| FAULTn Masking function | Register & Data Bit |
|---|---|
| Digital Ground Loss Fault | SERVFLTMSK1, D[15] |
| Analog Ground Loss Fault | SERVFLTMSK1, D[14] |
| Fail Safe VDS Fault | SERVFLTMSK1, D[10] |
| EEPROM Trimming Data CRC Error Fault | SERVFLTMSK1, D[8] |
| SPI Timeout Latch Fault | SERVFLTMSK1, D[7] |
| SPI Timeout Fault | SERVFLTMSK1, D[6] |
| VDD Under Voltage Fault | SERVFLTMSK1, D[4] |
| VDD Over Voltage Fault | None |
| V3V3A Over Voltage | None |
| V3V3D Under Voltage | None |
| V3V3D Over Voltage | None |
| Oscillator Stuck | None |
| Oscillator Mismatch | None |

| FAULTn Masking function | Register & Data Bit |
|---|---|
| Internal Global Register Error | None |
| CP Under Voltage Fault | SERVFLTMSK1, D[3] |
| Configuration Register Mismatch Fault | SERVFLTMSK1, D[2] |
| VBATP Over Voltage Fault | SERVFLTMSK1, D[1] |
| Core Over Temperature Fault | SERVFLTMSK1, D[0] |
| SPI Protocol Error Fault | SERVFLTMSK2 D[15] |
| IN 3 Echo Fault | SERVFLTMSK2 D[4] |
| IN 2 Echo Fault | SERVFLTMSK2 D[3] |
| IN 1 Echo Fault | SERVFLTMSK2 D[2] |
| IN 0 Echo Fault | SERVFLTMSK2 D[1] |
| EN_DR Echo Fault | SERVFLTMSK2 D[0] |

**Table 6. Solenoid channel and fail safe fault pin error masking**

| FAULTn Masking function | Register & Data Bit |
|---|---|
| E_Sol_Thermal Warning | DRVFLTMSK1,D[15] |
| EEPROM CRC Error on CSA Calibration Data | DRVFLTMSK1,D[14] |
| EEPROM CRC Error on ADC Trimming Bits | DRVFLTMSK1,D[13] |
| PWM check fault | DRVFLTMSK1,D[12] |
| E_Sol_Open Load Fault | DRVFLTMSK1,D[6] |
| E_Sol_Short Fault | DRVFLTMSK1,D[5] |
| E_Sol_ADC Fault | DRVFLTMSK1,D[4] |
| E_LSCLAMP Fault | DRVFLTMSK1,D[3] |
| E_Sol_HS Over Current Fault | DRVFLTMSK1,D[2] |
| E_Sol_LS Over Current Fault | DRVFLTMSK1,D[1] |
| E_Sol Over Temperature Fault | DRVFLTMSK1,D[0] |
| Out of Regulation Fault | DRVFLTMSK2,D[4] |
| GND_SOL Loss Fault | DRVFLTMSK2,D[3] |
| E_RAM_CRC_ERR Fault | DRVFLTMSK2,D[2] |
| E_SOL_HS/LS Fault | DRVFLTMSK2,D[1] |
| E_CFG_REG_FAIL Fault | DRVFLTMSK2,D[0] |

## 4.5 SPI communications (CS, SCLK, MOSI & MISO)

The CS, SCLK, MOSI & MISO pins provide serial communications between the device and the microcontroller. Please see Section 9: SPI for details on SPI features, device register functions and electrical characteristics.

## 4.6 Input / output electrical specifications

4.75 V ≤ $V_{DD}$ ≤ 5.5 V; 5.5 ≤ $V_{BATP}$ ≤ 19 V; -40 °C ≤ $T_j$ ≤ 175 °C unless otherwise noted. All voltages refer to GNDA pin.

**Table 7. Digital input/output electrical performance**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| EN_DR_low | Logic input low detection | – | – | – | 0.75 | – | EN_DR |
| EN_DR_high | Logic Input high detection | – | 1.75 | – | – | V | EN_DR |
| EN_DR_hyst | Input hysteresis voltage | – | 0.1 | – | – | V | EN_DR |
| EN_DR_pd | Inter pull down resistance | $V_{IN}$ < 3V | 10 | 38 | 70 | kΩ | EN_DR |
| EN_DR_deglitch | EN_DR deglitch filter | Guaranteed by scan | 9 | | 12 | µs | EN_DR |
| EN_DR_test_low | Logic input low detection | – | – | – | 6 | – | EN_DR |
| EN_DR_test_high | Logic input high detection | – | 9 | – | – | V | EN_DR |
| EN_DR_test_hyst | Input hysteresis voltage | – | 0.1 | – | – | V | EN_DR |
| INx_DISx_low | Logic Input low detection | – | – | – | 0.75 | V | INx_DISx |
| INx_DISx_high | Logic input high detection | – | 1.75 | – | – | V | INx_DISx |
| INx_DISx_hyst | Input hysteresis voltage | – | 0.1 | – | – | V | INx_DISx |
| INx_DISx_pd | Inter pull down resistance | VIN < 3V | 10 | 38 | 70 | kΩ | INx_DISx |
| INx_DISx_deglitch_SW | Actuation deglitch in SW mode | Guaranteed by scan | 3 | 3.5 | 3.9 | µs | INx_DISx |
| INx_DISx_deglitch_HW | Disable deglitch in HW mode | Guaranteed by scan | 1.2 | 1.5 | 1.7 | µs | INx_DISx |
| RESn_low | Logic input low detection | – | – | – | 0.75 | – | RESn |
| RESn_high | Logic input high detection | – | 1.75 | – | – | V | RESn |
| RESn_hyst | Input hysteresis voltage | – | 0.1 | – | – | V | RESn |
| RESn_pd | Inter pull down resistance | VIN < 2.5V | 10 | 38 | 70 | kΩ | RESn |
| RESn_deglitch | RESn deglitch filter | Guaranteed by scan | 4.5 | 5 | 7 | µs | RESn |
| FAULTn_lleak | Leakage current in tri-state condition | – | – | – | 10 | – | FAULTn |
| FAULTn_low | Logic low level | Ext pull-up 4.7k to VDDIO | – | – | 0.4 | – | FAULTn |
| FAULTn_high | Logic high level | Ext pull-up 4.7k to VDDIO | VDDIO-0.4 | – | – | V | FAULTn |
| FAULTn_trise | FAULTn rise time | Ext pull-up 4.7k to VDDIO, Cload=20pF,tested by correlation | – | – | 100 | ns | FAULTn |
| FAULTn_tfall | FAULTn fall time | Ext pull-up 4.7k to VDDIO, Cload=20pF | – | – | 100 | ns | FAULTn |

# 5 Power supply

## 5.1 Overview

The L9305 has multiple supply pins. Internal circuits are powered from VDD (+5 V) and VBATP (reverse battery protected) while digital I/O pins are powered from VDDIO (3.3 V or 5 V) for consistency with the main microcontroller I/O operation. The charge pump regulator is sourced from VBATP and supplies the necessary voltage source for the high side integrated valve drivers and fail safe pre-drivers.

## 5.2 Battery supply (VBATP)

This pin is the supply for the charge pump and must be connected to the reverse polarity protected battery voltage supply. VBATP input voltage is diagnosed for over voltage conditions. The status of this diagnostic is readable by SPI. Refer to Section 8.1.2: VBATP supply over voltage for additional information. The following table summarizes the functional ranges dependent on battery supply voltage.

**Table 8. VBATP electrical performance**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VBATP operational | Normal operating voltage range(1) | $T_{amb}$ = 40 °C, 4.75 V ≤ VDD ≤ 5.5 V | 5.5 | – | 19 | V |
| | | $T_{amb}$ = 27 °C, 4.75 V ≤ VDD ≤ 5.5 V | 5.55 | – | 19 | V |
| | | $T_{amb}$ = 125 °C, 4.75 V ≤ VDD ≤ 5.5 V | 5.6 | – | 19 | V |
| VBATP double/load dump | High voltage range(2) | $T_{amb}$ ≤ 50 °C, 4.75 V ≤ VDD ≤ 5.5 V | 19 | – | 36 | V |
| VBATP over voltage | Over voltage range(3) | $T_{amb}$ ≤ 50 °C, 4.75 V ≤ VDD ≤ 5.5 V | 36 | – | 40 | V |
| VBATP low voltage | Low Voltage Range Cranking(4) | $T_{amb}$ = -40 °C, 4.75 V ≤ VDD ≤ 5.5 V | – | – | 5.5 | V |
| | | $T_{amb}$ = 27 °C, 4.75 V ≤ VDD ≤ 5.5 V | – | – | 5.55 | V |
| | | $T_{amb}$ = 125 °C, 4.75 V ≤ VDD ≤ 5.5 V | – | – | 5.6 | V |

1. *Device is capable of full functional operation; VBATP must be reversed battery protected*
2. *Device is capable of full functional operation at Ta ≤ 50 °C with possible degradation of electrical parameters linked to battery line (ex. solenoid slew rate control and current regulation accuracy); There will be no damage to the device, no false operation and input pins will withstand voltage and current defined in Absolute ratings regardless of battery voltage range. Full functional operation will resume without operator intervention when battery voltage returns to Normal Operating Voltage Range at Ta ≤ 50 °C.*
3. *Ta ≤ 50 °C, duration less than 500 ms. There will be no damage to the device, Solenoid channels and Fail Safe switch will be disabled and input pins will withstand voltages and currents defined in Absolute ratings regardless of battery voltage range. Full functional operation will resume with operator intervention, as described in the specification, when battery voltage returns to normal operating voltage range.*
4. *Device is capable of full functional operation until charge pump is out of under voltage condition with possible degradation of electrical parameters linked to battery line (ex. solenoid slew rate control and current regulation accuracy). Full functional operation will resume without operator intervention when battery voltage returns to normal operating voltage range.*

## 5.3 Load supplies (VSOL1, VSOL2, VSOL3 & VSOL4)

The VSOLx pins are connected to the high side of the solenoid load when the output drivers are configured for low side operation. In low side operation, VSOLx provides power to the load and recirculation path through the high side driver. When the output drivers are configured for high side operation, the VSOLx pin becomes the power source for driving the load thru the high side solenoid driver transistor. In this case, load current is recirculated through the corresponding low side driver. VSOLx pins are independent for each solenoid driver channel. Solenoid driver operation and configuration are detailed in Section 6.4: Solenoid driver and load diagnostic.

## 5.4 Analog and digital supply (VDD)

The VDD pin provides the source voltage for all internal analog (V3V3A) and digital (V3V3D) circuits. An internal start-up circuit connected to VDD initializes the internal regulators (V3V3A & V3V3D) once VDD reaches VDD_UV threshold. V3V3A & V3V3D regulators are monitored for internal power on reset control (POR). VDD input voltage is diagnosed for over and under voltage conditions. The status of this diagnostic is readable by SPI. Please see Section 8.1.1: VDD over and under voltage diagnostics.

## 5.5 I/O supply (VDDIO)

VDDIO is the supply for all pins that interface with the external microcontroller. This pin must be connected to a supply with the same voltage used by the microcontroller I/O, 3.3 V or 5.0 V. There is no monitoring function associated with VDDIO.

## 5.6 Power-On reset

An internal power on reset circuit holds the device in a reset state if VDD goes below the under voltage threshold. The power on reset is released once VDD is within normal operating range for the specified reset filter time TPOR. The SPI interface can be accessed after the power on reset time.

The fault bit “POR_flag” in the SERVFLT1 register is set, when the device exits the reset state. This bit is cleared automatically, whenever the SERVFLT1 register is accessed. Also RES_echo in PINSTATUS register is set, when the device exits the reset state in case of Power-On reset event, despite the state of RESn pin. The microcontroller can use these bits to determine if an internal or external reset has occurred.

A power on reset (POR) can also occur if any of the internal bandgap regulators or internal analog & digital regulators are diagnosed as over or under voltage. Additional details on these and VDD monitoring can be found in sections Section 8.1.1 and Section 8.1.4.

## 5.7 GND (GNDD, GNDA, GND_SOLx)

The L9305 has two low power ground connections, GNDD and GNDA. These connections are for internal analog and digital control circuits. Exposed pad is connected to substrate and to GNDA. GNDD and GNDA are connected through a pair of anti-parallel ESD diodes. The device has 4 power ground connections, GND_SOL0, GND_SOL1, GND_SOL2 and GND_SOL3. All ground pins have open circuit detection. Additional details on ground loss detection are shown in Section 8.1.5: GND loss detection .

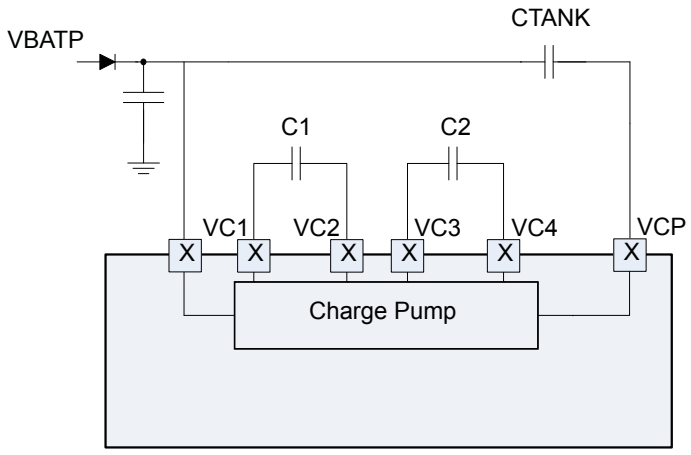
## 5.8 Charge pump

To effectively bias the high side solenoid drivers and fail safe switch, a charge pump is used to drive the gate voltage above VBATP. The device uses a common charge pump for all channels and is referred to the battery voltage supply connected to the VBATP pin. The charge pump output voltage is present at the VCP pin. The charge pump switching frequency is nominally 470 kHz and its internal control loop reduces emissions by pulse skipping once the targeted operating voltage is reached.

The charge pump circuit requires three external capacitors. A “Tank” capacitor with a recommended value of 220 nF must be connected between the VCP pin and the VBATP pin. Two pump capacitors with recommended values of 68 nF must be connected between the VCP1 and VCP2 pins and also between the VCP3 and VCP4 pins. A built-in monitoring circuit checks if the charge pump output voltage is sufficient to control the high side valve driver. Additional details for charge pump voltage monitoring are shown in Section 8.1.3: VCP supply under voltage.

The charge pump voltage is also used as parallel supply to the VDD supply for internal references to avoid ASIC reset at low VDD input.

Figure 6. **Charge pump mechanization**

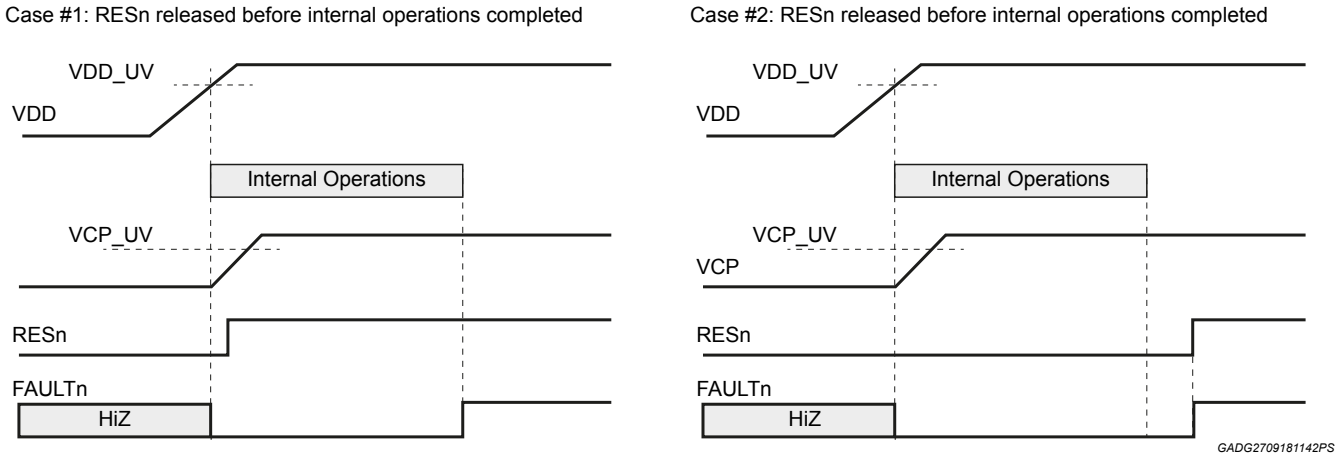



## 5.9 Startup & power down sequence

L9305 begins initialization and execution of all internal diagnostic and self-test functions upon VDD reaching the VDD_UV threshold. A detailed list of these monitoring functions is summarized in Section 8: Safety features . While the device is initializing, the FAULTn pin remains low. Upon completing initialization, the SPI POR flag is set high (clear on read) to indicate a POR event has occurred and the FAULTn pin remains low until the RESn input is set high. The RESn input can be set high prior to the device completing initialization but the FAULTn pin will not be released until the POR event is complete. This sequence is shown in Figure 7. Also RES_echo in PINSTATUS register is set, when the device exits the reset state in case of Power-On reset event, despite the state of RESn pin.

Once the POR event is complete and the RESn input is set high, the device can be configured by the user. All registers maintain RESET default states until both POR is set high and RESn is set by the user.

Figure 7. **Startup procedure example**




L9305 power down sequence requires only the VDD supply be disabled. Once the VDD_UV threshold is reached, the solenoid and fail safe pre-driver outputs are disabled. There are no timing dependencies between VDD and VBATP voltage levels to perform the power down sequence.

## 5.10 Power supply electrical specifications

4.75V ≤ VDD ≤ 5.5V; 5.5 ≤ VBATP ≤ 19V; -40°C ≤ Tj ≤ 175°C unless otherwise noted. All voltages refer to GNDA pin.

**Table 9. Power supply electrical performance**

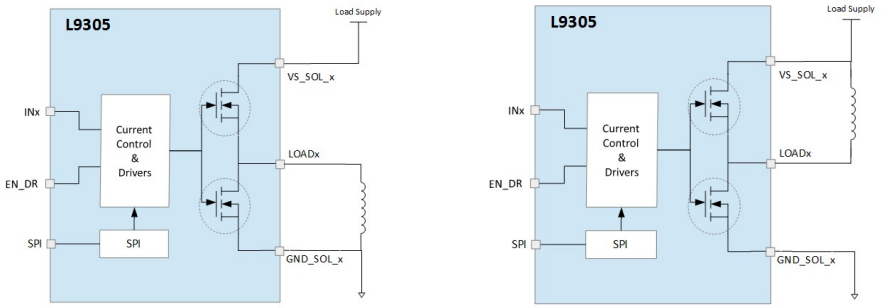
| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| POR_deglitch | POR analog deglitch | | 10 | 18 | 30 | µs | POR |
| VBATP_stby_cur | VBATP stby current consumption | VDD = 0 V, VBATP = 13 V | – | – | 45 | µA | VBATP |
| VDD_stby_cur | VDD stby current consumption | VDD < 0.3 V | – | – | 1 | µA | VDD |
| VBATP_on_state_cur | VBATP on state current consumption | VDD = 5 V, VBATP = 13 V, All channels tristated | 5 | 10 | 20 | mA | VBATP |
| VDD_on_state_cur | VDD on state current consumption | VDD = 5 V | 20 | 30 | 40 | mA | VDD |
| VDDIO_stby_curr | VDDIO stby current consumption | VDD = 0 V, VDDIO = 5 V | -1 | – | 1 | µA | VDDIO |
| VDDIO_on_state_curr | VDDIO on state current consumption | VDD = 5 V, VDDIO = 5 V | – | – | 5 | mA | VDDIO |
| V3V3A | Internal analog supply line | Design info, not tested | – | 3.3 | – | V | V3V3A |
| V3V3D | Internal digital supply line | Design info, not tested | – | 3.3 | – | V | V3V3D |
| fosc_main | Main oscillator frequency | – | -5% | 16 | 5% | MHz | fosc |
| fosc_aux | Auxiliary oscillator frequency | – | -5% | 16 | 5% | MHz | fosc_aux |
| fosc_mod_freq | Spread spectrum modulation frequency | Design info, not tested | – | 125 | – | kHz | fosc, fosc_aux |
| fosc_mod_index_min | Spread spectrum minimum modulation index | Guaranteed by scan | -5 | – | -2 | % | fosc, fosc_aux |
| fosc_mod_index_max | Spread spectrum maximum modulation index | Guaranteed by scan | 2 | – | 5 | % | fosc, fosc_aux |
| VCP_start | CP initialization time | VBATP = 13 V, CP from VBATP to VBATP+7 V | – | – | 1 | ms | CP |
| tasic_init | Initialization time of ASIC | Time from VDD rising to FAULTn release, RESn HIGH | – | – | 5 | ms | VDD, FAULTN |
| CP_freq | Charge pump frequency | – | fosc/34 | 470 | fosc/34 | kHz | Cx |
| VCP_out | CP target output voltage | Design info, not tested | – | VBATP+9 | – | V | CP |
| VCP_out_min | Minimum charge pump output voltage | $I_{load}$ = 10 mA, solenoid channels tri-stated, FS disabled, VBATP = 5.5 V | VBATP+7 | – | – | V | CP |
| VDDIO | Io voltage | – | 3.3 | – | 5 | V | VDDIO |
| VDD | Power supply | – | 4.75 | – | 5.25 | V | VDD |

# 6 Current control drivers

The L9305 provides four independent current control channels. Each channel includes the Driver Control Block, Analog Current Measurement Block and Output Stage. The Output Stage consists of a driving transistor and the recirculation transistor and is user configurable for high side or low side control. When configured as a low side driver, the high side driver recirculates load current. When configured as a high side driver, the low side driver recirculates load current. Configuration examples are shown in Figure 8 and Section 6: Current control drivers.

Both high and low side paths have independent current sense circuits to ensure accurate current control in either configuration. The high or low side configuration is selected in register, Channelx_CONFIGURATION1, D[3]. The device defaults to low side configuration.

**Figure 8. HS driver (left) and LS driver (right) configuration**




GADG2709181147PS

Calibration and trim data are stored in internal $E^2$PROM memory and are used to optimize current control performance. Upon power on reset, the device transfers calibration and trim data into local RAM for use in the Driver Control and Current Measurement blocks. These data are verified using CRC checks, please see Section 8.4.4 for more details.

Load current can be controlled using the internal closed loop control circuits or directly by the microcontroller as summarized below.

- Hardware current control
  - Current Set Point and Switching frequency are programmed through SPI registers
  - Device automatically adjusts the PWM Duty cycle to maintain the programmed load current
- Software current control
  - Current Set Point and Switching frequency are managed directly by the microcontroller
  - L9305 provides average current feedback through SPI and acts only as load driver

Current control configuration and setup are programmed through the SPI interface. Configuration registers (Channel_x. CONFIGURATION 1 and Channel_x.CONFIGURATION2) can only be modified when the channel is not enabled (SOLENDR).

## 6.1 Hardware current control

Each channel has four operating states, Disabled, Tristate, PWM and Full on. These operating states are dependent on internal registers settings, SOLENDR register, bit D[7:0] and EN_DR and INxDISx input pins. A summary of these settings is shown below. Please note the SOLENDR register assigns 2 bits per channel to select driver operating state, therefore the table below shows only two bits.

**Table 10. Solenoid driver status in hardware mode**

| EN_DR | INx | Driver Configuration Status | | Channel Status |
|---|---|---|---|---|
| | | [1] | [0] | |
| LOW | X | X | X | Driver Disabled, Off Diagnosis disabled and Masked |
| HIGH | HIGH | X | X | |
| HIGH | LOW | 0 | 0 | |
| HIGH | LOW | 0 | 1 | Driver in Tristate, Off diagnosis can be switched on |
| HIGH | LOW | 1 | 0 | Driver ON in PWM mode,Off Diagnosis disabled and Masked |
| HIGH | LOW | 1 | 1 | Driver ON in Full ON mode,Off Diagnosis disabled and Masked |

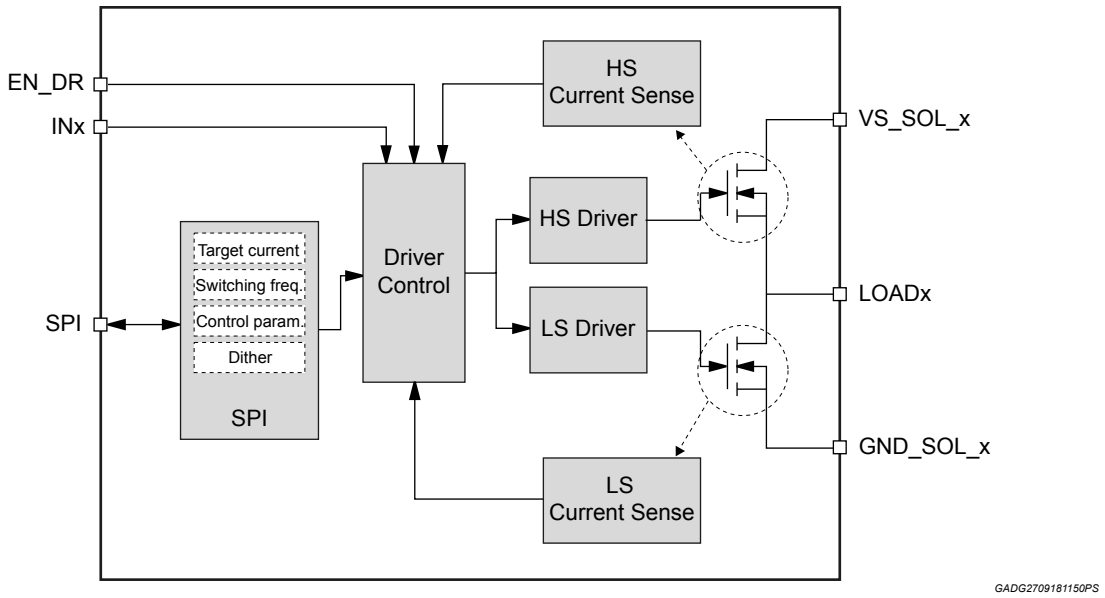
Disabled Mode: Output drivers are disabled, no bias is present on the driver, off-state diagnostics are masked and cannot be enabled; LS clamp feature is inactive, thus, if an overvoltage occurs when driver is disabled, low side mos will not be protected

Tristate Mode: Driver is supplied and kept in a tristate high impedance mode, off state diagnostics can be enabled

PWM Mode: Output drivers are actively regulating load current as programmed, off state diagnostics are disabled.

FULL_ON Mode: Output driver is driven to saturation and is kept on continuously until the mode is changed by the user or a fault occurs.

**Figure 9. Hardware control configuration**




Upon completing channel configuration and set-up as summarized in Section 6: Current control drivers, the internal hardware control loop can then be configured for either fixed frequency or variable frequency current control (HW feedback Frequency Mode D[11] in CTRLCFG register). The current control method (HW mod/SW mode) is selectable using register CONFIGURATION1, D[2]. In addition to selecting the control method, the user must program the targeted load current and operating frequency. Load current is programmed through the Current Set Point Register (SETPOINT) and the operating frequency in the Control Configuration Register (CTRLCFG). Once the channel is enabled, the device begins to PWM control the load current for the targeted current value.

The device can synchronize channel actuation by enabling all channels with a single SPI write operation. Actuation control can also be staggered 90 degrees when programmed for fixed frequency control using the Stagger Enable D[0] bit in SERVENA register.

### 6.1.1 Current set point programming

The targeted average current set point is independently programmable for each channel through the dedicated SPI register (Channel_x.Current_Set_Point) and it is 13-bit wide. The current resolution is programmable in two resolution steps through the HILOAD bit (D[8] in Channel_x.Configuration1) which will also set the maximum regulated current. Below is a brief summary for using HILOAD to select current range and resolution.

- HILOAD = 0 → Normal current mode - Single bit resolution = 0.25 [mA] - Max Avg. Current 1.5 [A].

$$TargetAverageCurrent = Setpoint[12:0]*0.25[mA]$$

- HILOAD = 1 → High current mode - Single bit resolution = 0.33 [mA] - Max Avg. Current 2.0 [A].

$$TargetAverageCurrent = Setpoint[12:0]*0.33[mA]$$

The maximum guaranteed ripple current for the device's specified accuracy is 0.5 [A] peak to peak for HILOAD=0 and 0.66 [A] peak to peak for HILOAD=1, so that the max load current for correct current control is

- 1500 mA + 250 mA = 1750 mA for HILOAD = 0
- 2000 mA + 330 mA = 2330 mA for HILOAD = 1

If the channel is enabled and programmed with 0x0000h current set point, the power output is forced with duty cycle 0 (recirculation path fully on) and the current measurement is disabled; set point codes higher than 0x1770h are reserved for calibration and offset compensation purposes: in case such codes are selected, the accuracy is not guaranteed.

When CHx.SETPOINT=0000 and channel x is controlled Hardware mode (CONFIGURATION1.D[2]=0), then current measurement is disabled and AVGCUR always returns all '0', even if channel x is driven full-on.

### 6.1.2 PWM switching period programming

The PWM switching period is programmable as shown in the next table, through the dedicated 11-bit field in the SPI register Channel_x.Control Configuration (CTRLCFG):

**Table 11. PWM period and Frequency Programming**

| PWM code [10:0] | | Period [µs] | Frequency [Hz] | Status |
|---|---|---|---|---|
| hex | dec | | | |
| 0x000 | 0 | 50 | 20000 | Short period/High frequency range<br>PWM Period = 50 µs + PWM Code D[10:0] * 5 µs |
| 0x001 | 1 | 55 | 18180 | |
| … | … | … | … | |
| 0x009 | 9 | 95 | 10520 | |
| 0x00A | 10 | 100 | 10000 | PWM Period = PWM Code D[10:0] * 10 µs<br>Normal Period/Frequency range. |
| 0x00B | 11 | 110 | 9090 | |
| … | … | … | … | |
| 0x681 | 1665 | 16650 | 60.06 | |
| 0x682 | 1666 | 16660 | 60.02 | |
| 0x683 | 1667 | 16670 | 60.02 | Values clamped to maximum period of 16.67 ms |
| … | … | 16670 | 60.02 | |
| 0x7FF | 2047 | 16670 | 60.02 | |

### 6.1.3 Current control loop configuration

Hardware current control feedback Frequency Mode is user programmable for either variable or fixed frequency operation through register Channelx_CTRLCFG, bit D[11].

In fixed frequency current control configuration, the programmed PWM period is exactly the actuated period. The control algorithm and a Proportional-Integral (PI) processing circuit with ramp-compare control the duty cycle.

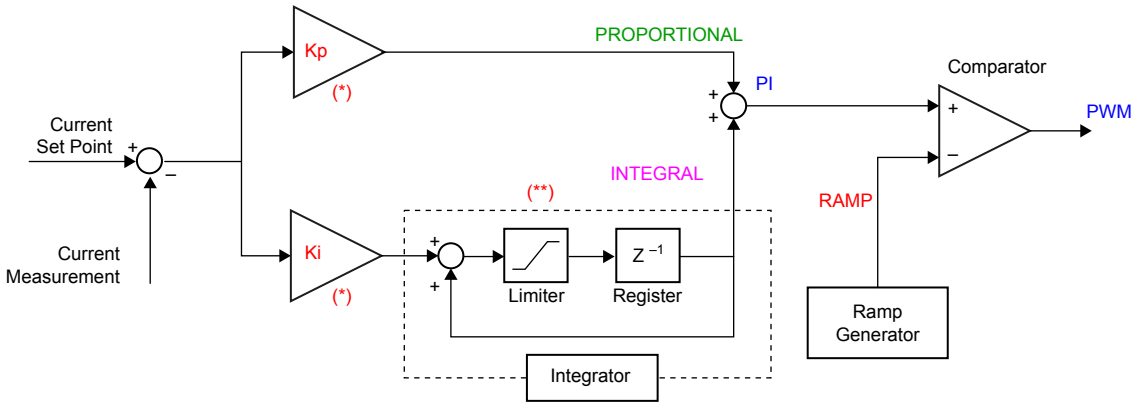
In variable frequency current control configuration, the programmed PWM period is the target set point for the inner frequency control loop. The control algorithm and a zero crossing integrator control both PWM period and duty cycle. The actual PWM period may differ from the target PWM period, especially during transients.

A set of parameters for the loop control is available through SPI registers in order to tune the transient response and settling time of the loop based on the user's load characteristics. These settings and details are discussed in the following sections.

### 6.1.4 Fixed frequency control

The fixed frequency control subtracts the current measurement signal from the programmed set point to create the error signal. The proportional and integral amplifiers process the error signal and generate the PROPORTIONAL and INTEGRAL signals. The processing of PROPORTIONAL and INTEGRAL signals depends on the user programmed values of Kp and Ki in the Channel_x.KGAINS register. The control loop then adds PROPORTIONAL and INTEGRAL signals and compares the result with ramp generator.

**Figure 10. Fixed frequency algorithm**

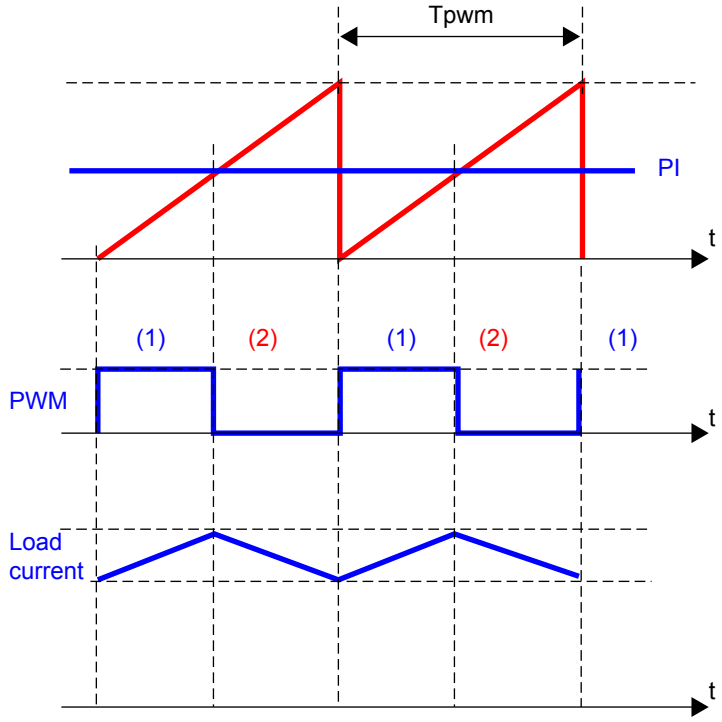



(*) Programmable parameter.

(**) The integrator limiter is automatically calculated for Fixed Frequency algorithm. It avoids that the PI signal exceeds the max. and min. levels of the RAMP signal. This allows fastest loop transient response.

The LIMITER in the integral path, limits the integral signal automatically to the RAMP signal to ensure the fastest PWM changes to reduce current over and under shoot. An example of current control block diagram is shown in Figure 10.

Figure 11. **Fixed frequency signals**




In fixed frequency current control, basic operation is dependent on the ramp generator and the PI signal as follows:

- Switch OFF point (1): the PI signal crosses the RAMP signal from high to low, the output driver is switched off and the load CURRENT reaches its maximum peak value.
- Switch ON point (2): every clock based TPWM periods, the RAMP signal resets and the output driver is switched on and the load current reaches its minimum peak value.

To optimize current control capability, the user must properly select KP and KI amplitude settings (Channel_x.KGAINS) for each application.

- **KP**: parameter controls the amplitude of the Proportional signal and is calculated as: $KP = 2^{KP\_sel}$
- **KI**: parameter controls the amplitude of the Integral signal and is calculated as: $KI = 2^{KI_{sel}}$

### 6.1.5 Variable frequency control

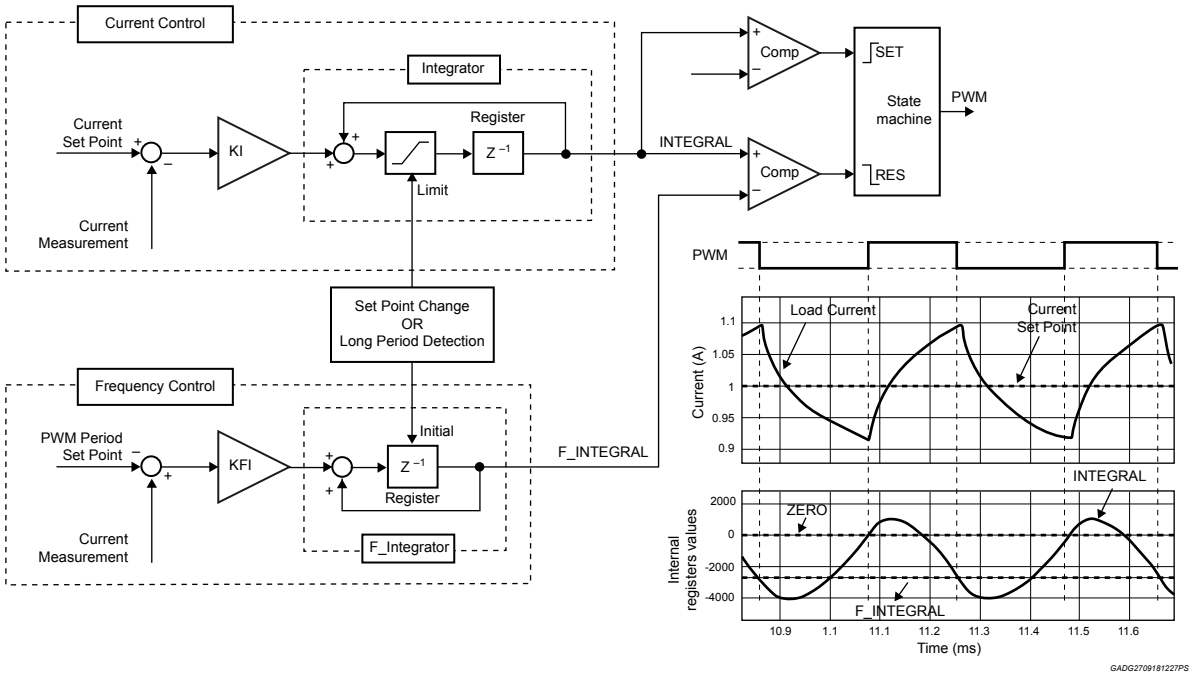
From Figure 12, the current control loop subtracts the measured current from the programmed set point to derive an error signal. The integral amplifier with gain KI processes the error signal creating the INTEGRAL signal. The frequency control loop subtracts the PWM period set point $T_{PWM}$ from the measured PWM period creating a period error signal. The integral amplifier with gain KFI, processes the period error and generates the resulting frequency integral (F_I) output signal.

Variable frequency control operation is dependent on the INTEGRAL signal, F_I signal and zero level signal as follows:

- Switch OFF point: the INTEGRAL signal crosses the F_I signal from high to low, the output driver is switched off and the load CURRENT reaches its maximum peak value.
- Switch ON point: the INTEGRAL signal crosses the zero level signal from low to high, the output driver is switched ON, and the load CURRENT reaches its minimum peak value.

The variable frequency control provides a transient mode for optimization of the transient condition behavior. It eliminates in this way current over/undershoot and allows the fastest reaching of the final frequency. The transient mode is entered in case of a change of current set point (Set Point Change) while the Auto Limit control bit is set. The transient mode is also entered in case the PWM period is longer than a threshold (Long Period Detection). The 2-bit control input Transition Time (D[15:14] in CTRLCFG register) selects the Long Period Detection threshold.

Figure 12. **Variable frequency algorithm**




In transient mode the integrator limits the INTEGRAL signal within user programmable limits, this guarantees the fastest current transitions between different set points without showing over/undershoot. The integrator limits of variable frequency control are not automatically calculated; the user-programmed parameters POSINTLIM and NEGINTLIM are available for optimized positive and negative integrator limits.

In transient mode the F_INTEGRAL signal at the frequency integrator output is set to a programmable value with the 3 control bits FINT_START (D[2:0] in KFREQCTRL register), in this way the F_INTEGRAL signal starts close to its final value when exiting from transient mode.

To optimize the controller response for different applications, the following parameters must be programmed by the user:

- KI (Channel_x.KGAINS)
- KFI (Channel_x.KFREQCTRL)
- POSINTLIM & NEGINTLIM (Channel_x.INTGLIM)
- Auto Limit (Channel_x.SETPOINT)
- Transition Time (Channel_x.CTRLCFG)
- Fint_Start (Channel_x.KFREQCTRL)

Programming values can be selected considering the following:

- **KI**: Integral portion of the loop gain. It can be calculated as $KI = 2^{KI_{sel}}$
- **KFI**: Integral portion of the frequency control loop gain. It can be calculated as $KFI = 2^{KFI_{sel}}$
- **POSINTLIM**: Positive Integrator Saturation Limit. It can be calculated as $POSINTLIM = 2^{(POSINTLIM_{sel} - 1)}$
- **NEGINTLIM**: Negative Integrator Saturation Limit. It can be calculated as $NEGINTLIM = -2^{(NEGINTLIM_{sel} - 1)}$
- AUTO_LIMIT:
  - If AUTOL_LIMIT_SEL = 0 → Transient mode is insensitive to changes of Current Set Point
  - If AUTOL_LIMIT_SEL = 1 → Any change in the current set point activates the transient mode
- FINIT_START:
  - If FINIT_START_SEL = 0 → $FINIT_{START} = 0$
  - If FINIT_START_SEL >0 → $FINIT_{START} = NEGINTLIM{*}2^{(FINITSTART_{sel} - 7)}$

- **TRANSITION TIME**: Too long PWM period detection: if the current PWM time exceeds this threshold, the controller enters the transient state. It can be programmed as follows:
  - If TRANSITION TIME = 0 → $TRANSTIME = 2{,}5{*}T_{PWM}$
  - If TRANSITION TIME = 1 → $TRANSTIME = 4{,}5{*}T_{PWM}$
  - If TRANSITION TIME = 2 → $TRANSTIME = 8{,}5{*}T_{PWM}$
  - If TRANSITION TIME = 3 → $TRANSTIME = 16{,}5{*}T_{PWM}$

### 6.1.6 Chopper offset compensation of current sense amplifier

This function cancels the input offset of the current sense amplifier by converting the DC input offset voltage to an AC noise at the chopper frequency. Function is normally enabled and can be disabled by the user via SPI register (OFS_CMP_DIS D[14] in Channel_x.CONFIGURATION1 register).

### 6.1.7 Staggered channel activation

Staggered channel operation is enabled by the user through the SPI Service Enable register, SERVENA (Stagger Enable bit D[0]). When staggered operation is enabled and the targeted regulated current is achieved, the PWM switch-on points is staggered per the following sequence:

- Channel 0 → 0° phase advance; reference channel
- Channel 1 → 90° phase advance
- Channel 2 → 180° phase advance
- Channel 3 → 270° phase advance

This function is specific to fixed frequency current control and is disabled in variable frequency mode.

### 6.1.8 Parallel mode

The 4 channels can be configured to work in parallel mode to allow regulation of higher current set-points: this option is suitable for example in applications where setting HILOAD = 1 is not enough to match targets.

Channel parallelization can be enabled only for fixed channel pairs:

- ch0 can be put in parallel with ch1 only
- ch2 can be put in parallel with ch3 only

In parallel mode one channel acts as a master (ch0, ch2) and the other as a slave (ch1, ch3): both channel current sense measurements are kept active to measure load current split between channel pair: the two measurements are combined and used to close control loop on master logic only.

Configuration of parallel mode is done through master channel registers and in detail the following master parameters are valid for both channels, overwriting slave channel configuration (if any):

- Current set-point,
- Dither parameters,
- Control loop parameters (Ki, Kp, fix/var frequency mode selector, Kfi, etc…)

As a consequence of the described implementation, the resulting resolution of the current and dither set-point registers is doubled since target value is applied on both channels in parallel: it means that in parallel mode 1 LSB = 0.5 mA instead of default 0.25 mA.

Feedback of measured average current is kept distinguished like in normal operation and available for each channel on its own register with nominal LSB of 0.25 mA. The same applies for HS-LS compare check and applied offset compensation.

The following parameters are kept independent between master and slave channels and particular attention must be paid for proper configuration settings:

- HW/SW mode selection
- HS/LS configuration
- INx/NDISx functionality
- diagnostic
- calibration data
- offset compensation

To enable parallel mode the following conditions must be verified, otherwise the channels will be kept independent depending on their own settings:

- Bit 14 and/or Bit15 in SERVENA register must be set to 1 (Bit14 enables parallel mode for ch0-ch1 pair, Bit15 for ch2-ch3 pair)
- SOLENDRV configuration must be equal for selected parallel channel pair

Even if diagnostic is kept independent, faults causing tri-state condition will affect both channels in parallel mode.

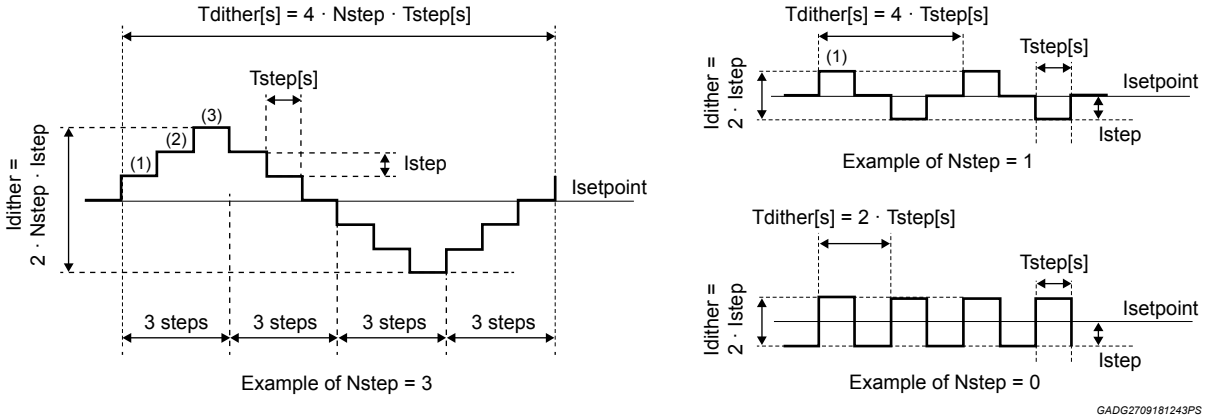
Parallel mode is mandatory to use only with maximum slew rate setting and in configuration HILOAD=0. Besides, driver active time (T_ON) must be higher than a minimum value, which directly depends on load current, battery voltage applied to the solenoid and load parameters.

Further guidelines on the usage of this feature are provided in a specific dedicated Application Note.

### 6.1.9 Dither programming

Dither programming (Channel_x.DITHPGM1 and Channel_x.DITHPGM2) superimposes a triangular amplitude modulation on the current set point as shown in the Figure 13.

**Figure 13. Dither waveforms definitions**




To implement dither function, the following parameters need to be set according to the user operating requirements.

- **Tstep**: Dither step time duration is programmable as an integer number of PWM periods as defined by the formula $DitherStepDuration = (Tstep + 1)*Tpwm$ where:
  - Tstep is programmable in Channel_x.DITHPGM2, D[5:0].
  - $T_{PWM}$ is the PWM period programmable in Channel_x.CTRLCFG register, D[10]
- **Nstep**: number of steps in a quarter of a dither period, where:
  - Nstep is the value programmed in Channel_DITHPGM2 register, D[12:8]
  - If Nstep = 0, a square wave dither of 2 steps peak to peak will be generated
- **Istep**: Current step amplitude is programmable in Channel_xDITHPGM1 register, D[7:0] with the same current resolution as the current set point.
  - HILOAD = 0 → Normal current mode - Single bit resolution = 0.25 [mA] - Max Step Current 63.75[mA]; $DitherStepCurrent = Istep[7:0]*0.25[mA]$
  - HILOAD = 1 → High current mode - Single bit resolution = 0.33 [mA] - Max Step Current 84.15[mA]. $DitherStepCurrent = Istep[7:0]*0.33[mA]$
- Tdither: Dither period calculated as: $Tdither = 4*Nstep*Tstep$
- Idither: Peak-to-peak current modulation amplitude calculated as: $Idither = 2*Nstep*Istep$

Dither can be enabled/disabled via SPI in register Channel_x.DITHPGM1, D[15]. Dither waveform maximum amplitude is limited by the selected current resolution configuration (HILOAD, register CONFIGURATION1, D[15]) as shown below:

HILOAD = 0 → Normal current mode - Max Dither Current Amplitude = ± 250 [mA];

HILOAD = 1 → High current mode - Max Dither Current Amplitude = ± 330 [mA];

### 6.1.10 Dither synchronization

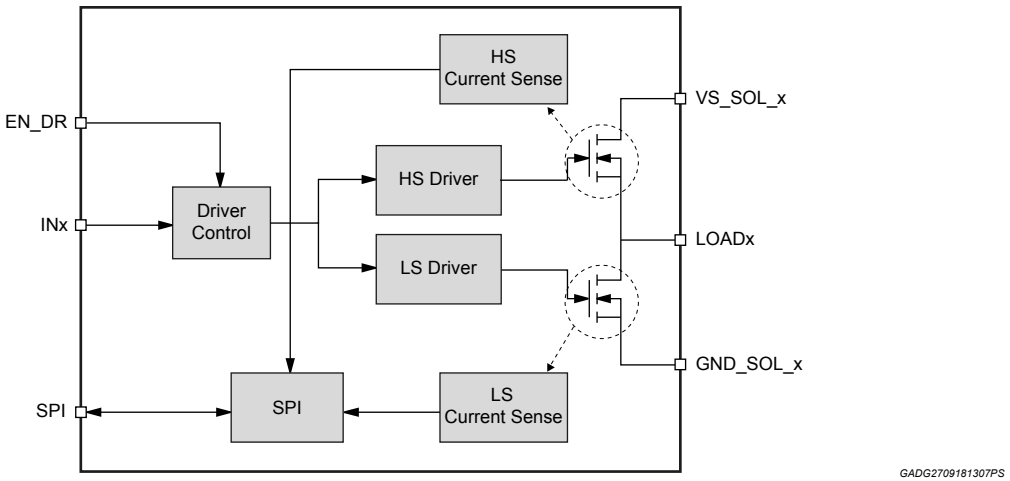
In variable frequency mode, the PWM switch-on events are not clock based and are dependent on frequency control loop response. Therefore variable frequency mode is naturally asynchronous with respect to the dither steps. However, it is still possible to synchronize dither with the variable frequency PWM control by synchronizing with the actual PWM frequency. There are two options to sync the dither waveform. The two sync types are shown below. Please, note that the function is not valid for fixed frequency operation since all dither steps are synchronous with the PWM control frequency.

- **Dither SYNC Enable** - register Channelx_DTHPGM1, bit D[14]
  - 0 → Dither synch for variable frequency is disabled
  - 1 → Dither synch for variable frequency is enabled
- **SYNC TYP**E – register ChannelxDTHPGM1, bit D[13]
  - 0 → All Dither Steps are synchronous with the PWM Period. In this case the time base for Dither Step duration is the actual PWM period rather than the exact target set point PWM period
  - 1 → The Dither Period starts synchronous with the actual PWM Period. Only for the initial step in the dither period, the $T_{step}$ is delayed to the next switch on transition of the PWM period. The time of such initial step may be longer than the programmed period.

## 6.2 Software current control

In this configuration the device works as a driver without internal current control but provides the average measured load current to the MCU through register Channel_x.AVGCUR, bits D[13:0]. With the average current feedback, the MCU can close the current control loop.

**Figure 14. Software control configuration**




To avoid spurious switching of the external loads due to noise spikes on INx pins, a digital filter, *LOADx_ton_res* and *LOADx_toff_res* (where “x” is related to selected channel), has been added to these pins.

Since the filter time is applied on each transition of the INx pin signal, OFF to ON and ON to OFF, the effect limits the minimum period or maximum frequency of the signal delivered to the LOADx pin.

Channel state depends on the EN_DR input pin and the value of the Driver Configuration/Status SPI register (Global.Solenoid Drivers Enable) as shown below.

**Table 12. Solenoid driver channel status in software mode**

| EN_DR | Driver configuration status | | Channel status |
|---|---|---|---|
| | [1] | [0] | |
| LOW | X | X | Driver Disabled, Off Diagnosis disabled and Masked |
| HIGH | 0 | 0 | |
| HIGH | 0 | 1 | Driver in Tristate, Off diagnosis can be switched on |

| EN_DR | Driver configuration status | | Channel status |
|---|---|---|---|
| | [1] | [0] | |
| HIGH | 1 | 0 | Driver ON in PWM mode,Off Diagnosis disabled and Masked |
| HIGH | 1 | 1 | Driver ON in Full ON mode,Off Diagnosis disabled and Masked |

**Disabled Mode:** Driver is kept disabled. No supply is present onto the driver; off diagnosis is masked and cannot be enabled.

**Tristate Mode:** Driver is supplied and kept in Tristate: Hi impedance. Off state diagnostics (Channel_x.Configuration) can be enabled.

**PWM Mode:** Driver is supplied and on. Off state diagnostics are masked. Load is driven by the PWM signal applied to the INx pin. Depending on the selected configuration (HS or LS mode), the INx polarity is defined as follows:

**Table 13. INx polarity**

| Driver Configuration | Driver Status | INx Pin Status | |
|---|---|---|---|
| | | HIGH | LOW |
| LOW Side (load connected between VS_SOLx pin and LOAD_SOLx pin) | Low side FET | ON | OFF |
| | High side FET | OFF | ON |
| HIGH Side (load connected between LOAD_SOLx pin and GND_SOLx pin) | Low side FET | OFF | ON |
| | High side FET | ON | OFF |

**FULL_ON Mode:** Driver is supplied and in FULL_ON mode. In this condition, the driver is kept on continuously, until the FULL_ON mode is removed or a fault occurs.

## 6.3 Solenoid current control feedback

### 6.3.1 Average current

The solenoid current, as a result of internal current sensing, calibration correction and final average calculation over an entire PWM period, is available for SPI reading from Channel_x.AVGCUR register. Independent of HW or SW mode current control selection, the average current calculation cycle starts at each PWM switch ON event and ends at the next PWM switch ON event. The average current calculated is immediately available to the SPI output register through the dedicated 14-bit field in SPI register Channel_x.AVGCUR.

- HILOAD = 0 → Normal current mode - Single bit resolution = 0.25 [mA]
  $AverageCurrent = 2Complemet(AvgCur[13:0])*0.25[mA]$
- HILOAD = 1 → High current mode - Single bit resolution = 0.33 [mA]
  $AverageCurrent = 2Complemet(AvgCur[13:0])*0.33[mA]$

In case the Driver input signal is stuck high or low for a time period longer than $T_{pwm\_max}$, the TMOUT warning flag is set in Channel_x.PWMSENSE register and the average current is evaluated only for $T_{pwm\_max}$. After timeout, the average current and PWM code calculations restart automatically.

When CHx.SETPOINT=0000 and channel x is controlled Hardware mode (CONFIGURATION1.D[2]=0), then the current measurement is disabled and AVGCUR always returns all ‘0’, even if channel x is driven full-on.

### 6.3.2 Integrator feedback

The current integrator output values are important feedback for proper selection of many control parameters. The device provides integrator feedback through the Channel_x.INTOUT register. The content of Channel_x.INTOUT register is determined in the Channel_x.INTGLIM register bits D[15:14]. The integrator feedback definition is defined below:

**Integrator low threshold:**

The integrator such a threshold corresponds to the integrator value at which the PWM toggles from high to low and the output driver switches off. At this point, the load current reaches its max peak level. In variable frequency this level also corresponds to the “F_INTEGRAL” signal at the frequency integrator output. Use this integrator reading to correctly set the “Fint_Start” parameter.

**Integrator high threshold:**

The integrator such a threshold corresponds to the integrator value at which the PWM toggles from low to high and the output driver switches on. At this point, the load current reaches its min peak level. In variable frequency this level is zero. Use this integrator reading to verify the correct functionality of the variable frequency algorithm.

**Integrator minimum level:**

The minimum current integrator level. Use this integrator reading to correctly set the “NEGINTLIM” parameter.

**Integrator maximum level:**

The maximum current integrator level. Use this integrator reading to correctly set the “POSINTLIM” parameter.

### 6.3.3 Solenoid PWM period feedback

The actual PWM time period, whether it is generated by the internal logic in hardware mode or by the INx pins in software mode, is internally measured at each PWM rising edge and provided to the MCU for comparison with the programmed value in register Channel_x.PWMSENSE. It is also checked against the minimum period reference ($T_{pwm\_min}$) and maximum period reference ($T_{pwm\_max}$) values. Should the PWM period fall outside these limits, the TMOUT flag is set in SPI register Channel_x.PWMSENSE indicating the control loop is working at an unusual value. If no PWM signal is generated after the maximum reference period ($T_{pwm\_max}$), the average current is calculated over $T_{pwm\_max}$ period of time.

The PWM period is provided using 15 bits with 1µs resolution, providing feedback for periods exceeding $T_{pwm\_max}$ values. The PWM period feedback value is obtained by the formula:

$$PWMPeriod = Channel\_x.PWMSENSE.PWMCode[\mu s] \quad (1)$$

- $T_{pwm\_min}$ = 40 µs → fpwm_max = 25 kHz
- $T_{pwm\_max}$ = 16.667 ms → fpwm_min = 60 Hz

### 6.3.4 Out of regulation flag

An out of regulation flag is set when the current controller average error is not zero for a time longer than 8 PWM periods, where the PWM period is the programmed PWM period in SPI register Channel_x.CTRLCFG. The flag is independent for each channel and is only available in Hardware Current Control mode.

## 6.4 Solenoid driver and load diagnostic

### 6.4.1 Thermal protection

Each solenoid channel has a dedicated temperature sensor that continuously monitors the temperature of the Low Side and of the High Side power transistor. Temperature information is available in the dedicated SPI register Channel_x.TEMPMON. Register data can be decoded from the SPI frame using the following formula:

$$T_J = 1.353 * TemperatureMonitor - 74 \left[^oC\right] \quad (2)$$

Should channel temperature reach the thermal warning threshold T_WARN, the thermal warning flag is set in the EXCEPTIONS1 register bit D[15]. The warning flag is latched and is cleared upon SPI read if the thermal warning condition is no longer present.

Should channel temperature continue to rise up to the thermal shutdown threshold T_SD, the related channel is placed in tristate mode (setting the Solenoid Driver Status bits to 01, but keeping the programmed current set-point). This event has a dedicated fault flag in the EXCEPTIONS1 register, bit D[0]. Channel activation is prevented if thermal shut down condition is still present on SPI read. This fault is latched and is cleared upon SPI read if the fault is no longer present. Channel thermal shutdown temperature has no hysteresis, but user can decide which temperature is low enough to re-enable the channel. In fact, by monitoring Channelx.TEMPMON register, user can re-enable the channel when TEMPMON reading is below the temperature desired value: thus a further degree of flexibility is provided.

### 6.4.2 Overcurrent protection

Overcurrent protection is present for each HS and LS solenoid driver. The overcurrent threshold is selectable through SPI register Channel_x.CONFIGURATION1 bit D[6].

Should an overcurrent fault be detected (on HS or on LS), the related channel is put in tri-state (setting the Solenoid Driver Status bits to 01, but keeping programmed current set-point) and a dedicated diagnostic bit is set in register Channel_x.EXCEPTION1, bits D[2] for HS and D[1] for LS. To restart the channel, the MCU must clear the fault bit by reading the fault register and re-enable the channel.

### 6.4.3 Supply disconnection

When a solenoid channel is configured for low side operation, current recirculation occurs through the internal high side transistor. If the supply Vs_solX of the high side driver is lost, the voltage at LOAD_SOLx pin can become unpredictable and possibly exceed the absolute rating of the device. To prevent this condition from damaging the device, the low side driver has an integrated clamping circuit to limit the peak voltage.

Should the low side clamping structure be activated during normal operation (i.e. solenoid supply line within normal operating range), the channel is put in tri-state (setting the Solenoid Driver Status bits to 01) and the Low Side Clamp Active fault flag D[3] is set in the EXCEPTIONS1 register. To restart the channel, the MCU must clear the fault by reading the EXCEPTIONS1 register and re-enable the channel.

Activation of LS clamp during a load dump event could damage the device due to the high energy of load dump event. To avoid this condition, the LS clamp circuitry is automatically disabled when VBATP pin exceeds deep over-voltage threshold, as defined in Section 8.1.6.

### 6.4.4 Off state solenoid diagnostics

The device provides independent off-state diagnostics for each channel. Simplified diagrams are shown in Figure 15 and Figure 16 below, depending on the chosen configuration.

Figure 15. **Low side configuration diagnostic**

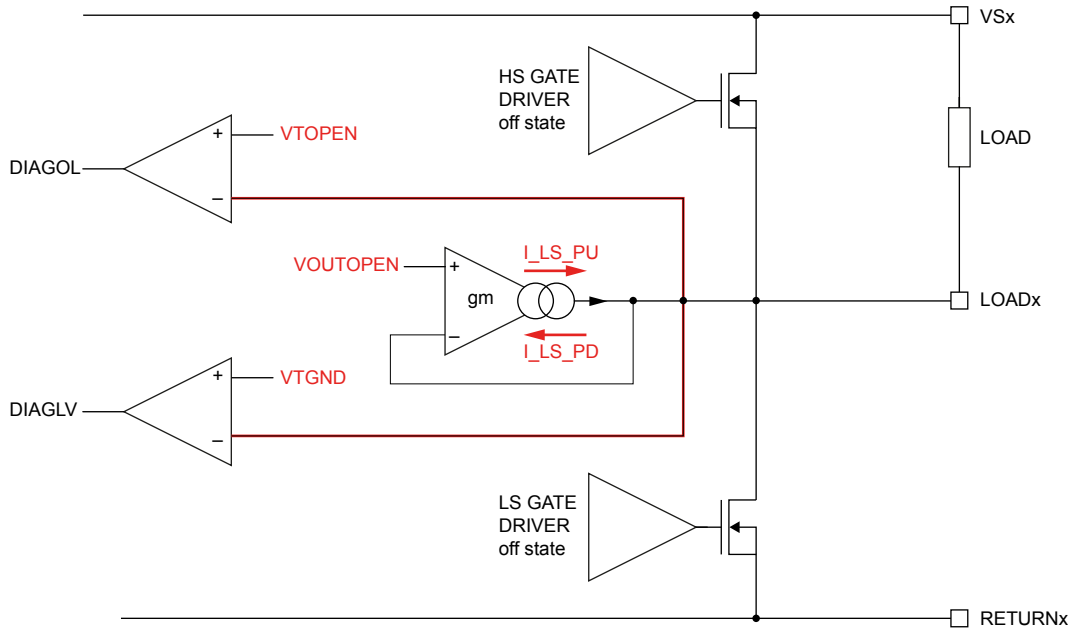
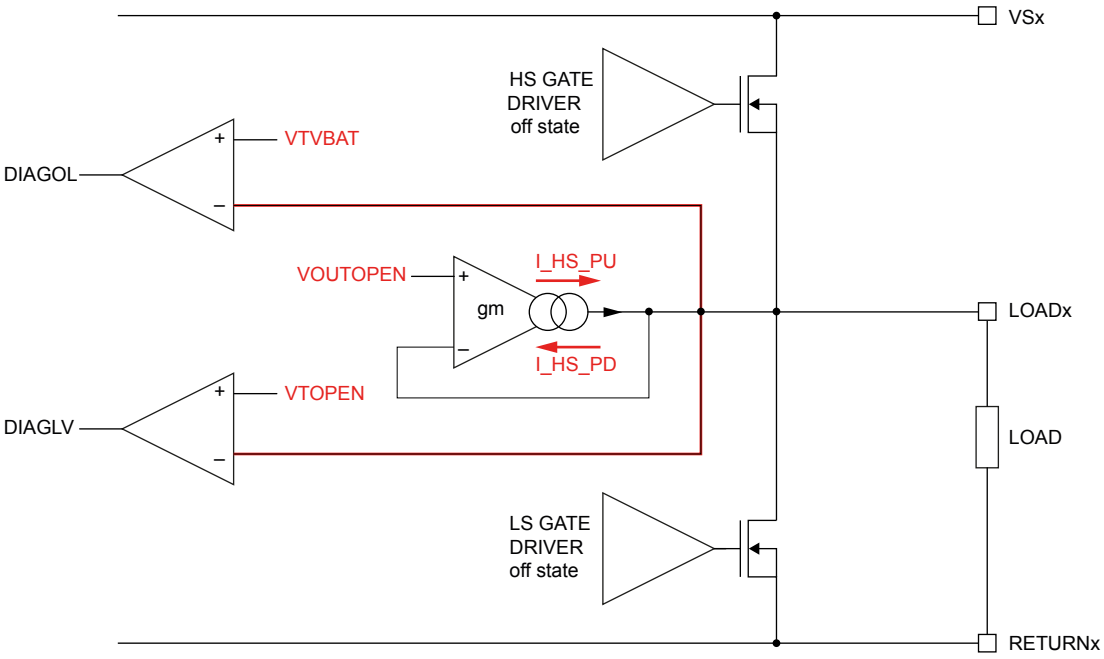



Figure 16. **High side configuration diagnostic**



By default, diagnostic pull up/down current sources are disabled and comparator outputs are masked by internal logic. To enable OFF state diagnostics, the channel must be in tri-state (set in the SOLENDRV register Solenoid Driver State_x[1:0]=01) and enabled using register Channel_x.CONFIGURATION1, bit [5]. In case the desired channel is put in tri-state after operation a false diagnostic can be sensed due to the time needed to discharge output voltage through the load. To avoid incorrect fault detection, the fault comparators are masked for *td_blank* filter time. The diagnostic blanking time is programmable through SPI register Channel_x.CONFIGURATION1, bit D[9]. Blanking time is programmable to best align with external load values and ESD capacitor connected to the output pin. Fault conditions are latched and cleared on SPI read, however they do not prevent from enabling the solenoid channels. OFF state diagnostic comparators are the same for both HS and LS configuration and their output is decoded from internal logic to set the SPI fault bits (Channel_x.EXCEPTIONS1) according to the following tables

**Table 14. LS diagnostic truth table**

| Comparator output | | Fault detection | Exception registers | |
|---|---|---|---|---|
| DIAGOL | DIAGLV | | OPEN LOAD | SHORT |
| 0 | 0 | Normal operation – no fault- | 0 | 0 |
| 0 | 1 | Not possible | 0 | 0 |
| 1 | 0 | Open load | 1 | 0 |
| 1 | 1 | Short to ground | 0 | 1 |

**Table 15. HS diagnostic truth table**

| Comparator output | | Fault detection | Exception registers | |
|---|---|---|---|---|
| DIAGOL | DIAGLV | | OPEN LOAD | SHORT |
| 0 | 0 | Short to Battery | 0 | 1 |
| 0 | 1 | Not possible | 0 | 0 |
| 1 | 0 | Open load | 1 | 0 |
| 1 | 1 | Normal operation – no fault- | 0 | 0 |

## 6.5 Valve driver electrical specifications

4.75 V ≤ VDD ≤ 5.5 V; 5.5 V ≤ VBATP ≤ 19 V; VS_SOLx ≤ 19 V; VBATP-1 V ≤ VS_SOLx ≤ VBATP+1 V; -40 °C ≤ $T_j$ ≤ 175 °C unless otherwise noted. All voltages refer to GNDA pin.

**Table 16. Valve driver power stage electrical parameters**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| **Solenoid driver power stage** | | | | | | | |
| Irev_VSx | VSx reverse current | Application note: in the application condition, no impact on other functions, no reset generation | -3 | – | – | A | VS_SOLx |
| Irev_LOADx | LOADx reverse current | Application note: in the application condition, no impact on other functions, no leakage from nearby pins, no reset generation | -3 | – | – | A | LOAD_SOLx |
| VSx_lkg | VSx current leakage stby | Output disabled, VDD = 0 V, VS_SOLx = 13 V | -1 | – | 1 | µA | VS_SOLx |
| LOADx_lkg | LOADx current leakage tristate | Output disabled, VDD = 5 V, VS_SOLx = 13 V, LOAD_SOLx = VS_SOLx or GND | -140 | – | 100 | µA | LOAD_SOLx |
| HS_RdsON | High side RdsON | $T_j$ = 150 °C, $I_{LOAD}$ = 1 A | – | – | 0.33 | Ω | LOAD_SOLx |
| HS_RdsON | High side RdsON | $T_j$ = 175 °C, $I_{LOAD}$ = 1 A | – | – | 0.375 | Ω | LOAD_SOLx |
| LS_RdsON | Low side RdsON | $T_j$ = 150 °C, $I_{LOAD}$ = 1 A | – | – | 0.33 | Ω | LOAD_SOLx |

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| LS_RdsON | Low side RdsON | $T_j$ = 175 °C, $I_{LOAD}$ = 1 A | – | – | 0.375 | Ω | LOAD_SOLx |
| LOAD_SOLx_ton_res | ton filter time | Software mode, Guaranteed by scan | 3 | 3.5 | 3.9 | µs | LOAD_SOLx |
| LOAD_SOLx_toff_res | toff filter time | Software mode, Guaranteed by scan | 3 | 3.5 | 3.9 | µs | LOAD_SOLx |
| LOAD_SOLx_SR00 | Voltage slew rate SR00 | 20% to 80% & 80% to 20%, VBATP = 13 V, $R_{load}$ = 6 Ω, $C_{load}$ = 10 nF | 0.2 | 0.3 | 0.6 | V/µs | LOAD_SOLx |
| LOAD_SOLx_SR01 | Voltage slew rate SR01 | 20% to 80% & 80% to 20%, VBATP = 13 V, $R_{load}$ = 6 Ω, $C_{load}$ = 10 nF | 0.6 | 1 | 1.8 | V/µs | LOAD_SOLx |
| LOAD_SOLx_SR10 | Voltage slew rate SR10 | 20% to 80% & 80% to 20%, VBATP = 13 V, $R_{load}$ = 6 Ω, $C_{load}$ = 10 nF | 3 | 4 | 6 | V/µs | LOAD_SOLx |
| LOAD_SOLx_SR11 | Voltage slew rate SR11 | 20% to 80% & 80% to 20%, VBATP = 13 V, $R_{load}$ = 6 Ω, $C_{load}$ = 10 nF | 6 | 8 | 12 | V/µs | LOAD_SOLx |
| LOAD_SOLx_ton00_HS | ton 00_HS_mode | SW mode from INx_DISx to 20% in HS | 8 | – | 16 | µs | LOAD_SOLx |
| LOAD_SOLx_ton00_LS | ton 00_LS_mode | SW mode from INx_DISx to 80% in LS | 12 | – | 20 | µs | LOAD_SOLx |
| LOAD_SOLx_ton01_HS | ton 01_HS_mode | SW mode from INx_DISx to 20% in HS | 4 | – | 10 | µs | LOAD_SOLx |
| LOAD_SOLx_ton01_LS | ton 01_LS_mode | SW mode from INx_DISx to 80% in LS | 5 | – | 13 | µs | LOAD_SOLx |
| LOAD_SOLx_ton10 | ton 10 | SW mode from INx_DISx to 20% in HS, from INx_DISx to 80% in LS | 3 | – | 8 | µs | LOAD_SOLx |
| LOAD_SOLx_ton11 | ton 11 | SW mode from INx_DISx to 20% in HS, from INx_DISx to 80% in LS | 3 | – | 8 | µs | LOAD_SOLx |
| LOAD_SOLx_toff00_HS | toff 00_HS_mode | SW mode, from INx_DISx to 80% in HS | 10 | – | 22 | µs | LOAD_SOLx |
| LOAD_SOLx_toff00_LS | toff 00_LS_mode | SW mode, from INx_DISx to 20% in LS | 16 | – | 26 | µs | LOAD_SOLx |
| LOAD_SOLx_toff01 | toff 01 | SW mode, from INx_DISx to 80% in HS, from INx_DISx to 20% in LS | 8 | – | 20 | µs | LOAD_SOLx |
| LOAD_SOLx_toff10_HS | toff 10_HS_mode | SW mode, from INx_DISx to 80% in HS | 3 | – | 8 | µs | LOAD_SOLx |
| LOAD_SOLx_toff10_LS | toff 10_LS_mode | SW mode, from INx_DISx to 20% in LS | 5 | – | 10 | µs | LOAD_SOLx |
| LOAD_SOLx_toff11 | toff 11 | SW mode, from INx_DISx to 80% in HS, from INx_DISx to 20% in LS | 3 | – | 8 | µs | LOAD_SOLx |

**Table 17. Current control electrical parameters**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| **Current control** | | | | | | | |
| $I_{reg\_range}$ | Current regulation range | HILOAD_x = 0, Design info, not tested | 0 | – | 1.5 | A | LOAD_SOLx |
| $I_{peak\_range}$ | Peak Current regulation range | HILOAD_x = 0, Design info, not tested | – | – | 1.75 | A | LOAD_SOLx |
| $I_{reg\_res}$ | Current regulation resolution | HILOAD_x = 0, Design info, not tested | – | 0.25 | – | mA | LOAD_SOLx |
| $I_{reg\_acc\_L}$ | Current regulation accuracy | HILOAD_x = 0, 0A ≤ Ireg ≤ 0.5A(1) | -5 | – | 5 | mA | LOAD_SOLx |
| $I_{reg\_acc}$ | Current regulation accuracy | HILOAD_x = 0, 0.5A < Ireg ≤ 1.5A(1) | -1 | – | 1 | % | LOAD_SOLx |
| $I_{reg\_range}$ | Current regulation range | HILOAD_x = 1, Design info, not tested | 0 | – | 2 | A | LOAD_SOLx |
| $I_{peak\_range}$ | Peak Current regulation range | HILOAD_x = 1, Design info, not tested | 0 | – | 2.33 | A | LOAD_SOLx |
| $I_{reg\_acc\_L}$ | Current regulation accuracy | HILOAD_x = 1, 0 A ≤ $I_{reg}$ ≤ 0.3 A(1) | -15 | – | 15 | mA | LOAD_SOLx |

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| $I_{reg\_acc\_L}$ | Current regulation accuracy | HILOAD_x = 1, 0.3A ≤ $I_{reg}$ ≤ 0.5A(1) | -5 | – | 5 | % | LOAD_SOLx |
| $I_{reg\_acc}$ | Current regulation accuracy | HILOAD_x = 1, 0.5 A < $I_{reg}$ ≤ 2 A(1).$T_j$ = -40 °C | -4 | – | 4 | % | LOAD_SOLx |
| | | HILOAD_x = 1, 0.5 A < $I_{reg}$ ≤ 2 A. $T_j$ = 27 °C | -4 | – | 4 | | |
| | | HILOAD_x = 1, 0.5 A < $I_{reg}$ ≤ 1.3A(1).$T_j$ = 150 °C | -4 | – | 4 | | |
| | | HILOAD_x = 1, 1.3 A < $I_{reg}$ ≤ 2 A(1).$T_j$ = 150 °C | -12 | – | 12 | | |
| **Current control – Dither parameters** | | | | | | | |
| Dth_ampl | Dither $T_{step}$ amplitude | Guaranteed by scan | 0 | – | 255*$I_{reg\_res}$ | mA | LOAD_SOLx |
| Dth_num | Dither $T_{step}$ number | Guaranteed by scan | 0 | – | 31 | step | LOAD_SOLx |
| Tstep | Dither $T_{step}$ duration | Guaranteed by scan | $T_{PWM}$ | – | 64*$T_{PWM}$ | | LOAD_SOLx |
| Tdither | Dither Period | Guaranteed by scan | 2*$T_{PWM}$ | – | 4*31*64*$T_{PWM}$ | | LOAD_SOLx |
| **Current control – PWM parameters** | | | | | | | |
| $T_{PWM\_range}$ | PWM period range | Guaranteed by scan, nominal system clock frequency | 50 | – | 20470 | µs | LOAD_SOLx |
| $T_{PWM\_res}$ | PWM period resolution | TPWM < 100 µs, Guaranteed by scan | 4.5 | 5 | 5.6 | µs | LOAD_SOLx |
| $T_{PWM\_res\_2}$ | PWM period resolution | TPWM < 100 µs, Guaranteed by scan | 9 | 10 | 11.1 | µs | LOAD_SOLx |
| $T_{PWM\_min}$ | PWM period meter min value | – | 36.1 | 40 | 44.1 | µs | LOAD_SOLx |
| $T_{PWM\_max}$ | PWM period meter max value | – | 15.04 | 16.67 | 18.38 | ms | LOAD_SOLx |

1. *provided configuration parameters and current control settings are able to allow proper regulation.*

**Table 18. Valve driver on state diagnostics parameters**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| **On state diagnostic** | | | | | | | |
| I_HS_ovc0 | HS overcurrent | OVC_thres_x=0 | – | – | -3 | A | LOAD_SOLx |
| I_HS_ovc1 | HS overcurrent | OVC_thres_x=1 | – | – | -4.5 | A | LOAD_SOLx |
| I_LS_ovc0 | LS overcurrent | OVC_thres_x=0 | 3 | – | – | A | LOAD_SOLx |
| I_LS_ovc1 | LS overcurrent | OVC_thres_x=1 | 4.3 | – | – | A | LOAD_SOLx |
| I_HS_ocv_flt | HS overcurrent filter time | Guaranteed by scan | 3 | – | 5 | µs | LOAD_SOLx |
| I_LS_ocv_flt | LS overcurrent filter time | Guaranteed by scan | 3 | – | 5 | µs | LOAD_SOLx |
| T_SD_accuracy | Temperature ADC accuracy | Design info, not tested | -10 | – | 10 | °C | Tj_SOLx |
| T_WARN | Temperature warning | – | 175 | – | 185 | °C | Tj_SOLx |
| T_SD | Temperature shut down | – | 185 | – | 200 | °C | Tj_SOLx |
| T_SD_deglitch | Digital deglitch filter time | Guaranteed by scan | 7.5 | 10 | 12.5 | µs | Tj_SOLx |
| T_WARN_deglitch | Digital deglitch filter time | Guaranteed by scan | 7.5 | 10 | 12.5 | µs | Tj_SOLx |
| VBATP_ov_th1 | VBATP over voltage first threshold | – | 27 | 27.8 | 29 | V | VBATP |
| VBATP_ov_th1_deglitch | VBATP over voltage digital deglitch | Guaranteed by scan | 90 | – | 120 | µs | VBATP |
| Vclamp | LOADx clamp voltage | VBATP < 27V | 32 | 35 | 38 | V | LOAD_SOLx |
| Vclamp_dly | LOADx disable delay by clamp activation detection | Design info, not tested | – | – | 2 | µs | LOAD_SOLx |

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| Vclamp_flt | LOADx clamp detection filter time | Guaranteed by scan | 3.5 | 5 | 7 | µs | LOAD_SOLx |
| Eclamp | Energy clamp single pulse | $I_{load}$ = 1 A, $T_j$ = 100 °C | – | – | 25 | mJ | LOAD_SOLx |
| Eclamp | Energy clamp single pulse | $I_{load}$ = 1 A, $T_j$ = 175 °C | – | – | 18 | mJ | LOAD_SOLx |

**Table 19. Valve driver LS off state diagnostics parameters**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| **Off state diagnostic – LS configuration** | | | | | | | |
| VTGND | Short to GND threshold voltage | LS mode, driver tristate, diagnostic on | 1.9 | 2.1 | 2.3 | V | LOAD_SOLx |
| VTOPEN | Open load threshold voltage | LS mode, driver tristate, diagnostic on | 2.7 | 2.9 | 3.1 | V | LOAD_SOLx |
| VOUTOPEN | Open load voltage | LS mode, driver tristate, diagnostic on | 2.35 | 2.5 | 2.65 | V | LOAD_SOLx |
| I_LS_THOPEN | Open load threshold current | – | 40 | 60 | 80 | µA | LOAD_SOLx |
| I_LS_PD | Diagnostic pull down current | – | 50 | 70 | 90 | µA | LOAD_SOLx |
| I_LS_PU | Diagnostic pull up current | – | 55 | 75 | 95 | µA | LOAD_SOLx |
| td_blank_0 | Blank time 0 | Bit_blank_x = 0, Guaranteed by scan | 5 | – | 7.5 | ms | LOAD_SOLx |
| td_blank_1 | Blank time 1 | Bit_blank_x = 1, Guaranteed by scan | 2.5 | – | 3.75 | ms | LOAD_SOLx |
| tflt_diagoff | Filter time | Guaranteed by scan | 55 | – | 80 | µs | LOAD_SOLx |
| | Minimum OFF time for correct diagnostic (Blank time 0) | Application note (esd cap < 12 nF, Bit_blank = 0) | 7.58 | – | | ms | LOAD_SOLx |
| | Minimum OFF time for correct diagnostic (Blank time 1) | Application note (esd cap < 6 nF, Bit_blank = 1) | 3.83 | – | | ms | LOAD_SOLx |

**Table 20. Valve Driver HS Off State Diagnostic Parameters**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| **Off State Diagnostic – HS Configuration** | | | | | | | |
| VTVBAT | Short to battery threshold voltage | HS mode, driver tristate, diagnostic on | 2.7 | 2.9 | 3.1 | V | LOAD_SOLx |
| VTOPEN | Open load threshold voltage | HS mode, driver tristate, diagnostic on | 1.9 | 2.1 | 2.3 | V | LOAD_SOLx |
| VOUTOPEN | Open load voltage | HS mode, driver tristate, diagnostic on | 2.35 | 2.5 | 2.65 | V | LOAD_SOLx |
| I_HS_THOPEN | Open load threshold current | – | 30 | 60 | 90 | µA | LOAD_SOLx |
| I_HS_PU | Diagnostic pull up current | – | 55 | 70 | 95 | µA | LOAD_SOLx |
| I_HS_PD | Diagnostic pull down current | – | 60 | 70 | 100 | µA | LOAD_SOLx |
| td_blank_0 | Blank time 0 | Bit_blank_x = 0, Guaranteed by scan | 5 | – | 7.5 | ms | LOAD_SOLx |
| td_blank_1 | Blank time 1 | Bit_blank_x = 1, Guaranteed by scan | 2.5 | – | 3.75 | ms | LOAD_SOLx |
| tflt_diagoff | Filter time | Guaranteed by scan | 55 | – | 80 | µs | LOAD_SOLx |
| | Minimum OFF time for correct diagnostic (Blank time 0) | Application note (esd cap < 12nF, Bit_blank = 0) | 7.58 | – | | ms | LOAD_SOLx |
| | Minimum OFF time for correct diagnostic (Blank time 1) | Application note (esd cap < 6nF, Bit_blank = 1) | 3.83 | – | | ms | LOAD_SOLx |

# 7 High side fail safe pre-driver

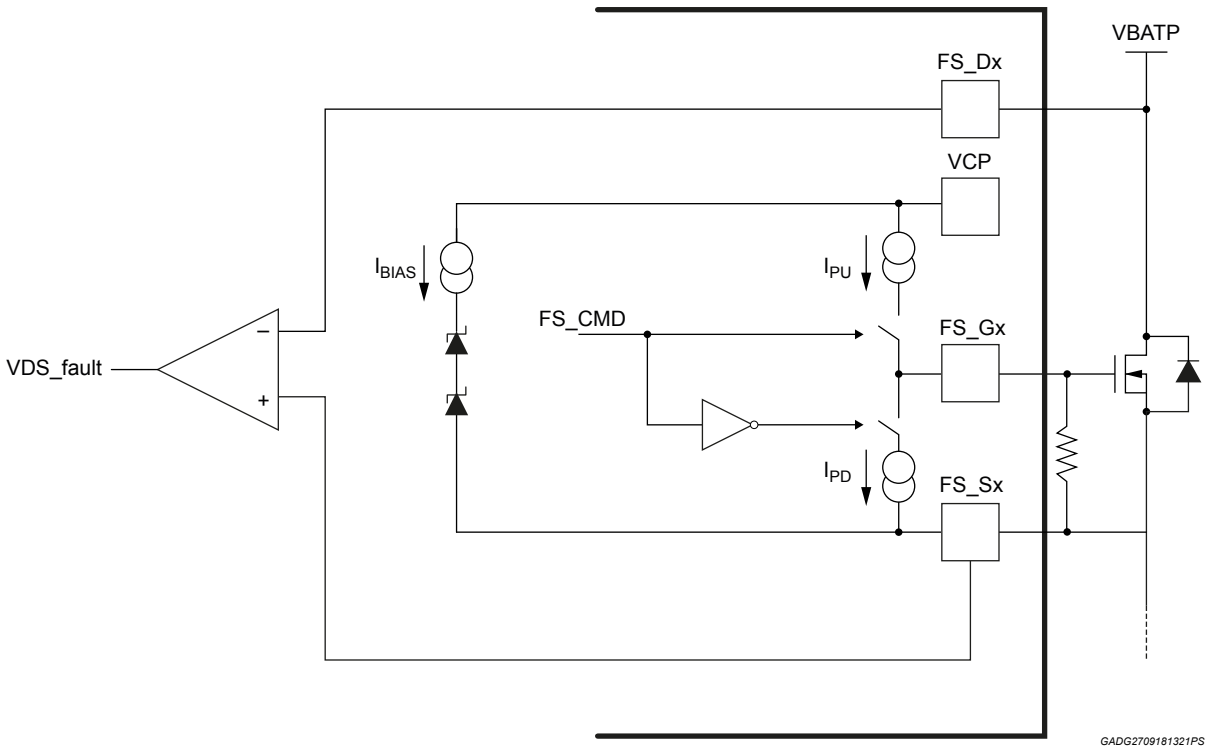
For safety purpose the solenoid loads must be connected to battery line through an external fail safe switch driven by L9305: in case of fault the device must be always able to disconnect external fail safe switch to avoid unwanted energization of solenoid loads. The device provides also diagnostic for external switch, by means of VDS comparator, to detect overcurrent/short conditions and prevent FET from overheating.

In PWSSO36 package, L9305 provides one fail safe pre-driver channel to control an external high side N-channel safety switch. In TQFP48 package, L9305 provides 4 fail safe pre-driver channels to control 4 external high side N-channel safety switches. The pre-driver protects the external N-channel Mosfet by monitoring the drain to source voltage drop across the Mosfet. The threshold for this diagnostic is programmable by the user in the FSCONF register, bits D[1:0]. To enable the output driver, set bit D[2]=1 in the FSCONF register. Upon enabling the output driver, fault monitoring is masked for a period of T_FS_VDS_blank and filtered for T_FS_VDS_flt. Should a fault be detected, the VDS fault flag is set in the SERVFLT1 register, bit D[10]. The fault bit is latched and is clear on read. To re-enable the failsafe pre-driver, the fault must be cleared and the enable bit must be set again through the SPI (FSCONF register).

An external microcontroller can inhibit pre-driver activation by means of the EN_DR input pin: if this pin is driven low the failsafe gate is pulled to ground by an internal switch-off path parallel to the digital one. The internal switch off path is triggered also in case of safety relevant internal faults such as stuck of main clock or overvoltage of the logic core supply voltage.

While the device is in either IDLE or RUNNING mode, EN_DR is set high and FS_EN is set high through an SPI command, the user can set EN_DR low and verify that the fail-safe switch is disabled thru the parallel safety switch off path by reading the PINSTATUS register SAFETY echo (bit D[7]). The user can also verify the EN_DR status reading the PINSTATUS register, bit D[0].

**Figure 17. Fail safe concept**




The Fail Safe pre-driver can be in the following states:

- **FS OFF:** Device in Idle State. Fail Safe related registers at their default state. Internal reset state
- **FS IDLE:** Fail safe disabled. Fail safe related registers preserved but Enable Low. Two cases:
  - EN_DR low. Echo on SPI
  - Error on FS present. Error on SPI and on FAULT pin, if not masked.
- **RUNNING:** Fail Safe enabled and running with gate status depending on SPI command register value

The package option codification is stored inside NVM and verified at power up, in case the package option will not allow for multiple fail safe pre-drivers the unused drivers will be kept disabled.

In case of CRC fault during NVM download the default configuration with only one pre-driver enabled will be applied.

## 7.1 Fail safe predriver diagnostic

The Fail Safe pre-driver has a VDS monitoring that is used to protect the external FET in case of short circuit to ground. Through SPI registers four different VDS thresholds are programmable (FSCONF register, bits D[1:0]).

Once FS_G0 is driven high, after a blanking time (T_FS_VDS_blank) to allow full turn-on of the external FET, the device starts monitoring the falling differential voltage between FS_D0 and FS_S0: if the differential voltage does not drop below the VDS voltage threshold within the over-current filter time (T_FS_VDS_flt), the device disables the Fail Safe pre-driver and sets the VDS fault flag in the SERVFLT1 register, bit D[10].

The fault SPI bit is latched until read; once the fault condition disappears to re-enable the Fail Safe pre-driver, the fault has to be cleared and the enable bit must be set again via SPI. The Fail Safe operation is inhibited until the fault register is cleared.

## 7.2 Fail safe predriver electrical characteristics

4.75≤ VDD ≤ 5.5; 5.5 V ≤ VBATP ≤ 19 V; VBATP - 1 V ≤ FS_Dx ≤ VBATP+1 V; -40 °C ≤ $T_j$ ≤ 175 °C unless otherwise noticed. All voltages refer to AGND pin.

**Table 21. Fail safe predriver electrical parameters**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| FS_ON | External FET gate driving for ON state | FS_G – FS_S | 7 | – | 10 | V | FS_Gx, FS_Sx |
| FS_OFF | External FET gate driving for OFF state | FS_G – FS_S | | – | 1 | V | FS_Gx, FS_Sx |
| FS_Isource | FS current source capability | FS_G = 0 V | 0.5 | 1 | 1.5 | mA | FS_Gx |
| FS_Isink | FS current sink capability | FS_G = VBATP | 3 | 5 | 7 | mA | FS_Gx |
| FS_S_Ibias_IDLE | FS_S bias current from CP supply in IDLE state | Fail safe Pre-driver enabled, CMD off, FS_Dx = VBATP = 13V, VDD = 5V | -450 | -400 | -200 | µA | FS_Sx |
| FS_S_Ibias_RUNNING | FS_S bias current from CP supply in RUNNING state | Fail safe Pre-driver enabled, CMD on, VDD = 5 V, FS_Dx = VBATP = 13 V | -300 | -200 | -100 | µA | FS_Sx |
| FS_D_Ileak_dis | FS_D leakage current with device in IDLE state | Fail safe Pre-driver disabled, FS_Dx = VBATP = 13 V, FS_Sx = open, VDD = 0 V | -1 | – | 1 | µA | FS_Dx |
| FS_Dx_Rpd | FS_Dx resistor toward FS_Sx pin for VDS threshold generation | Fail safe Pre-driver disabled, FS_Dx = VBATP = 13 V, FS_Sx = 0 V, VDD = 0V | 50 | 140 | 250 | kΩ | FS_Dx, FSx |
| FS_D_Ileak_idle | FS_D leakage current in IDLE mode | Fail safe Pre-driver disabled, CMD on, FS_Dx = VBATP = 13 V, VDD = 5 V | 250 | 370 | 500 | µA | FS_Dx |
| FS_D_Ileak_en_on | FS_D leakage current in ON state | Fail safe Pre-driver enabled, CMD on, FS_Dx = VBATP = 13 V, VDD = 5 V | 140 | 250 | 340 | µA | FS_Dx |
| FS_D_Ileak_en_on | FS_D leakage current in ON state | Fail safe Pre-driver enabled, CMD off, FS_D = VBATP = 13 V, VDD = 5 V | 250 | 360 | 550 | µA | FS_Dx |
| FS_VDS_00 | VDS_threshold_0 | FS_PREDRIVER_TH = 00 | 0.15 | 0.25 | 0.35 | V | FS_Dx, FS_Sx |
| FS_VDS_01 | VDS_threshold_1 | FS_PREDRIVER_TH = 01 | 0.4 | 0.5 | 0.6 | V | FS_Dx, FS_Sx |
| FS_VDS_10 | VDS_threshold_2 | FS_PREDRIVER_TH = 10 | 0.65 | 0.75 | 0.85 | V | FS_Dx, FS_Sx |
| FS_VDS_11 | VDS_threshold_3 | FS_PREDRIVER_TH = 11 | 0.9 | 1 | 1.1 | V | FS_Dx, FS_Sx |

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| T_FS_VDS_blank | VDS blank time | Guaranteed by scan | 90 | 110 | 120 | µs | FS_Dx, FS_Sx |
| T_FS_VDS_flt | VDS filter time | EMI filter, guaranteed by design | 100 | 600 | 1000 | ns | FS_Dx, FS_Sx |

# 8 Safety features

The L9305 has several integrated features to enable a reliable functional safety system implementation. A complete list of all monitoring and self-test functions is shown in the next table. The following sections detail these features.

**Table 22. Safety monitors and self test summary**

| | Function | Primary monitor | Self test |
|---|---|---|---|
| **Supply monitors** | Vbat | OV | POR |
| | VCP | UV | POR |
| | VDD | OV & UV | POR |
| | GNDA | LOSS | POR |
| | GNDD | LOSS | POR |
| **Global functions internal monitors** | V3V3AN | OV & UV | POR |
| | V3V3Dig | OV & UV | POR |
| | Trimming Data Error | CRC | None |
| | Global Register Error | Mismatch | None |
| | SPI | Timeout | None |
| | SPI | n * Timeout Latch | None |
| | Core Temperature | Over Temperature | None |
| | Oscillator | Diag Clk stuck-at | None |
| | Oscillator | Clock Mismatch + Main Clk stuck-at | None |
| **Solenoid channel internal monitor** | GND_SOLx | LOSS | POR & On Demand |
| | HS (On state) | OC | None |
| | LS (On State) | OC | None |
| | LS Clamp, On State (Only in LS conf) | OV (dis. for VB > 27V) | None |
| | STG, Off State (Only in LS conf) | | On Demand Only |
| | Open Load, Off State | | On Demand Only |
| | STB, Off State (Only in HS conf) | | On Demand Only |
| | ADC Mismatch | ADC Compare | Channel on Only |
| | EPROM Calibration Data Error | CRC & Data Compare | None |
| | Trim Data Error | CRC | None |
| | RAM Calibration Data Error | CRC | None |
| | Driver Temperature | Over Temperature | None |
| | Driver Status | Command vs. Actual | On Demand Only |
| | Solenoid Register Error | Mismatch | None |
| | Out of regulation | | On Demand Only |
| | HS/LS compare | | Channel on Only |
| | Solenoid Driver Control Loop | Logic Bist | On Demand Only |
| **Fail safe** | VDS protection | OV | None |

## 8.1 Power supply monitoring and diagnostics

### 8.1.1 VDD over and under voltage diagnostics

The VDD power supply input pin is continuously monitored for over and under voltage conditions by comparing the input voltage with an independent reference. In addition to the static voltage monitoring function, the L9305 includes a self-test to verify the proper operation of the comparator and fault logic thus preventing latent faults from influencing device operation. The self-test is run automatically after a power on reset event. Upon detecting a fault, the corresponding fault bits are set as summarized below.

**Table 23. VDD Fault Summary**

| Register | Location | Bit Name |
|---|---|---|
| SERVFLT1 | D4 | VDD Under Voltage |
| SERVFLT1 | D5 | VDD Over Voltage |
| SERVFLT2 | D6 | VDD UV Self Test |
| SERVFLT2 | D7 | VDD OV Self Test |

A VDD under voltage fault will disable all solenoid drivers and the fail-safe pre-driver. The fault is clear on SPI read but solenoid and fail safe operation must be re-enabled through the SPI.

In case of overvoltage on VDD, fault information is available on SPI, but no action is executed on the solenoid drivers and the fail-safe pre-driver. The fault is clear on SPI read.

### 8.1.2 VBATP supply over voltage

The VBATP power supply input pin is continuously monitored for an over voltage condition by comparing the input voltage with an independent reference. In addition to the static voltage monitoring function, the L9305 includes a self-test to verify the proper operation of the comparator and fault logic thus preventing latent faults from influencing device operation. The self-test is run automatically after a power on reset event. Upon detecting a fault, the corresponding fault bits are set as summarized below.

**Table 24. VBATP Fault Summary**

| Register | Location | Bit Name |
|---|---|---|
| SERVFLT1 | D1 | VBATP over voltage |
| SERVFLT2 | D4 | VBATP over voltage self-test |

A VBATP over voltage fault will disable all solenoid drivers and the failsafe pre-driver. The fault is clear on SPI read but solenoid and fail safe operation must be re-enabled through the SPI.

### 8.1.3 VCP supply under voltage

The VCP charge pump power supply is continuously monitored for an under voltage condition by comparing the input voltage with an independent reference. Upon detecting a fault, the corresponding fault bit is set as summarized below.

**Table 25. Charge pump fault summary**

| Register | Location | Bit Name |
|---|---|---|
| SERVFLT1 | D3 | CP under voltage |

A VCP under voltage fault will disable all solenoid drivers and the failsafe pre-driver. The fault is cleared on SPI read but solenoid and fail safe operation must be re-enabled through the SPI.

### 8.1.4 Bandgap regulators, internal analog and digital supply monitoring

There are two internal bandgap regulators, main and auxiliary and two internal low voltage regulators, V3VA and V3VD. These regulators are monitored for over and under voltage conditions and a fault on any regulator regardless of the type of the result in a Power On Reset (POR). There are no flags dedicated to these fault conditions other than the POR flag. A POR event resets all registers and disables all solenoids and fail safe. The POR flag is available as shown below.

**Table 26. POR fault summary**

| Register | Location | Bit Name |
|---|---|---|
| SERVFLT1 | D9 | POR Flag |

In addition to the static voltage monitoring function, the L9305 includes a self-test to verify the proper operation of all comparators and fault logic thus preventing latent faults from influencing the device operation. The self-test function verifies the voltage comparison and logic to ensure the entire path is verified. The self-test is run on demand by setting the ODTEST [D0]. The sequence for initiating the self-test and reading the response is shown below:

- In ODTEST register set bit D[0] = 1
- Monitor ODTEST register bit D[0] for test status, 1 = test in process, 0 = test complete.
- If ODTEST register bit D[0] = 1 the test has succeeded; if the test fails device executes a POR and the related bit will be set on SPI register.

### 8.1.5 GND loss detection

GNDA and GNDD are continuously monitored for loss of ground connection. Ground loss comparators and fault logic are monitored for latent faults using a self-test function. The self-test is automatically performed upon a POR event. Should a ground loss or self-test fault be detected, the corresponding fault bits are set and are summarized below.

**Table 27. GNDA and GNDD fault summary**

| Register | Location | Bit Name |
|---|---|---|
| SERVFLT1 | D15 | GNDD Loss |
| SERVFLT1 | D14 | GNDA Loss |
| SERVFLT2 | D2 | GNDA Loss Self Test |
| SERVFLT2 | D3 | GNDD Loss Self Test |

A GNDA or GNDD Loss fault will disable all solenoid drivers and the fail-safe pre-driver. The fault is cleared on SPI read but solenoid and fail-safe operation must be re-enabled through the SPI.

Each solenoid driver channel has a dedicated ground connection, GND_SOL0, GND_SOL1, GND_SOL2 and GND_SOL3. Should a fault be detected, the faulted channel will be disabled and fault flag set as shown below:

**Table 28. Solenoid GND fault summary**

| Register | Location | Bit Name |
|---|---|---|
| EXCEPTIONS2 | D3 | Ground Loss |

Each solenoid ground connection is continuously monitored for loss of connection. Each loss of ground monitoring circuit also contains a self-test function that must be requested by the user. The sequence for initiating the self-test and reading the response is shown below:

- For the desired channel, in CONFIGURATION2 register set bit D[0] = 1
- Monitor EXCEPTIONS2 register, bit D[5] for test status, 1 = test in process, 0 = test complete.
- Read EXCEPTIONS2 register, bit D[3]; 0 = no fault; 1 = fault

As stated previously, a fault will disable the associated channel and it must be re-enabled by the user. Solenoid ground loss faults do not disable fail safe and are cleared on SPI read.

### 8.1.6 Power supply monitoring and diagnostics electrical characteristics

4.75 V ≤ VDD ≤ 5.5 V; 5.5 V ≤ VBATP ≤ 19 V; -40 °C ≤ $T_j$ ≤ 175 °C unless otherwise noted. All voltages refer to GNDA pin.

**Table 29. Power supply monitoring electrical performance**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| VDD_UV | VDD under voltage detection | – | 3.6 | – | 3.9 | V | VDD |
| VDD_UV_hyst | VDD under voltage hysteresis | – | VDD_UV+0.1 | – | VDD_UV+0.5 | V | VDD |
| VDD_UV_deglitch | Digital filter time | Guaranteed by scan | 9 | – | 12 | µs | VDD |
| VDD_OV | VDD over voltage detection | – | 5.5 | – | 7 | V | VDD |
| VDD_OV_hyst | VDD over voltage hysteresis | – | VDD_OV-0.1 | – | VDD_OV-0.5 | V | VDD |
| VDD_OV_deglitch | Digital filter time | Guaranteed by scan | 90 | – | 120 | µs | VDD |
| VBATP_OV(1) | VBATP over voltage detection | – | 36 | – | – | V | VBATP |
| VBATP_OV_hyst | VBATP over voltage hysteresis | – | VBATP_OV-1 | – | VBATP_OV-3 | V | VBATP |
| VBATP_OV_deglitch | Digital filter time | Guaranteed by scan | 90 | – | 120 | µs | VBATP |
| CP_UV | Charge Pump under voltage detection | – | VBATP+5 | – | – | V | CP |
| CP_UV_deglitch | Charge Pump Under Voltage Filter time | Guaranteed by scan | 9 | – | 12 | µs | CP |
| V3V3A_uv | Internal Analog supply under voltage monitor | Design info, not tested | 2.6 | – | – | V | V3V3A |
| V3V3A_uv_hys | Internal Analog supply under voltage hysteresis | – | V3V3A_uv +0.1 | – | V3V3A_uv +0.5 | V | V3V3A |
| V3V3A_ov | Internal Analog supply over voltage monitor | Design info, not tested | 3.6 | – | 4.6 | V | V3V3A |
| V3V3A_ov_hys | Internal Analog supply over voltage hysteresis | – | V3V3A_ov -0.1 | – | V3V3A_ov -0.5 | V | V3V3A |
| V3V3D_uv | Internal Digital supply under voltage monitor | Design info, not tested | 2.6 | – | – | V | V3V3D |
| V3V3D_uv_hys | Internal Digital supply under voltage hysteresis | – | V3V3D_uv +0.1 | – | V3V3D_uv +0.5 | V | V3V3D |
| V3V3D_ov | Internal Digital supply over voltage monitor | Design info, not tested | 3.6 | – | 4.6 | V | V3V3D |
| V3V3D_ov_hys | Internal Digital supply over voltage hysteresis | – | V3V3D_ov -0.1 | – | V3V3D_ov -0.5 | V | V3V3D |
| GNDA_lost | Analog ground lost detection | Design info, not tested | 0.1 | – | 0.6 | V | GNDA |
| GNDA_lost_deglitch | GNDA deglitch | Guaranteed by scan | 14 | – | 22 | µs | GNDA |
| GNDD_lost | Digital ground lost detection | Design info, not tested | 0.1 | – | 0.6 | V | GNDD |
| GNDD_lost_deglitch | GNDD deglitch | Guaranteed by scan | 14 | – | 22 | µs | GNDD |
| GND_SOLx_lost | Power ground lost detection | Design info, not tested | 0.3 | – | 1 | V | GND_SOLx |
| GND_SOLx_lost_deglitch | Power ground deglitch | Guaranteed by scan | 35 | – | 50 | µs | GND_SOLx |

1. *LS clamp circuitry automatically disabled, see Section 6.4.3*

## 8.2 Main & reference oscillators

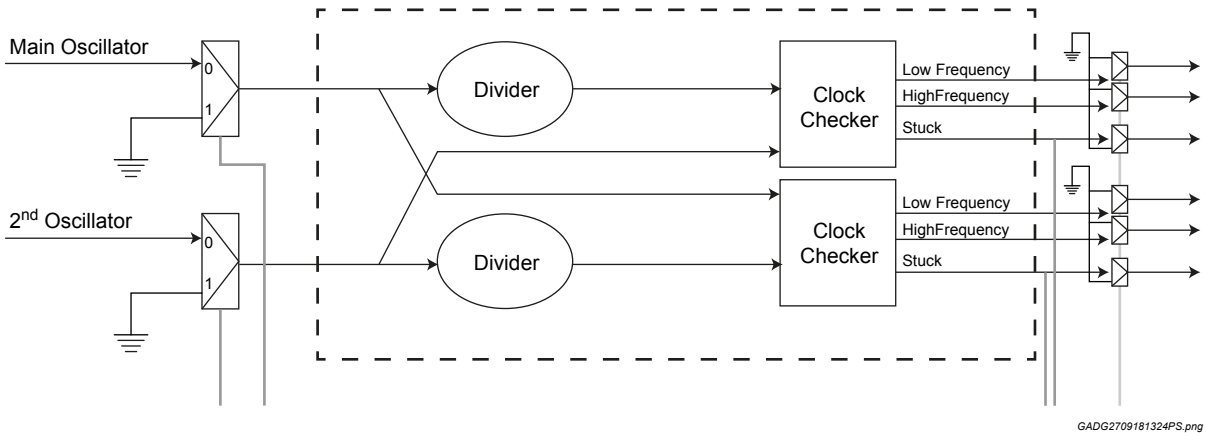
The L9305 has two internal clock oscillators, main and reference. The main clock oscillator provides the timing and control for all device operating functions. The reference clock oscillator provides the monitoring reference to verify the main oscillator. The monitor is able to check if one of the two oscillators is stuck and if there is a strong frequency mismatch between them. In case the main oscillator isn't toggling or there is a strong frequency mismatch on it, the monitor will generate an asynchronous activation of a safety switch off path to disable the fail-safe pre-driver: this disable condition will last until fault is recovered.

If a stuck fault on diagnostic oscillator is detected, the device keeps working but reports the corresponding fault through SPI Service Fault 2 register.

Basic implementation of clock monitor is shown in the next figure.

Oscillator monitor is able to detect either stuck condition of one of the two clocks or frequency error of one clock respect the other.

**Figure 18. Oscillator monitor**




### 8.2.1 Main and reference oscillators electrical characteristics

4.75 V ≤ VDD ≤ 5.5 V; 5.5 V ≤ VBATP ≤ 19 V; -40 °C ≤ $T_j$ ≤ 175 °C unless otherwise noted. All voltages refer to GNDA pin.

**Table 30. Main and reference oscillator safety parameters**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OSCMON_timeout | Timeout for stuck detection | Guaranteed by scan | – | – | 60 | µs |
| OSC_freq_error | Max tolerable delta between oscillators | Guaranteed by scan | -15 | – | 15 | % |

## 8.3 Safety switch-off path

In case an over voltage condition is detected on either internal analog or digital supply lines a safety switch-off path is triggered in parallel to the main diagnostic functions. The meaning of this safety path is to ensure a safe state for the system even in case the over voltage condition, caused by overshoot, latent fault, etc., will lead to absolute violation for the internal circuitry: in this catastrophic event the functionality of the device cannot be guaranteed so a high voltage protected circuitry is needed to guarantee the switch-off of the external fail safe transistor(s) and disconnect the safety relevant loads from the main supply line. The safety circuitry is placed in an isolated layout area where no top routing is allowed and a safe distance from other circuits is kept to avoid cross-talk.

The safety off-path is triggered by POR event, main oscillator fault and EN_DR pin low voltage too; safety_fault trigger signal is the asynchronous combination of the main oscillator fault, EN_DR monitor and digital supply overvoltage detection, i.e. the faults that cannot be directly managed by the digital core.

An echo of safety off path activation is fed back to the digital core and mapped on the SPI registers: in this way at power up it is always possible to test the safety off path functionality through EN_DR pin actuation.

### 8.3.1 Safety switch-off path electrical characteristics

4.75 V ≤ VDD ≤ 5.5 V; 5.5 V ≤ VBATP ≤ 19 V; -40 °C ≤ $T_j$ ≤ 175 °C unless otherwise noted. All voltages refer to GNDA pin.

**Table 31. Oscillator safety switch-off path parameter**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| tSAFETYn echo_deglitch | Digital deglitch of safetyn echo | Guaranteed by scan | 0.2 | – | 1 | µs |

## 8.4 Valve drivers

To verify current control integrity, various diagnostic tests are integrated throughout the control path and are explained in the following sections.

### 8.4.1 High side – low side current sense compare

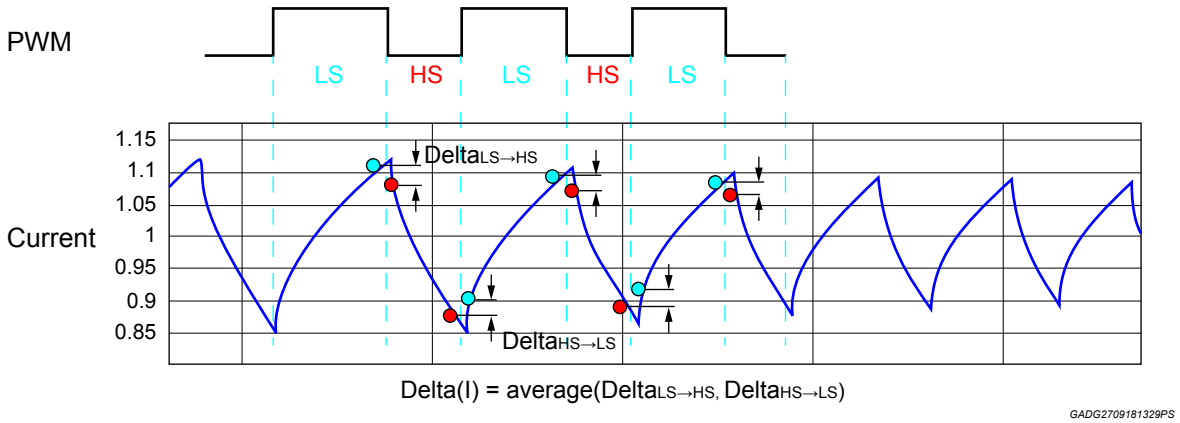
Load current is monitored in both the high side and low side solenoid drivers. The current sensing circuits are independent. The current sense output is multiplexed into an analog to digital converter to close the control loop. To verify the correct current sense functionality, an automatic check between the high and low side current measurements can be made. In the Measured H/L Delta Current register is stored the actual difference between the current sensed from HS and LS circuits, this measured delta current value can be read at power-on by the microcontroller and its value can be written into the Base H/L Delta Current Register, in order to compensate known systematic offsets or delta induced by asymmetrical load transient response and to improve check accuracy. Once the device has the Base H/L Delta Current value recorded, it will continuously monitor the high and low side current values and should the difference exceed the Base H/L Current value, the HS/LS compare fault bit is set (EXCEPTIONS2 register, D[1]). The microcontroller may also perform the same test by simply reading the Measured H/L Delta Current value on a continuous basis and check for deviations.

The current step value is 2 mA per bit. The HS/LS compare fault bit, ie D[1] in the EXCEPTIONS2 register is set high in case the measured current delta exceed the value ± (25 mA + 12.5%*Isetpoint). An example waveform is shown below in Figure 19.

The current step value is measured and sensed. Delta values are stored in SPI registers with two's complement format:

$$MeasuredDeltaCurrent = 2Complement(MeasDeltaCurrent[7:0])*2[mA] \quad (3)$$

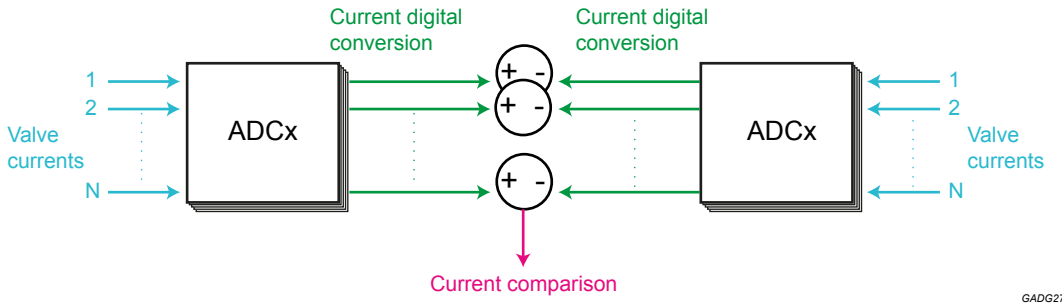
**Figure 19. HS/LS current compare example**



### 8.4.2 Solenoid current control ADC check

Each solenoid current control channel uses two independent current sense circuits, one for each HS and LS power stage. The current sense outputs are multiplexed into the ADC for digital processing and load current control. Each channel has a dedicated current measurement ADC and a redundant verification ADC. The verification is continuous during run time operation and requires no activation by the user. The comparison is done independently for each channel. Should the comparison check result in a difference of more than ADC_CHECK, the Solenoid ADC Mismatch Monitor bit, D[4] in the EXCEPTIONS1 register is set high. The fault is cleared upon reading. A simplified block diagram is shown in the figure below.

**Figure 20. ADC check block diagram**




### 8.4.3 Digital control loop logic BIST

Digital control loop logic test verifies the logic controlling solenoid A/D data calibration and the current control loop. The test is performed independently on each channel. This self-test can be activated only if the channel is in tri-state mode as the control loop is disabled during this test. The sequence for initiating the self-test and reading the response is shown below:

- In CONFIGURATION1 register, set Solenoid Logic Bist, bit D[10] =1
- Test status and results are available in the EXCEPTIONS1 register, bits D[8:7]

Test results are cleared on register read. If test is running and channel is activated, result is unpredictable since CONFIGURATION1 register becomes write protected and test cannot be put back in IDLE. In this case it is better to de-activate the test before activating the channel.

### 8.4.4 Calibration data check

Calibration and trimming data are used to compensate solenoid current control and internal reference circuitry. Data is stored in internal 8K bit NVM made of 256-bit sectors with the following architecture:

**Table 32. NVM memory map**

| 256-bit calibration data field | | | |
|---|---|---|---|
| 120 bits data | 8 bits CRC | 120 bits data | 8 bits CRC |

Upon Power on Reset (POR), the L9305 downloads calibration data from non-volatile memory into the appropriate local registers. During this process, the data is verified using the 8-bit CRC field. If a CRC failure is detected in data corresponding to analog trim data, the CRC error on CSA Compensation data bit, D[14] is set in the EXCEPTIONS 1 fault register. If a failure is detected in data corresponding to ADC compensation, the CRC error on A2D trimming data bit, D[13] is set in the EXCEPTIONS 1 fault register. In all cases, the register(s) affected by the faulty data are loaded to “0” to avoid unpredictable operation. Registers loaded with “0” due to a CRC fault will operate uncalibrated thus having reduced performance.

### 8.4.5 Diagnostic comparators

All solenoid diagnostic comparators (overcurrent, off-state diagnostic, ground loss) have analog self-tests implemented to detect latent faults. The self-test must be enabled by the user with the channel in tri-state. The self-test is independent for each channel. Should the test fail, a diagnostic fault flag is set and is cleared upon reading the register. Should actuation be requested while the self-test is in process, the self-test will be terminated with an error (EXCEPTIONS1 register, self-test fail bit D[8:7] that indicates the case when both the comparators (LV and OV) fails and actuation will be permitted.

The typical procedure for running the diagnostic comparator self-test is outlined below:

- Disable off-state diagnostics, set CONFIGURATION1 register, D[5] = 0
- Enable diagnostics self-test, CONFIGURATION2 register, D[1] = 1
- Read results in EXCEPTIONS1 register, D[8:7]

### 8.4.6 PWM check

The L9305 can verify output driver status with respect to the PWM input signal. This function can only be performed when the channel is enabled and controlling load current. Should a mismatch be detected, the PWM Check Fault, D[12] is set in the EXCEPTIONS1 register.

### 8.4.7 Valve driver safety electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; 5.5 V ≤ VSx ≤ 19 V; -40 °C ≤ $T_j$ ≤ 175 °C unless otherwise noticed. All voltages refer to GNDA pin.

**Table 33. Valve driver safety parameters**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| Delta_curr_sense | Tolerable mismatch between high side and low side current sense | Guaranteed by scan, $I_{load}$ = 0.8 A | -15 | – | 15 | % | LOAD_SOLx |
| ADC_checkHILOAD=0 | Tolerable mismatch between functional and safety ADCs | Guaranteed by scan | -128 | – | 128 | mA | |
| ADC_checkHILOAD=1 | Tolerable mismatch between functional and safety ADCs | | -170.6 | – | 170.6 | mA | |
| t_ADC_blank | Self test blanking time | Guaranteed by scan | 3 | – | 4 | µs | |
| t_BIST | Solenoid digital BIST duration | Guaranteed by scan | – | – | 5 | ms | |
| t_BIST | Analog BIST duration | Guaranteed by scan | 0.9 | 1.7 | 1.8 | ms | |
| t_EEPROM | EEPROM download time | Guaranteed by scan | – | – | 4 | ms | |
| t_PWM_check | PWM check masking time | SR = 00 Guaranteed by scan | 13*64/$f_{OSC}$ | – | 14*64/$f_{OSC}$ | – | LOAD_SOLx |
| t_PWM_check | PWM check masking time | SR = 01 Guaranteed by scan | 9*64/$f_{OSC}$ | – | 10*64/$f_{OSC}$ | – | LOAD_SOLx |
| t_PWM_check | PWM check masking time | SR = 10/11 Guaranteed by scan | 5*64/$f_{OSC}$ | – | 6*64/$f_{OSC}$ | – | LOAD_SOLx |
| PWM_check_deglitch | PWM check fault deglitch time | Guaranteed by scan | 0.2 | – | 1 | µs | LOAD_SOLx |
| I_safe_pd | Safety switch off pull down current capability | Design info not tested | 1 | – | – | mA | FS_Gx |
| Vgs_off_safed | Residual voltage at FS_G pins with safe off path active | Design info not tested in production | – | – | 2 | V | FS_Gx |

## 8.5 Core over temperature

The device internal temperature is monitored against overheating. If an over temperature event is detected, all solenoid driver outputs are disabled, their enable bit is cleared and their configuration registers are reset, a fault bit cleared on read is set in the SPI registers (Core Over Temperature D[0] bit in SERVFLT1 register). Once the over temperature condition is removed the fault information must be cleared to restart the outputs. Core over temperature is provided with a hysteresis in order to avoid power-on/power-off oscillations when temperature is around over temperature threshold.

### 8.5.1 Core over temperature electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; 5.5 V ≤ VSx ≤ 19 V; -40 °C ≤ $T_j$ ≤ 175 °C unless otherwise noticed. All voltages refer to GNDA pin.

Table 34. **Core thermal monitoring electrical performance**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| CORE_ot | CORE over temperature shut down threshold | | 175 | – | 185 | °C |
| CORE_ot_hyst | CORE over temperature hysteresis | – | 4 | 7 | 10 | °C |
| CORE_ot_filt | Digital deglitch | Guaranteed by scan | 9 | 10 | 12 | µs |

## 8.6 IC data verification

All read/write registers are mirrored thus resulting in a main register and a mirror register. The contents of each register's main and mirror are verified for consistency. Should a data mismatch between a main read/write register and its mirror register occur, an associated fault bit is set as described below :

- A global register mismatch flag (SERVFLT1, D[2]) is associated to the global registers
  - SERVENA
  - SOLENDR
  - TIMEOUTSPICFG
  - FSCONF
  - SERVFLTMSK1
  - SERVFLTMSK2
- A channel register mismatch flag (EXCEPTIONS2, D[0]) is dedicated to each channel register bank
  - CONFIGURATION1
  - CONFIGURATION2
  - DITHPGM1
  - DITHPGM2
  - SETPOINT
  - CTRLCFG
  - KFREQCTRL
  - KGAINS
  - INTGLIM
  - DRVFLTMASK1
  - DRVFLTMASK2
  - BASEHLDELTACURR

All the flags are cleared-on-read and refer to the entire register bank. No action is taken when a mismatch arises.

Data mismatch flags can also be mapped to FAULTn pin using SERVFLTMSK1, D[2] for global register and DRVFLTMSK2, D[0] for channel registers. These flags are masked by default and must be enabled by the users as per their system needs.

# 9 SPI

The SPI interface is used to configure the device, control the outputs and read diagnostic and status registers.

## 9.1 SPI protocol

The SPI protocol is defined by 32-bit frames with 5 bits of CRC (Cyclic Redundancy Check) for transmit and receive. MOSI frame consists of an 8-bit address, 16-bit data, 5-bit CRC field and a one-bit frame counter. MISO frame consists of SPI error and IC status information, address feedback, 16-bit data and 5-bit CRC field. SPI communication uses various safety mechanisms to ensure high safety level coverage as defined in ISO26262 table D.8:

- 5-bit CRC check (Hamming distance of 3 over 26 bits data)
- Frame Counter and Address Feedback
- Timeout Monitoring
- Short and Long Frame Length

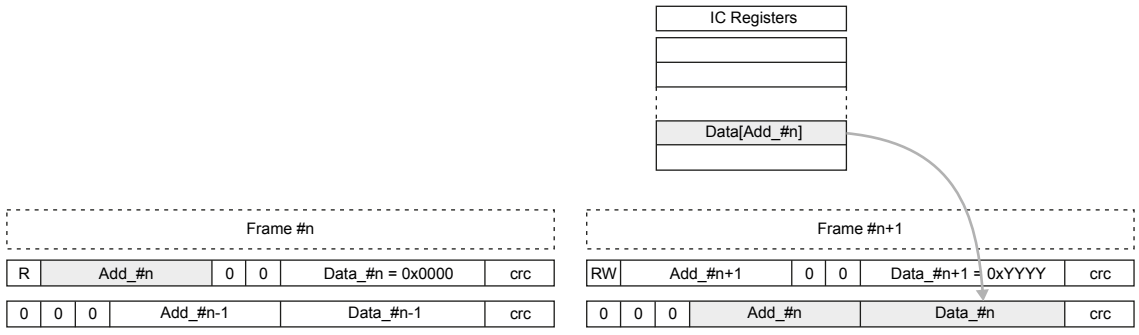
All R/W registers are mirrored (i.e., simultaneously written with the same value) and the content of each main register is verified with its related mirror register. Should a mismatch be detected, a fault flag is set. Details of this safety feature are summarized in Section 8.6. The SPI frame format is shown in Figure 21.

**Figure 21. SPI Frame Format**

| BIT | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MOSI | RW | Page | | | Idx | | | | | 0 | cnt | Data[n] | | | | | | | | | | | | | | | | CRC | | | | |
| MISO | E | IERR | | PageFdbk | | | IndxFdbk | | | | | Data[n-1] | | | | | | | | | | | | | | | | CRC | | | | |

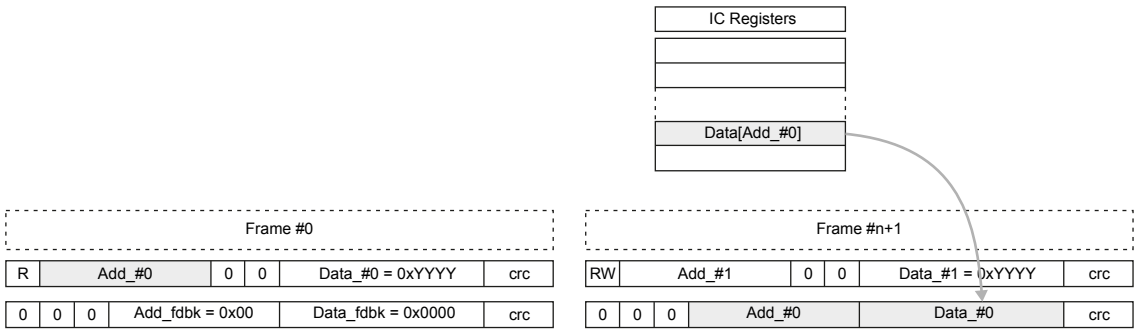
The protocol implements Out of Frame response meaning the MISO output frame is related to the previous transmitted MOSI frame as shown in Figure 22. The First SPI transfer after power on reset will have a fixed MISO response consisting in the device ID.

**Figure 22. Out of frame response**



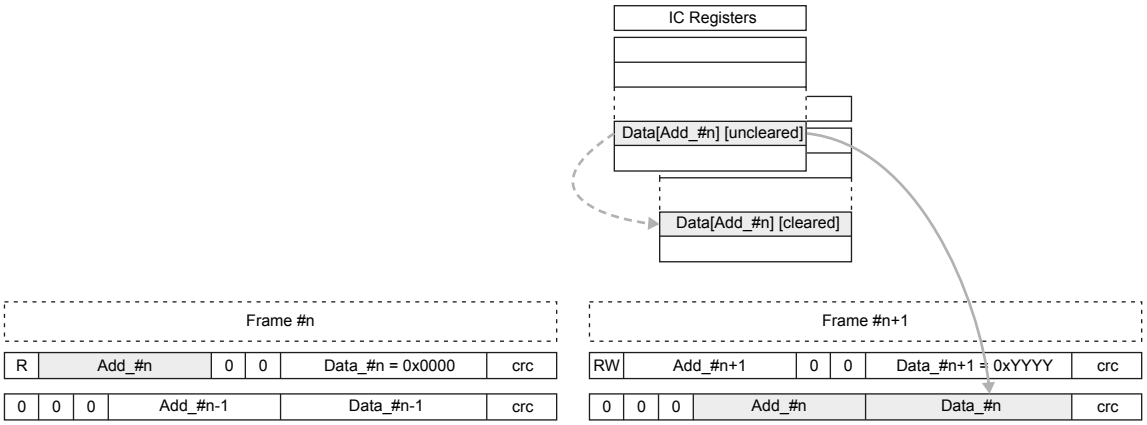

Upon power on reset, the first SPI Frame will set all SPI fault bits and address bits to “0” and the data field will contain the device ID as shown in Figure 23.

Figure 23. **SPI frame after Power On Reset**



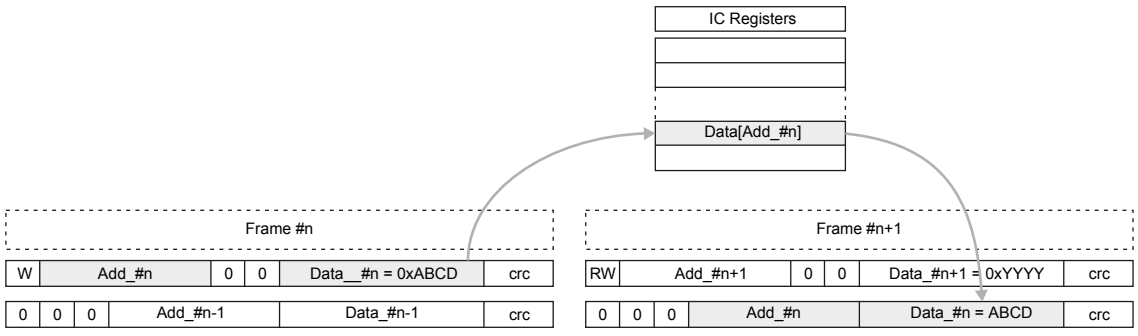

Upon reading a register with Clear on Read fields, the related bits will be cleared only when data has been completely moved on the next SPI access as shown in Figure 24.

Figure 24. **Clear on Read SPI sequence**




Upon register write, data is updated after the frame is completely received and no error has been detected (CRC, frame sequence, frame length). On the next SPI access, MISO data field will contain updated data content from the written register as shown in Figure 25.

Figure 25. **SPI write sequence**




The SPI interface is supplied by VDDIO pin and consists of the following pins and definitions:

- Input pins:
  - CS: Chip Select Active Low
  - SCLK: SPI Clock
  - MOSI: Master Output Slave Input. Communication path from MCU to the device
- Output pins:
  - MISO: Master Input Slave Output. Communication path from the device to the MCU

## 9.2 CRC

Received and transmitted data are verified using a 5-bit CRC field. The CRC is calculated from D[31] of the frame to D[5] excluding frame counter bit, D[21]. The CRC field is checked using 5° degree polynomial and is implemented per the following equation:

g(x)= x5 + x2 + 1

If a CRC error is detected, the received frame is ignored and the fault is indicated in the next SPI frame.

In the logic block for CRC calculation, internal logic shift register is initialized all ‘1’: user should take this into account when executing hand calculations for CRC check.

In fact, since internal logic shift register is initialized all ‘1’, most significant 5 bits must be complemented, in addition, as already stated, Bit 21 must be removed and Bit 4 to Bit 0 must be removed for CRC calculation.

For example, in order to calculate CRC for data “0x1820080A”, user should consider the following data:

Data = "11100000000000000001000000";

which should be divided by 100101, then “01010” should result as a CRC.

As a double check that the remainder is 0, user has to concatenate the 01010 to the previous data and then divide by 100101, i.e:

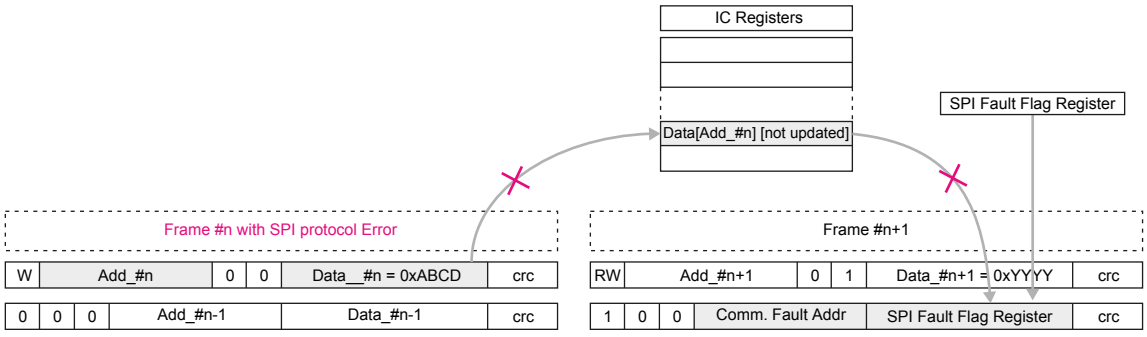
Data = "11100000000000000001000000001010";

and divide by 100101, then ‘0’ will be obtained as a remainder.

## 9.3 SPI errors management

If a communication fault is detected, the SPI error bit (MISO[31]: E bit) is set to “1” and the frame is ignored. The SPI error bit always refers to the previous SPI frame. The next figure shows the SPI frame sequence for faulted communications.

**Figure 26. SPI frame with error on previous SPI frame**




## 9.4 SPI timeout monitoring function

An internal monitor detects a failure if the period between communications exceeds the SPI Timeout period. This monitoring function detects loss of the communications between the microcontroller and the device.

If no valid frames are received before the Timeout Configuration period elapses, the SPI Timeout flag is set (SERVFLT1 register, D[6]) and the FAULTn pin is set low if the corresponding fault mask bit is not set.

The Timeout Configuration value is programmable through a 3-bit SPI field (TIMEOUTSPICFG register, D[4:2]) with a default value of 2 ms. The timer is cleared when a valid SPI frame is received.

Table 35. **SPI time out values**

| Dec | Bin | SPI Time Out<br>63 x 8 x 2N [µs] |
|---|---|---|
| 0 | 000 | 504 |
| 1 | 001 | 1008 |
| 2 | 010 | 2016 |
| 3 | 011 | 4032 |
| 4 | 100 | 8064 |
| 5 | 101 | 16128 |
| 6 | 110 | 32256 |
| 7 | 111 | 64512 |

Reset latch function can reset the device to IDLE state if a certain number of timeout events occur. Enable of this function (TIMEOUTSPICFG register, D[1:0] ) and the number of timeout events (TIMEOUTSPICFG register, D[6:5]) is programmed through SPI.

Table 36. **Reset latch enable state**

| En_Res_Latch[1]<br>(Reset Latch enable) | Dis_Res_Latch[0]<br>(Reset latch disable) | Reset Latch |
|---|---|---|
| 0 | 0 | Disabled |
| 0 | 1 | Disabled |
| 1 | 0 | Enabled |
| 1 | 1 | Disabled |

Table 37. **Time out reset latch counter values**

| Dec | Bin | Time Out Reset Latch Counter [2N+1] |
|---|---|---|
| 0 | 00 | 2 |
| 1 | 01 | 4 |
| 2 | 10 | 8 |
| 3 | 11 | 16 |

## 9.5 SPI channel exception field

MISO frame has 2 bits (IERR) reserved for solenoid channel exceptions. MISO[29] is the OR of all the exceptions related to Channel 0 and Channel 1, while MISO[30] is the OR of all the exceptions related to Channel 2 and Channel 3.

MISO[29] = (Ch0.Exception1&0xF87F) | (Ch1.Exception1&0xF87F) | Ch0.Exception2 | Ch1.Exception2

MISO[30] = (Ch2.Exception1&0xF87F) | (Ch3.Exception1&0xF87F) | Ch2.Exception2 | Ch3.Exception2

In this way, it is always possible to detect a failure happening on solenoid channel during every SPI communication. Details and clearing of the channel exception can be retrieved by reading the dedicated SPI registers.

## 9.6 SPI electrical specification

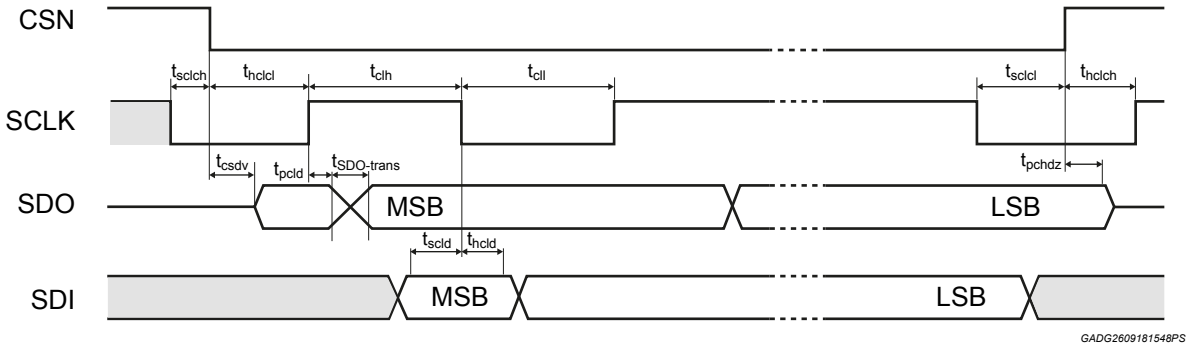
4.75 V ≤ VDD ≤ 5.5 V; 5.5 V ≤ VBATP ≤ 19 V; -40 °C ≤ $T_j$ ≤ 175 °C unless otherwise noted. All voltages refer to GNDA pin.

**Table 38. SPI electrical parameters**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| SPI_in_low | Logic input low detection | – | – | – | 0.75 | V | CS, MOSI, SCLK |
| SPI_in_high | Logic input high detection | – | 1.75 | – | – | V | CS, MOSI, SCLK |
| SPI_in_hyst | Input hysteresis voltage | – | 0.1 | – | – | V | CS, MOSI, SCLK |
| SPI_in_pd | Internal pull down resistance | VIN < 2.5 V | 20 | 40 | 80 | kΩ | MOSI, SCLK |
| SPI_in_pu | Internal pull up resistance | VIN < 2.5 V | 40 | 90 | 180 | kΩ | CS |
| MISO_lleak | Leakage current in tri-state condition | – | – | – | 10 | µA | MISO |
| MISO_low | Logic low level | $I_{sink}$ = 1 mA | – | – | 0.4 | V | MISO |
| MISO_high | Logic high level | $I_{source}$ = 1 mA | VDDIO-0.4 | – | – | V | MISO |
| MISO_trise | MISO rise time | $C_{load}$ = 200 pF | – | – | 50 | ns | MISO |
| MISO_tfall | MISO fall time | $C_{load}$ = 200 pF | – | – | 50 | ns | MISO |
| fclk | Transfer Frequency | Design info 50% duty cycle, not tested(1) | – | – | 8 | MHz | SCLK, MOSI, MISO |
| tpcld+tsdo_trans | Propagation delay | SCLK to data at SDO is valid $C_{load\_max}$ = 200 pF inlcuding parasitics | – | – | 100 | ns | SCLK, MISO |
| tcsdv | NCS=LOW to data at SDO active | $C_{load\_max}$ = 200 pF inlcuding parasitics | – | – | 200 | ns | CS, MISO |
| tpchdz | NCS L/H to SDO at high impedance | $C_{load\_max}$ = 200 pF inlcuding parasitics | – | – | 200 | ns | CS, MISO |
| tsclch | SCLK before NCS low | Design info, not tested | 50 | – | – | ns | CS, SCLK |
| thclcl | SCLK change L/H after NCS=LOW | Design info, not tested | 130 | – | – | ns | CS, SCLK |
| tsclcl | SCLK low before NCS high | Design info, not tested | 50 | – | – | ns | CS, SCLK |
| thclch | SCLK high after NCS high | Design info, not tested | 50 | – | – | ns | CS, SCLK |
| tscld | SDI input setup time | Design info, not tested | 20 | – | – | ns | MOSI |
| thcld | SDI input hold time | Design info, not tested | – | – | 20 | ns | MOSI |
| tonNCS | NCS min. high time | Design info, not tested | 650 | – | – | ns | CS |
| tclh | Minimum Time SCLK=HIGH | Design info, not tested | 45 | – | – | ns | SCLK |
| tcll | Minimum Time SCLK=LOW | Design info, not tested | 45 | – | – | ns | SCLK |
| Cin | Input pin capacitance | Design info, not tested | – | – | 30 | pF | MOSI, CS, SCLK |
| Cout_hiz | MISO output pin capacitance in tri-state | Design info, not tested | – | – | 50 | pF | MISO |

1. *SPI max frequency may be less depending on the total capacitive load and MCU timing requirements*

Figure 27. **SPI timings, thresholds 20% to 80% and viceversa**




## 9.7 SPI registers map table

SPI frame has an 8-bit address field and 16-bit data field, then the available address space consists of up to 256 different registers. Taking into account the logical and physical partition of the functions to be configured and monitored by SPI interface, the address space has been divided in pages of 32 addresses each.

The table below shows the SPI page vs. macro function distribution.

Table 39. **SPI page address mapping**

| Page ID[binary] | Macro Function | Address Space Name | SPI Base Address | |
|---|---|---|---|---|
| | | | [hex] | [binary] |
| 000 | Solenoid Channel 0 | Channel_0_BaseAddress | 0x00 | 0000 0000 |
| 001 | Solenoid Channel 1 | Channel_1_BaseAddress | 0x20 | 0010 0000 |
| 010 | Solenoid Channel 2 | Channel_2_BaseAddress | 0x40 | 0100 0000 |
| 011 | Solenoid Channel 3 | Channel_3_BaseAddress | 0x60 | 0110 0000 |
| 100 | unused | --- | 0x80 | 1000 0000 |
| 101 | unused | --- | 0xA0 | 1010 0000 |
| 110 | Global | Global_BaseAddress | 0xC0 | 1100 0000 |
| 111 | Fault and Test | Fault_Test_BaseAddress | 0xE0 | 1110 0000 |

## 9.8 Global page

Global page contains general control/monitor registers.

Table 40. **SPI global page register address mapping**

| Idx [hex] | Register |
|---|---|
| 0x00 | Service enable |
| 0x01 | Solenoid drivers enable |
| 0x02 | Timeout SPI configuration |
| 0x03 | Fail safe pre-driver configuration |
| 0x1F | Chip ID |

## SERVENA

**Service enable**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parallel mode selection for ch2-ch3 | Parallel mode selection for ch0-ch1 | Unused | | | | RAM retrigger | Spread Spectrum Disable | Unused | | | | | | | Stagger Enable |
| RW | RW | R | | | | RW | RW | R | | | | | | | RW |

**Address:** Global Base Address + 0x00

**Type:** RW

**Reset:** 0x0000

**Description:** General SERVICE Enable bits

[15] Parallel mode selection for ch2-ch3

[14] Parallel mode selection for ch0-ch1

[13:10] Unused

[9] RAM retrigger

1: Download calibration data from EEPROM.

0: Download complete or inactive

[8] Spread Spectrum Disable:

0: Main Clock Spread Spectrum Enabled

1: Main Clock Spread Spectrum Disabled

[7:1] Unused

[0] Stagger Enable:

1: Stagger Enabled.

0: Stagger Disabled.

Valid only when channel is in Fixed Frequency mode

## SOLENDR

**Solenoid drivers enable**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | | | | | | | | Solenoid Driver State_3 | | Solenoid Driver State_2 | | Solenoid Driver State_1 | | Solenoid Driver State_0 | |
| R | | | | | | | | RW | | RW | | RW | | RW | |

**Address:** Global Base Address + 0x01

**Type:** RW

**Reset:** 0x0055

**Description:** Solenoid Driver Configuration

[15:8] Unused

[7:6] Solenoid Driver State, Channel 3

00: Driver Off, OFF State Diagnostics disabled and masked

01 : Driver tristate. OFF DIAG depending on bit on config reg

10: Drives on in PWM. OFF DIAG off and masked

11: Drives on in full-on. OFF DIAG off and masked

[5:4] Solenoid Driver State, Channel 2

00: Driver Off, OFF State Diagnostics disabled and masked

01 : Drives tristate. OFF DIAG depending on bit on config reg

10: Drives on in PWM. OFF DIAG off and masked

11: Drives on in full-on. OFF DIAG off and masked

[3:2] Solenoid Driver State, Channel 1

00: Driver Off, OFF State Diagnostics disabled and masked

01 : Drives tristate. OFF DIAG depending on bit on config reg

10: Drives on in PWM. OFF DIAG off and masked

11: Drives on in full-on. OFF DIAG off and masked

[1:0] Solenoid Driver State, Channel 0

00: Driver Off, OFF State Diagnostics disabled and masked

01: Drives tristate. OFF DIAG depending on bit on config reg

10: Drives on in PWM. OFF DIAG off and masked

11: Drives on in full-on. OFF DIAG off and masked

## TIMEOUTSPICFG

**Timeout SPI configuration**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| unused | | | | | | | | | Timeout NR Reset | | Timeout Configuration | | | Enable Reset Latch | Disable Reset Latch |
| R | | | | | | | | | RW | | RW | | | RW | RW |

**Address:** Global Base Address + 0x02

**Type:** RW

**Reset:** 0x0028

**Description:** SPI TIMEOUT Configuration Register

[15:7] Unused

[6:5] Number of SPI timeout events to force an internal reset

Timeout NR Reset [1:0]; Calculated as 2^(N+1) (e.g., default N= "01", Timeout Events = 4)

[4:2] Maximum time between valid SPI frames before SPI time-out fault flag is set.Timeout Configuration [2:0]: Calculated as follows:

504 x 2N [µs] (e.g., default N=B“010” means 2016 [µs])

[1] Enable Reset Latch - En_Res_Latch[1]:

0: Reset Latch Disabled

1: Reset Latch Enabled

[0] Disable Reset Latch - Dis_Res_Latch[0]

0: Reset Latch Enabled

1: Reset Latch Disabled

## FSCONF

**Fail safe pre-driver configuration**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | | | | FS_3_EN (only TQFP48) | FS3 Predriver Fault Threshold (only TQFP48) | | FS_2_EN (only TQFP48) | FS2 Predriver Fault Threshold (only TQFP48) | | FS_1_EN (only TQFP48) | FS1 Predriver Fault Threshold (only TQFP48) | | FS_EN/ FS_0_EN | FS/FS0 Predriver Fault Threshold | |
| R | | | | RW | RW | | RW | RW | | RW | RW | | RW | RW | |

**Address:** Global Base Address + 0x03

**Type:** RW

**Reset:** 0x0000

**Description:** Fail Safe Configuration and Enable

[15:12] Unused

[11] FS3 Predriver Enable – FS_3_EN (only TQFP48)

0: Fail Safe Predriver Disabled

1: Fail Safe Predriver Enabled

[10:9] FS3 Predriver Fault Threshold (only TQFP48)

00: 0.25V VDS Threshold

01: 0.5V VDS Threshold

10: 0.75V VDS Threshold

11: 1.0V VDS Threshold

[8] FS2 Predriver Enable – FS_2_EN (only TQFP48)

0: Fail Safe Predriver Disabled

1: Fail Safe Predriver Enabled

[7:6] FS2 Predriver Fault Threshold (only TQFP48)

00: 0.25V VDS Threshold

01: 0.5V VDS Threshold

10: 0.75V VDS Threshold

11: 1.0V VDS Threshold

[5] FS1 Predriver Enable – FS_1_EN (only TQFP48)

0: Fail Safe Predriver Disabled

1: Fail Safe Predriver Enabled

[4:3] FS1 Predriver Fault Threshold (only TQFP48)

00: 0.25V VDS Threshold

01: 0.5V VDS Threshold

10: 0.75V VDS Threshold

11: 1.0V VDS Threshold

[2] FS/FS0 Predriver Enable – FS_EN/FS_0_EN

0: Fail Safe Predriver Disabled

1: Fail Safe Predriver Enabled

[1:0] FS/FS0 Predriver Fault Threshold

00: 0.25V VDS Threshold

01: 0.5V VDS Threshold

10: 0.75V VDS Threshold

11: 1.0V VDS Threshold

## CHIPID

**Chip ID**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | | | | | | | | | Reserved | CHIP ID Version | | | CHIP ID SubVersion | | |

**Address:** Global Base Address + 0x1F

**Type:** Read Only

**Description:** Chip Identification Information

| Register Bit | Field name/description | Default values | Type |
|---|---|---|---|
| [15:7] | Unused | All "0" | Read |
| [6] | Reserved | 0 | Read |
| [5:3] | CHIP ID Version | 001 | Read |
| [2:0] | CHIP ID SubVersion | 011 | Read |

*Note: Reserved bit [6] should not be used by customer.*

## 9.9 Fault and test page summary

Table 41. **SPI fault and test page register address mapping**

| Idx [hex] | Register |
|---|---|
| 0x00 | Pin Status |
| 0x01 | On Demand Tests |
| 0x03 | Service Fault 1 |
| 0x04 | Service Fault 2 |
| 0x05 | Service Fault Mask 1 |
| 0x06 | Service Fault Mask 2 |
| 0x1D | Communication Faults |

## PINSTATUS

**Pin status**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | | | | | | | BUSY echo | SAFETYn echo | FAULTn echo | RES echo | IN 3 echo | IN 2 echo | IN 1 echo | IN 0 echo | EN_DR echo |

**Address:** Fault Test Base Address + 0x00

**Type:** R

**Reset:** 0b0000000X1XXXXXXX

**Description:** Echo Input Status & Internal Settings

[15:9] Unused

[8] Busy Echo - Internal signal set high when device is downloading data from EEPROM to various system control registers

[7] SAFETY echo - internal signal set low when the device has disabled the failsafe pre-driver using the parallel shutdown path

[6] FAULTn Pin echo - FAULTn pin status feedback

[5] RES Echo

1: RESn pin is Low

0: RESn pin is high

[4] IN 3 echo: IN3 Pin Status when in HW mode

0: Solenoid Channel 3 Enabled

1: Solenoid Channel 3 Disabled or SW mode selected

[3] IN 2 echo: IN2 Pin Status when in HW mode

0: Solenoid Channel 2 Enabled

1: Solenoid Channel 2 Disabled or SW mode selected

[2] IN 1 echo: IN1 Pin Status when in HW mode

0: Solenoid Channel 1 Enabled

1: Solenoid Channel 1 Disabled or SW mode selected

[1] IN 0 echo: IN0 Pin Status when in HW mode

0: Solenoid Channel 0 Enabled

1: Solenoid Channel 0 Disabled or SW mode selected

[0] EN_DR echo: EN_DR pin status

0: Driver Disabled

1: Driver Enabled

## ODTESTS

**On demand self tests**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | | | | | | | | | | | | | | | V3V3 Self Tests |
| R | | | | | | | | | | | | | | | RW |

**Address:** Fault Test Base Address + 0x01

**Type:** RW

**Reset:** 0x0000

**Description:** Global On Demand Self Tests

[15:1] Unused

[0] V3V3 Self Tests:

1: Start test

0: Test completeShould test fail, POR fault will be latched (SERVFLT1 register).

## SERVFLT1

**Service Fault 1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Digital Ground Loss | Analog Ground Loss | Fail safe pre-driver CH3 VDS fault (valid only for TQFP48 package) | Fail safe pre-driver CH2 VDS fault (valid only for TQFP48 package) | Fail safe pre-driver CH1 VDS fault (valid only for TQFP48 package) | Fail safe VDS Fault | POR flag | EEPROM Trimming Data CRC error | SPI Timeout Latch | SPI Timeout | VDD Over Voltage | VDD Under Voltage | CP Under Voltage | Configuration Register Monitor | VBATP Over Voltage | Core Over temperature |
| RH | RH | R | R | R | RH | RH | R | RH | RH | RH | RH | RH | RH | RH | RH |

**Address:** Fault Test Base Address + 0x03

**Type:** R

**Type:** 0x200

**Description:** Service Fault register stores Diagnostic flags of enabled services (i.e., Monitors)

[15] Digital Ground Loss (GNDD Loss)

0: No Fault
1: GND_D Loss

Clear on Read

[14] Analog Ground Loss (GNDA Loss)

0: No Fault
1: GND_A Loss

Clear on Read

[13] Fail safe pre-driver VDS fault CH3:

0: No Fault.

1: VDS fault detected

[12] Fail safe pre-driver VDS faul CH2:

0: No Fault.

1: VDS fault detected

[11] Fail safe pre-driver VDS fault CH1:

0: No Fault.

1: VDS fault detected

[10] Fail safe pre-driver VDS fault CH0:

0: No Fault

1: VDS fault detected

Clear on Read

[9] Power On Reset (POR) flag:

0: POR released and flag read

1: POR detected

Clear on Read

[8] EEPROM Trimming data CRC error:

0: No CRC error

1: CRC error

[7] SPI Timeout Latch:

0: No Fault

1: SPI Communication Timeout Latch Set

Clear on Read

[6] SPI Timeout:

0: No Fault

1: SPI Communication Timeout

Clear on Read

[5] VDD Over Voltage:

0: No Fault

1: Over Voltage Fault

Clear on Read

[4] VDD Under Voltage:

0: No Fault

1: Under Voltage Fault

Clear on Read

[3] Charge Pump Under Voltage:

0: No Fault

1: Under Voltage Fault

Clear on Read

[2] Configuration Register Monitor Solenoid Drivers Enable, Timeout SPI Config, FS Predriver Config

0: No Fault

1: Register Fault

Clear on Read

[1] VBATP Over Voltage:

0: No Fault

1: Over Voltage Fault

Clear on Read

[0] Core Over Temperature:

0: No Fault

1: Thermal Shutdown

Clear on Read

## SERVFLT2

**Service Fault 2**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clamp inhibit self-test | Clamp inhibit monitor | Unused | | | | | | VDD OV Self-test | VDD UV Self-test | Unused | VBAT OV Self-test | GNDLOSS D Self-test | GNDLOSS A Self-test | Diag Oscillator Stuck-at Monitor | Main Oscillator Monitor |
| RH | R | R | | | | | | RH | RH | R | RH | RH | RH | RH | RH |

**Address:** Fault_Test_BaseAddress + 0x04

**Type:** R

**Reset:** 0x0000

**Description:** Service Fault register stores Diagnostic flags of enabled services (i.e., Monitors & Self Tests)

[15] Clamp Diode Inhibit Selftest

Clear on Read

[14] Clamp Diode Inhibit Monitor

[13:8] Unused

[7] VDD OV Selftest

0: No Fault

1: Fault Detected

Clear on Read

[6] VDD UV Selftest

0: No Fault

1: Fault Detected

Clear on Read

[5] Unused

[4] VBAT OV Selftest

0: No Fault

1: Fault Detected

Clear on Read

[3] GNDLOSS D Selftest:

0: No Fault

1: Fault Detected

Clear on Read

[2] GNDLOSS A Selftest:

0: No Fault

1: Fault Detected

Clear on Read

[1] Diag Oscillator Stuck-at Monitor:

0: No Fault

1: Fault Detected

Clear on Read

[0] Main Oscillator Monitor:

0: No Fault

1: Fault Detected

Clear on Read

## SERVFLTMSK1

**Service Fault Mask 1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Digital Ground Loss | Analog Ground Loss | Fail Safe VDS Fault CH3 (valid only for TQFP48 package) | Fail Safe VDS Fault CH2 (valid only for TQFP48 package) | Fail Safe VDS Fault CH1 (valid only for TQFP48 package) | Fail Safe VDS Fault CH 0 | Unused | EEPROM Trimming data CRC error | SPI Timeout Latch | SPI Timeout | Unused | VDD Under Voltage | CP Under Voltage | Configuration Register | VBATP Over Voltage | Core Over Temperature |
| RW | RW | R | | | RW | R | RW | RW | RW | R | RW | RW | RW | RW | RW |

**Address:** Fault_Test_BaseAddress + 0x05

**Type:** RW

**Reset:** 0xFFFF

**Description:** Service Fault Mask register allows the user to map specific fault flags to the FAULTn pin. Setting mask bit high disables (masks) fault from setting FAULTn pin.

[15] Digital Ground Loss:
0: Mask Disabled
1: Mask Enabled

[14] Analog Ground Loss:
0: Mask Disabled
1: Mask Enabled

[13] Fail Safe VDS Fault CH3:
0: Mask Disabled
1: Mask Enabled

[12] Fail Safe VDS Fault CH2:
0: Mask Disabled
1: Mask Enabled

[11] Fail Safe VDS Fault CH1:
0: Mask Disabled
1: Mask Enabled

[10] Fail Safe VDS Fault CH0:
0: Mask Disabled
1: Mask Enabled

[9] Unused

[8] EEPROM Trimming data CRC error:

0: Mask Disabled

1: Mask Enabled

[7] SPI Timeout Latch:

0: Mask Disabled

1: Mask Enabled

[6] SPI Timeout:

0: Mask Disabled

1: Mask Enabled

[5] Unused

[4] VDD Under Voltage:

0: Mask Disabled

1: Mask Enabled

[3] CP Under Voltage:

0: Mask Disabled

1: Mask Enabled

[2] Configuration Register

0: Mask Disabled

1: Mask Enabled

[1] VBATP Over Voltage:

0: Mask Disabled

1: Mask Enabled

[0] Core Over Temperature:

0: Mask Disabled

1: Mask Enabled

## SERVFLTMSK2

**Service fault mask 2**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | Clamp Inhibit Monitor | Unused | | | | | | SPI Protocol Error | Unused | | IN 3 echo | IN 2 echo | IN 1 echo | IN 0 echo | EN_DR echo |
| R | RW | R | | | | | | RW | R | | RW | RW | RW | RW | RW |

**Address:** Fault Test Base Address + 0x06

**Type:** RW

**Reset:** 0xFFFF

**Description:** Service Fault Mask register allows the user to map specific fault flags to the FAULTn pin. Setting mask bit high disables (masks) fault from setting FAULTn pin.

[15] Unused

[14] Clamp Inhibit Monitor

0: Mask Disabled

1: Mask Enabled

[13:8] Unused

[7] SPI Protocol Error

0: Mask Disabled

1: Mask Enabled

[6:5] Unused

[4] IN3

0: Mask Disabled

1: Mask Enabled

[3] IN2

0: Mask Disabled

1: Mask Enabled

[2] IN1

0: Mask Disabled

1: Mask Enabled

[1] IN0

0: Mask Disabled

1: Mask Enabled

[0] EN_DR

0: Mask Disabled

1: Mask Enabled

## COMMUNICATIONFLTS

**SPI communications faults**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | | | Frame Counter Error Flag | CRC Error Flag | Short Frame Flag | Loong Frame Flag | Unused | | | | | | | | |

**Address:** Fault_Test_BaseAddress + 0x1D

**Type:** R

**Reset:** 0x0000

**Description:** SPI communication faults monitors

[15:13] Unused

[12] Frame Counter Error Flag

0: No Fault

1: Wrong Counter Value

[11] CRC Error Flag

0: No Fault

1: CRC Check Fault

[10] Short Frame Flag

0: No Fault

1: Frame bits received < 16

[9] Long Frame Flag

0: No Fault

1: Frame bits received > 16

[8:0] Unused

## 9.10 Channel page registers

Table 42. **SPI channel page register address mapping**

| Idx [hex] | Register |
|---|---|
| 0x00 | Exceptions 1 |
| 0x01 | Exceptions 2 |
| 0x02 | Configuration 1 |
| 0x03 | Configuration 2 |
| 0x04 | Dither Programming 1 |
| 0x05 | Dither Programming 2 |
| 0x06 | Current Set Point |
| 0x07 | Control Configuration |
| 0x08 | Frequency Control |
| 0x09 | Gains Configuration |
| 0x0A | Integrator Limit |
| 0x0B | Average Current |
| 0x0C | PWM Sense |
| 0x0D | Driver Fault Mask 1 |
| 0x0E | Driver Fault Mask 2 |
| 0x0F | Base H/L Delta Current |
| 0x10 | Measured H/L Delta Current |
| 0x11 | Temperature Monitor |
| 0x14 | Integrator Output |

## EXCEPTIONS1

**Exceptions 1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| T_WARN | EEPROM CRC error on CSA Calibration data | EEPROM CRC error on A2D trimming bits | PWM check fault | PWM check comp mismatch | Solenoid Logic BIST Status | | Solenoid Diag Self Test | | Open Load | Short Detection | Solenoid ADC mismatch Monitor | LS clamp active | HS over current | LS over current | T_SD |
| RH | R | R | RH | RH | R | | RH | | RH | RH | RH | RH | RH | RH | RH |

**Address:** Channel_X_BaseAddress + 0x00

**Reset** 0x0000

**Description:** Solenoid Driver Fault Status

[15] Thermal Warning (T_WARN):

0: No Fault
1: Thermal Warning Present

Clear on Read

[14] EEPROM CRC Error on CSA Calibration Data:

0: No Fault
1: CRC Error

Read

[13] EEPROM CRC error on A2D trimming bits:

0: No Fault
1: CRC Error

Read

[12] PWM Check Fault (ON State):

0: No Fault
1: Fault

Clear on Read

[11] PWM Check Comp Mismatch (ON State):

0: No Fault
1: Fault

Clear on Read

[10:9] Solenoid Logic BIST Status: (ADC mismatch, out of regulation, Solenoid driver control loop)

00: Idle

01: BIST running

10: BIST passed
11: BIST failed

Read

[8:7] Solenoid Diag Self Test (OFF State):

00: Self Test pass

01: DIAG_LV comparator fail

10: DIAG OL comparator fail

11: Self Test fail

Clear on Read

[6] Open Load (OFF State):

0: No Fault

1: Open load

Clear on Read

[5] Short Detection (OFF State):

0: No Fault

1: Short Detected

Clear on Read

[4] Solenoid ADC Mismatch monitor:

0: No Fault

1: Mismatch Fault Detected

Clear on Read

[3] LS Clamp Active (ON state):

0: No Fault

1: LS Clamp Activated

Clear on Read

[2] HS Over Current (ON State)

0: No Fault

1: HS Over Current

Clear on Read

[1] LS Over Current (ON State)

0: No Fault

1: LS Over Current

Clear on Read

[0] T_SD: (Thermal Shutdown)

0: No Fault

1: Thermal Shutdown Fault

Clear on Read

## EXCEPTIONS2

**Exceptions 2**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| unused | | | | | | | | | | GND_SOL loss self test | Out of regulation | GND_SOL loss fault | RAM CRC error | HS/LS compare Fault | Configuration Register Monitor |
| R | | | | | | | | | | RH | RH | RH | RH | RH | RH |

**Address:** Channel_X_BaseAddress + 0x01

**Type:** RH

**Reset:** 0x0000

**Description:** Solenoid Driver Fault Status

[15:6] Unused

[5] GND_SOL Loss Self Test Status

0: Test Complete

1: Test Running

Clear on Read

[4] Out of regulation

0: No Fault

1: Out of Regulation After 8 PWM Cycles

Clear on Read

[3] GND_SOL loss fault

0: No Fault

1: Solenoid Ground Loss Detected

Clear on Read

[2] RAM CRC error

0: No Fault

1: CRC Fault Detected on RAM Read

Clear on Read

[1] HS/LS compare Fault:

0: No Fault

1: Fault Detected

Clear on Read

[0] Configuration Register Monitor:

0: No Fault

1: Fault Detected

Clear on Read

## CONFIGURATION1

**Configuration 1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| unused | OFS_CMP_DIS | CALIBRATION_DIS | unused | | Solenoid Logic BIST | Td_Blank | HILOAD | unused | Overcurrent threshold selection | Enable OFF Diagnosis | unused | Solenoid Load Configuration | Current Feedback Control Mode | Output Slew Rate | |
| R | RW | RW | R | | RW | RW | RW | RW | RW | RW | R | RW | RW | RW | |

**Address:** Channel_X_BaseAddress + 0x02

**Type:** RW

**Reset:** 0x0000

**Description:** Configuration Register provides information related to channel configuration

[15] Unused

[14] OFS_CMP_DIS:

0: Current Sense Offset Compensation Active

1: Current Sense Offset Compensation disabled

[13] CALIBRATION_DIS:

0: Digital Current Sense Calibration Active

1: Digital Current Sense Calibration Disabled

[12:11] Unused

[10] Solenoid Logic BIST:

0: Logic BIST Reset

1: Logic BIST Enabled

[9] Td_Blank:

0: Long Blanking Time

1: Short Blanking Time

[8] HILOAD: Current Sense Scale

0: 1.5A Max Current Range

1: 2.0A Max Current Range

[7] Unused

[6] Overcurrent threshold selection:

0: 4A Theshold

1: 5A Threshold

[5] Enable OFF Diagnosis:

0: Disabled (OFF)

1: Enabled

[4] Unused

[3] Solenoid Load Configuration:

0: Low Side

1: High Side

[2] Current Feedback Control Mode:

0: HW Feedback

1: SW Feedback

[1:0] Output Slew Rate:

00: 0.4V/µs

01: 1.0V/µs

10: 4.0V/µs

11: 8.0V/µs

## CONFIGURATION2

**Configuration 2**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | | | | | | | | | | | | | | Solenoid Diag Self Test | GND_SOL loss self test |
| R | | | | | | | | | | | | | | RW | RW |

**Address:** Channel_X_BaseAddress + 0x03

**Type:** RW

**Reset:** 0x0000

**Description:** Configuration Register for channel configuration self-tests. Before restarting any tests, wait for the register to return to "0"

[15:2] Unused

[1] Solenoid Diag Self Test: Short, Open Load and PWM Check

0: Self Test Disabled

1: Self Test Enabled

[0] GND_SOL loss self test

0: Self TestDisabled

1: Self Test Enabled

## DITHPGM1

**Dither programming 1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dither Enable | DITHER_SYNC_EN | SYNC TYPE | Unused | | | | | Istep | | | | | | | |
| RW | RW | RW | R | | | | | RW | | | | | | | |

**Address:** Channel_X_BaseAddress + 0x04

**Type:** RW

**Reset:** 0x0050

**Description:** Dither Generator Configuration

[15] Dither Enable:
0: Disabled
1: Enabled

[14] DITHER_SYNC_EN:
0: Disabled
1: Enabled

[13] SYNC TYPE:
0: Dither Synchronization at each Dither Step
1: Dither Synchronization at each dither Period

[12:8] Unused

[7:0] Istep: Current step Value

## DITHPGM2

**Dither programming 2**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | | | Nstep | | | | | Unused | | Tstep | | | | | |
| R | | | RW | | | | | R | | RW | | | | | |

**Address:** Channel_X_BaseAddress + 0x05

**Type:** RW

**Reset:** 0x028A

**Description:** Dither Generator Configuration

[15:13] Unused

[12:8] Nstep: Number of steps in a quarter of dither period

[7:6] Unused

[5:0] Tstep: Number of PWM cycles for each dither step

## SETPOINT

**Current set point**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Auto Limit | unused | | Current Set Point code | | | | | | | | | | | | |
| RW | R | | RW | | | | | | | | | | | | |

**Address:** Channel_X_BaseAddress + 0x06

**Type:** RW

**Reset:** 0x0000

**Description:** Register stores current setpoint code (HW mode current control). Current Control SETPOINT is coded into 13 bits. Current value depends on HILOAD bit.

[15] Auto Limit: Activates the transient mode on set point change

0: Inactive

1: Active

[14:13] Unused

[12:0] Current Set Point Code

## CTRLCFG

**Control configuration**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Transition Time | | Unused | | HW Feedback Frequency Mode | Target PWM Period Code | | | | | | | | | | |
| RW | | R | | RW | RW | | | | | | | | | | |

**Address:** Channel_X_BaseAddress + 0x07

**Type:** RW

**Reset:** 0x0000

**Description:**

[15:14] Transition Time: Too long period detection (if the current PWM time exceeds this threshold, the controller enters the transient state):

00: 2.5 * Tpwm

01 : 4.5 * Tpwm

10: 8.5 * Tpwm

11 : 16.5 * Tpwm

[13:12] Unused

[11] HW feedback Frequency Mode:

0: Fixed Frequency

1: Variable Frequency

[10:0] Target PWM Period Code

## KFREQCTRL

**Frequency control**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | | | | | | | | | | KFI | | | FINT_START | | |
| R | | | | | | | | | | RW | | | RW | | |

**Address:** Channel_X_BaseAddress + 0x08

**Type:** RW

**Reset:** 0x002F

**Description:** Register stores KF, FCIL (Variable frequency forward gain: HW mode current control)

[15:6] unused

[5:3] KFI: Integral Gain of Frequency Control Loop

[2:0] FINT_START: Start value for frequency integrator upon exiting transient mode

## KGAINS

**Gains configuration**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | | | | | | | | | | KI | | | KP | | |
| R | | | | | | | | | | RW | | | RW | | |

**Address:** Channel_X_BaseAddress + 0x09

**Type:** RW

**Reset:** 0x0024

**Description:** Register stores KI (Integral error gain: HW mode current control) and KP (Proportional error gain: HW mode current control).

[15:6] unused

[5:3] KI: Integral Gain of HW current control loop (fixed & variable freq.)

[2:0] KP: Proportional Gain of HW current control loop (fixed freq. only)

## INTGLIM

**Integrator limit**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INT_OUT_SEL | | unused | | | | | | NEGINTLIM | | | | POSINTLIM | | | |
| RW | | R | | | | | | RW | | | | RW | | | |

**Address:** Channel_X_BaseAddress + 0x0A
**Type:** RW
**Reset:** 0x0000
**Description:** --

[15:14] INT_OUT_SEL:
00: Integrator Low Threshold
01: Integrator High Threshold
10: Integrator Min Level
11: Integrator Max Level
[13:8] Unused
[7:4] NEGINTLIM
[3:0] POSINTLIM

## AVGCUR

**Average current**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | | AVGCUR | | | | | | | | | | | | | |

**Address:** Channel_X_BaseAddress + 0x0B
**Type:** R
**Reset:** 0x0000
**Description:** Stores Average Current Code in 1 PWM period

[15:14] Unused
[13:0] AVGCUR: Average current code (signed) in 1 PWM period

## PWMSENSE

**PWM sense**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMOUT | | | | | | | | PWM Code | | | | | | | |
| RH | | | | | | | | R | | | | | | | |

**Address:** Channel_X_BaseAddress + 0x0C

**Type:** RH

**Reset:** 0x0000

**Description:** PWM period out of range flag (TMOUT). PWM code: measured effective PWM period

[15] TMOUT

0: No Fault
1: Fault Detected

Clear on Read

[14:0] PWM Code

## DRVFLTMASK1

**Driver fault mask 1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E_SOL_TW | EEPROM CRC Error on CSA Calibration Data Mask | EEPROM CRC Error on A2D Trimming Bits Mask | PWM check fault | PWM Check Comp Mismatch | Unused | | | | E_SOL_OL | E_SOL_SHORT | E_SOL_A2D | E_LSCLAMP | E_SOL_HSOVC | E_SOL_LSOVC | E_SOL_OT |
| RW | RW | RW | RW | RW | R | | | | RW | RW | RW | RW | RW | RW | RW |

**Address:** Channel_X_BaseAddress + 0x0D

**Type:** RW

**Reset:** 0xFFFF

**Description:** Driver Fault Mask register is an active High Mask register for Driver Faults. Setting mask bit disables corresponding fault from generating interrupt on FAULT pin.

[15] E_SOL_TW: Solenoid Driver Thermal Warning

0: NOT Masked

1: MASKED

[14] EEPROM CRC error on CSA Calibration data Mask:

0: NOT Masked

1: MASKED

[13] EEPROM CRC error on A2D trimming bits Mask:

0: NOT Masked

1: MASKED

[12] PWM Check Fault:

0: NOT Masked

1: MASKED

[11] PWM Check Comp Mismatch:

0: NOT Masked

1: MASKED

[10:7] Unused

[6] E_SOL_OL: Open Load Fault Mask

0: NOT Masked

1: MASKED

[5] E_SOL_SHORT: Solenoid Short Fault Mask

0: NOT Masked

1: MASKED

[4] E_SOL_A2D: Solenoid ADC Mismatch Fault Mask

0: NOT Masked

1: MASKED

[3] E_LSCLAMP: Low Side Clamp Active Fault Mask

0: NOT Masked

1: MASKED

[2] E_SOL_HSOVC: High Side Over Current Fault Mask

0: NOT Masked

1: MASKED

[1] E_SOL_LSOVC: Low Side Over Current Fault Mask

0: NOT Masked

1: MASKED

[0] E_SOL_OT: Solenoid Driver Over Temperature Fault Mask

0: NOT Masked

1: MASKED

## DRVFLTMASK2

**Driver fault mask 2**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | | | | | | | | | | | Out of regulation | GND_SOL loss fault | E_RAM_CRC_ERR | E_SOL_HS/LS | E_CFG_REG_FAIL |
| R | | | | | | | | | | | RW | RW | RW | RW | RW |

**Address:** Channel_X_BaseAddress + 0x0E

**Type:** RW

**Reset:** 0xFFFF

**Description:** Driver Fault Mask register is an active Hi Mask register for Driver Faults. Setting mask bit disables corresponding fault from generating interrupt on FAULT pin

[15:5] unused

[4] Out of regulation

0: NOT Masked

1: MASKED

[3] GND_SOL loss fault

0: NOT Masked

1: MASKED

[2] RAM CRC error

0: NOT Masked

1: MASKED

[1] E_SOL_HS/LS:

0: NOT Masked

1: MASKED

[0] E_CFG_REG_FAIL:

0: NOT Masked

1: MASKED

## BSHLDELTACURR

**Base H/L delta current**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | | | | | | | | Base Delta Current | | | | | | | |
| R | | | | | | | | RW | | | | | | | |

**Address:** Channel_X_BaseAddress + 0x0F

**Type:** RW

**Reset:** 0x0000

**Description:** Base High Side/Low Side Delta Current

[15:8] Unused

[7:0] Base Delta Current: Base High Side/Low Side Delta Current

## MEASHLDELTACURR

**Measure H/L delta current**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| unused | | | | | | | | Meas Delta Current | | | | | | | |
| R | | | | | | | | RW | | | | | | | |

**Address:** Channel_X_BaseAddress + 0x10

**Type:** R

**Reset:** 0x0000

**Description:** Measured H/L Delta current

[15:8] Unused

[7:0] Measured Base Delta Current Between High & Low Side

## TEMPMON

**Temperature monitor**


**Address:** Channel_X_BaseAddress + 0x11

**Type:** R

**Reset:** 0x0000

**Description:** Temperature Monitor

[15:8] Unused

[7:0] Temperature Monitor: Unsigned

## INTOUT

**Integrator output**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | INTOUT | | | | | | | |

**Address:** Channel_X_BaseAddress + 0x14

**Type:** R

**Reset:** 0x0000

**Description:** Integrator Output Monitor

[15:0] Integrator Output Monitor: Unsigned

# 10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 10.1 TQFP48 (7x7x1 mm exp. pad down 5.0x5.0) package information

**Figure 28. TQFP48 (7x7x1 mm exp. pad down 5.0x5.0) package outline**

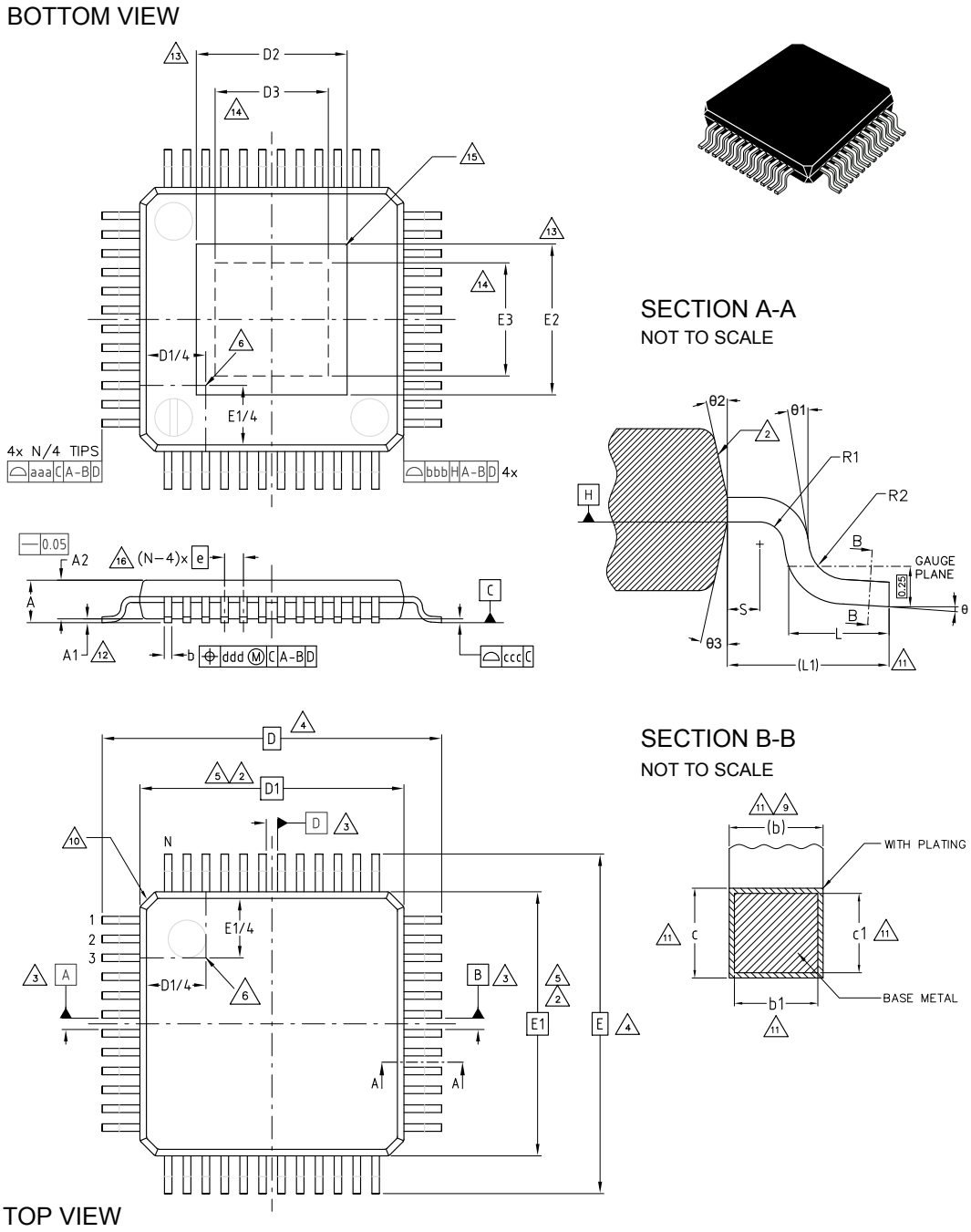


Table 43. **TQFP48 (7x7x1 mm exp. pad down 5.0x5.0) package mechanical data**

| Symbol | Dimensions | | | Note |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| Θ | 0° | 3.5° | 7° | |
| Θ1 | 0° | | | |
| Θ2 | 10° | 12° | 14° | |
| Θ3 | 10° | 12° | 14° | |
| A | | | 1.20 | 15 |
| A1 | 0.05 | | 0.15 | 12 |
| A2 | 0.95 | 1.00 | 1.05 | 15 |
| b | 0.17 | 0.22 | 0.27 | 9, 11 |
| b1 | 0.17 | 0.20 | 0.23 | 11 |
| c | 0.09 | | 0.20 | 11 |
| c1 | 0.09 | | 0.16 | 11 |
| D | 9.00 BSC | | | 4 |
| D1 | 7.00 BSC | | | 2, 5 |
| D2 | | | | 13 |
| D3 | | | | 14 |
| e | 0.50 BSC | | | |
| E | 9.00 BSC | | | 4 |
| E1 | 7.00 BSC | | | 2, 5 |
| E2 | | | | 13 |
| E3 | | | | 14 |
| L | 0.45 | 0.60 | 0.75 | |
| L1 | 1.00 REF | | | |
| N | 48 | | | 16 |
| R1 | 0.08 | | | |
| R2 | 0.08 | | 0.20 | |
| S | 0.20 | | | |
| **Tolerance of form and position** | | | | |
| aaa | 0.20 | | | 1, 7, 20 |
| bbb | 0.20 | | | |
| ccc | 0.08 | | | |
| ddd | 0.08 | | | |

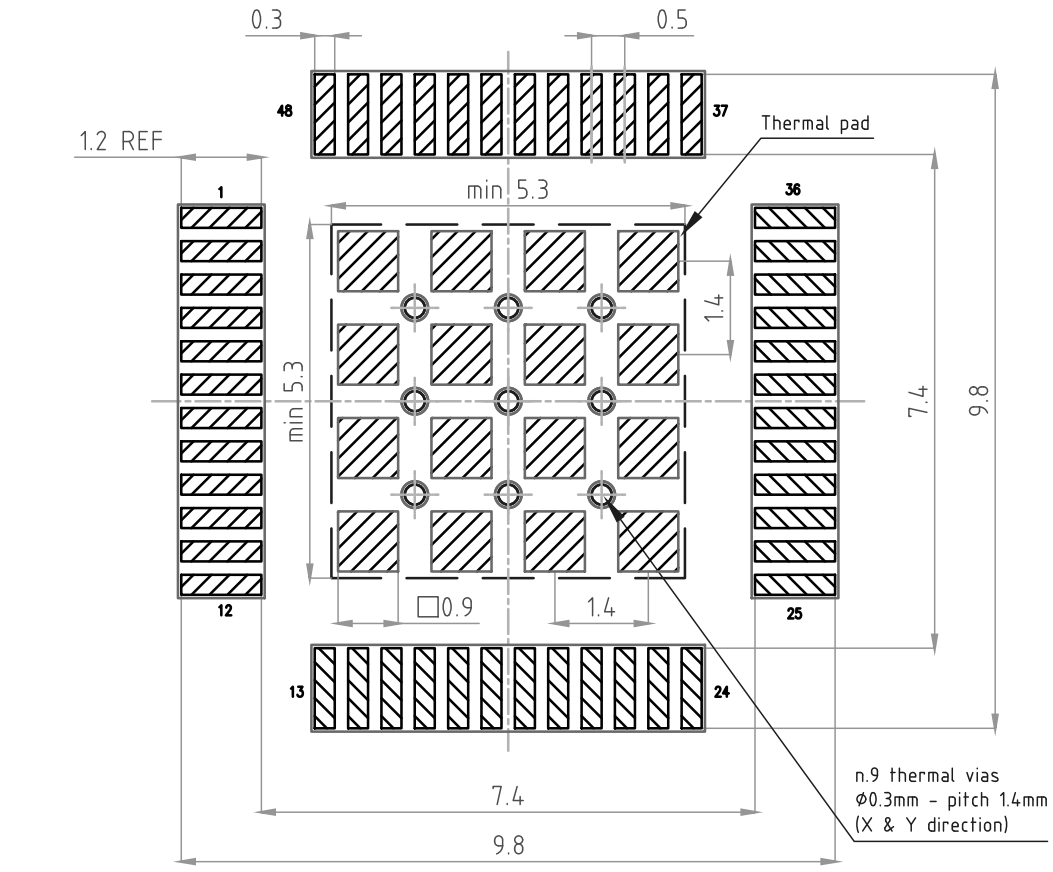
**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size up to 0.15 mm.
3. Datum A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.

8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the number of terminal positions for the specified body size.

## 10.2 TQFP48 (7x7x1.0 exposed pad down) footprint

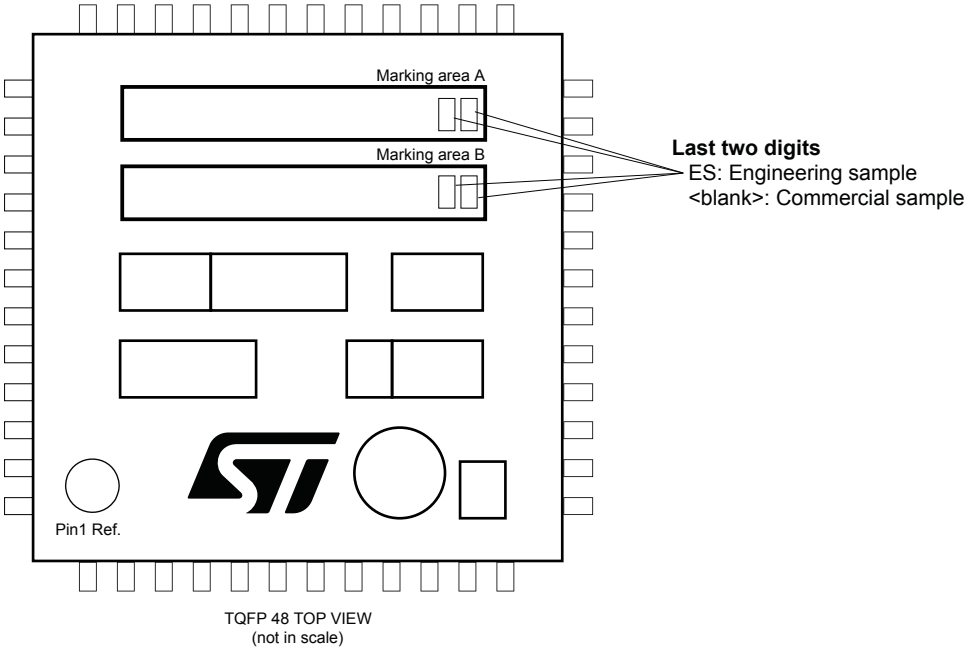
Figure 29. **TQFP48 (7x7x1.0 exposed pad down) footprint**




*NOTE:*
*This is a draft proposal only and it might be not in line with customer or pcb supplier design rules.*

## 10.3 TQFP48 marking information

Figure 30. **TQFP48 marking information**




Parts marked as ‘ES’ are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 10.4 PowerSSO-36 (7.2x4.75 mm option C exposed pad down) package information

**Figure 31. PowerSSO-36 (7.2x4.75 mm option C exposed pad down) package outline**

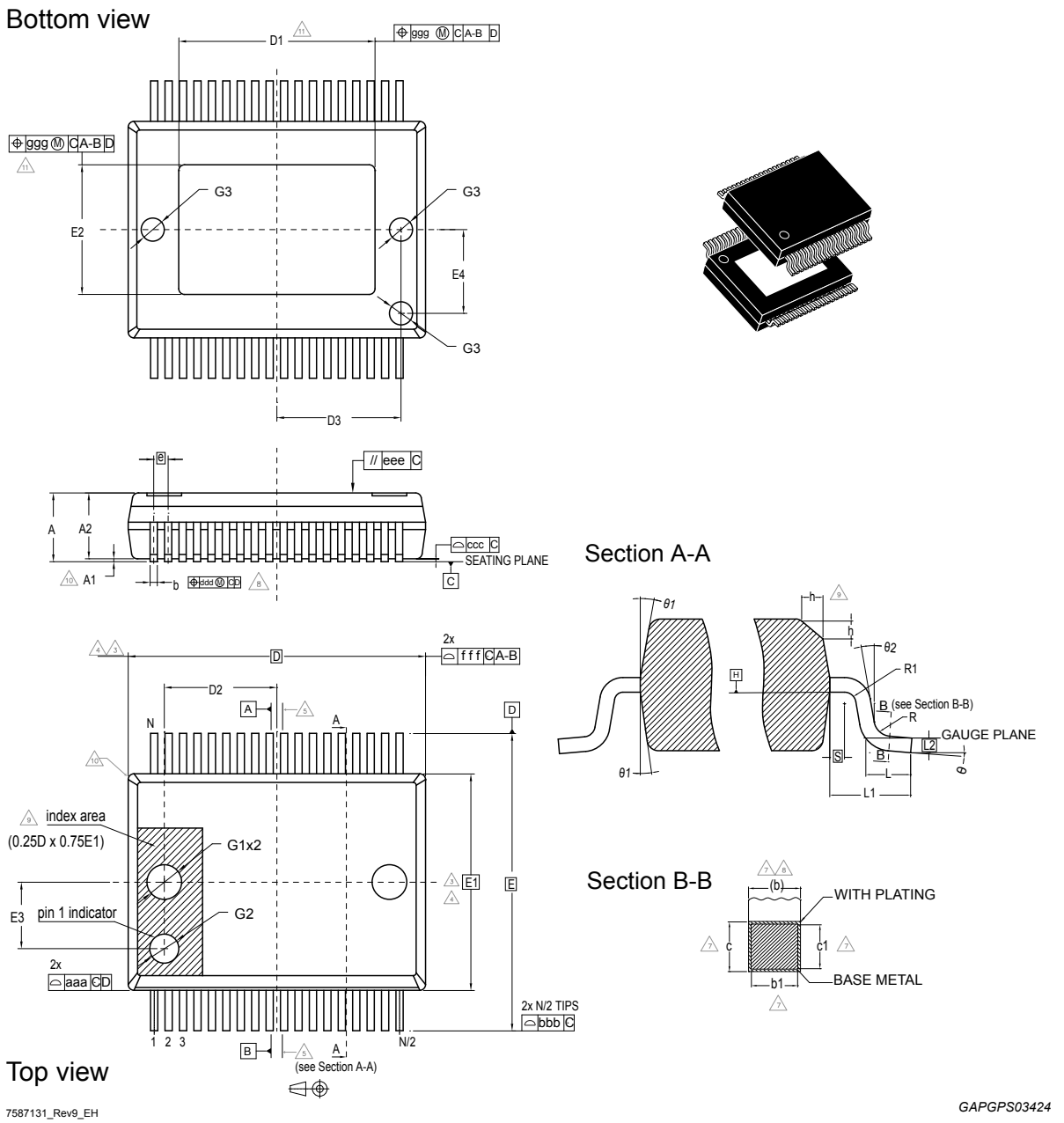



**Table 44. PowerSSO-36 (exposed pad down) package mechanical data**

| Symbol | Dimensions | | | Note |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| Θ | 0° | - | 8° | |
| Θ1 | 5° | - | 10 | |
| Θ2 | 0° | - | - | |
| A | 2.15 | - | 2.45 | |
| A1 | 0.00 | - | 0.10 | 10 |

| Symbol | Dimensions | | | Note |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| A2 | 2.15 | - | 2.35 | |
| b | 0.18 | - | 0.32 | 7, 8 |
| b1 | 0.13 | 0.2 | 0.30 | 7, 8 |
| c | 0.23 | - | 0.32 | 7 |
| c1 | 0.20 | 0.20 | 0.30 | 7 |
| D | | 10.30 BSC | | 3, 4 |
| D1 | | **VARIATION** | | 11 |
| D2 | - | 3.65 | - | |
| D3 | - | 4.30 | - | |
| e | | 0.50 BSC | | |
| E | | 10.30 BSC | | |
| E1 | | 7.50 BSC | | 3, 4 |
| E2 | | **VARIATION** | | 11 |
| E3 | - | 2.30 | - | |
| E4 | - | 2.90 | - | |
| G1 | - | 1.20 | - | |
| G2 | - | 1.00 | - | |
| G3 | - | 0.80 | - | |
| h | 0.30 | - | 0.40 | 9 |
| L | 0.55 | 0.70 | 0.85 | |
| L1 | | 1.40 REF | | |
| L2 | | 0.20 BSC | | |
| N | | 36 | | 6 |
| R1 | 0.30 | - | - | |
| R2 | 0.20 | - | - | |
| S | 0.25 | - | - | |
| **Tolerance of form and position** | | | | |
| aaa | | 0.20 | | 1, 2 |
| bbb | | 0.20 | | |
| ccc | | 0.08 | | |
| ddd | | 0.08 | | |
| eee | | 0.10 | | |
| fff | | 0.20 | | |
| ggg | | 0.15 | | |
| **VARIATIONS** | | | | |
| D1 | 6.50 | - | 7.10 | A |
| E2 | 4.10 | - | 4.70 | |
| D1 | 4.90 | - | 5.50 | B |
| E2 | 4.10 | - | 4.70 | |
| D1 | 6.90 | - | 7.50 | C |

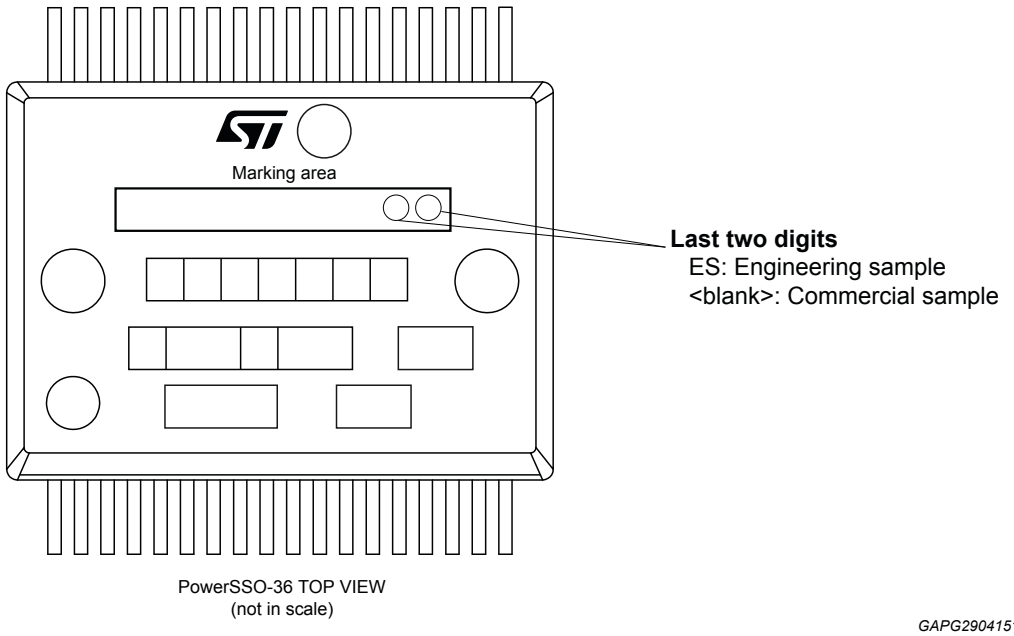
| Symbol | Dimensions | | | Note |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| E2 | 4.30 | - | 5.20 | C |

**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters.
3. Dimensions D and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side D and “0.15 mm” per side E1. D and E1 are Maximum plastic body size dimensions including mold mismatch.
4. The top package body size may be smaller than the bottom package size.
5. Datum A-B and D to be determined at datum plane H.
6. “N” is the max number of terminal positions for the specified body size.
7. The dimensions apply to the flat section of the lead between 0.10 to 0.25 mm from the lead tip.
8. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10 mm total in exceed of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This Chamfer feature is optional. If it is not present, then a PIN 1 identifier must be located within the index area indicated.
10. A1 is defined as the vertical distance from the seating plane to the lowest point on the package body.
11. Dimension D1 and E2 show the minimum allowed for the optional exposed pad. The size of exposed pad is variable depending of leadframe design pad size. End user should verify “D1” and “E2” dimensions for each device application.

## 10.5 PowerSSO-36 marking information

**Figure 32. PowerSSO-36 marking information**




Parts marked as ‘ES’ are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## Revision history

Table 45. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 12-Dec-2018 | 1 | Initial release. |
| 29-Mar-2019 | 2 | Updated:<br>*Section Product status / summary*;<br>*Section Features*. |
| 17-Jul-2019 | 3 | The confidentiality level is changed from "Restricted" to "Public". |
| 12-Feb-2020 | 4 | Updated:<br>Section *Features and Product summary;*<br>*Section 5.7 GND (GNDD, GNDA, GND_SOLx);*<br>*Table 4. Device operating temperature;*<br>*Table 33. Valve driver safety parameters*. |
| 06-Jul-2020 | 5 | Updated *Table 4. Device operating temperature;*<br>Minor text changes in *Features*. |
| 17-Dec-2020 | 6 | Updated:<br>*Section 9.8.5 CHIPID;*<br>*Section 9.10.3 CONFIGURATION1*.<br>Minor text changes in *Section 8.4.1 High side – low side current sense compare*. |
| 11-May-2021 | 7 | Minor text changes in *Section 6.1.8 Parallel mode*. |
| 25-Nov-2021 | 8 | Typo corrections. |
| 27-Feb-2024 | 9 | Updated *Table 33. Valve driver safety parameters*. |
| 04-Jun-2024 | 10 | Updated Table 9. Power supply electrical performance, Figure 8. HS driver (left) and LS driver (right) configuration, Section 8.4.5: Diagnostic comparators , Table 33. Valve driver safety parameters, SERVFLT1, SERVFLTMSK1, Table 43. TQFP48 (7x7x1 mm exp. pad down 5.0x5.0) package mechanical data and Section 10.2: TQFP48 (7x7x1.0 exposed pad down) footprint . |

# Contents

# List of tables

# List of figures

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.